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1979

Analogue circuits

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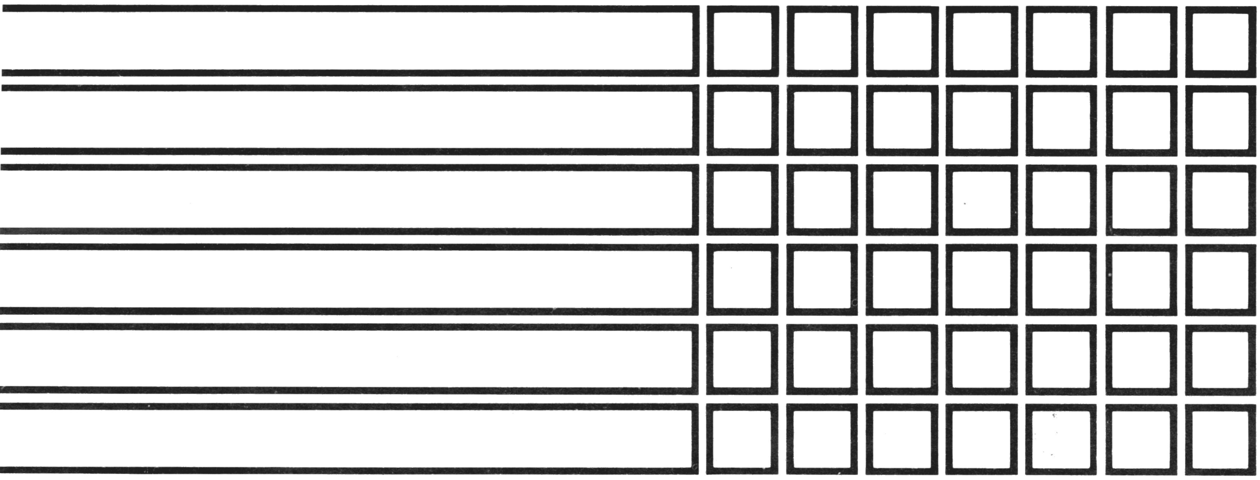
SIGNETICS ANALOG
–SPECIFICATIONS
–MILITARY SUMMARY

DATA MANUAL
1979



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INTRODUCTION

As one of the world's largest manufacturers of integrated circuits, Signetics designs, develops, manufactures, and sells over 1600 different types of integrated circuits. Signetics produces linear circuits utilizing both bipolar and metal-oxide semiconductor (MOS) manufacturing processes.

The Analog division is a major broad line supplier of both Signetics' original designs and industry standard devices. The NE5534 High Performance Operational Amplifier, the NE5018 microprocessor compatible DAC, and the NE5554 Dual Tracking Regulator are among Signetics' original products. The breadth of the Analog product line offers the designer, the component engineer, and the purchasing agent a varied approach to linear circuits.

This broad analog circuit product line is backed by Signetics' industry image as a quality manufacturer to whom the servicing of the customers' needs is paramount.

The 1979 Analog Data Manual is intended to serve as a single reference for linear circuits by presenting information necessary to select Signetics' analog products properly. The data manual is updated and rewritten to reflect data on new products issued.

Additions and errata will be generated at periodic intervals.

Your inputs to improve our publications will be greatly appreciated.

Ira Zingmond
Manager, Linear Applications

ORDERING INFORMATION

Signetics' Analog integrated circuit products may be ordered by contacting either the local Signetics sales office, Signetics representatives and/or Signetics authorized distributors. A complete listing is located in the back of this manual.

Minimum Factory Order:

Commercial Product:
  $1000 per order
  $50 per line item per order

Military Product:
  $250 per line item per order

Table 1 provides part number information concerning for both Signetics originated products and industry standard products.

Table 2 is a cross reference of both the old and new package suffixes for all presently existing types, while Table 3 and 4 provide appropriate explanations on the various prefixes employed in the part number descriptions.

As noted in Table 3, Signetics defines device operating temperature range by the appropriate prefix. It should be noted however, that devices with a SE prefix (-55°C to +125°C) indicates only its operating temperature range and *not* its military qualification status. The military qualification status of any analog product can be determined by either looking in the Military Section in this manual and/or contacting your local sales office.

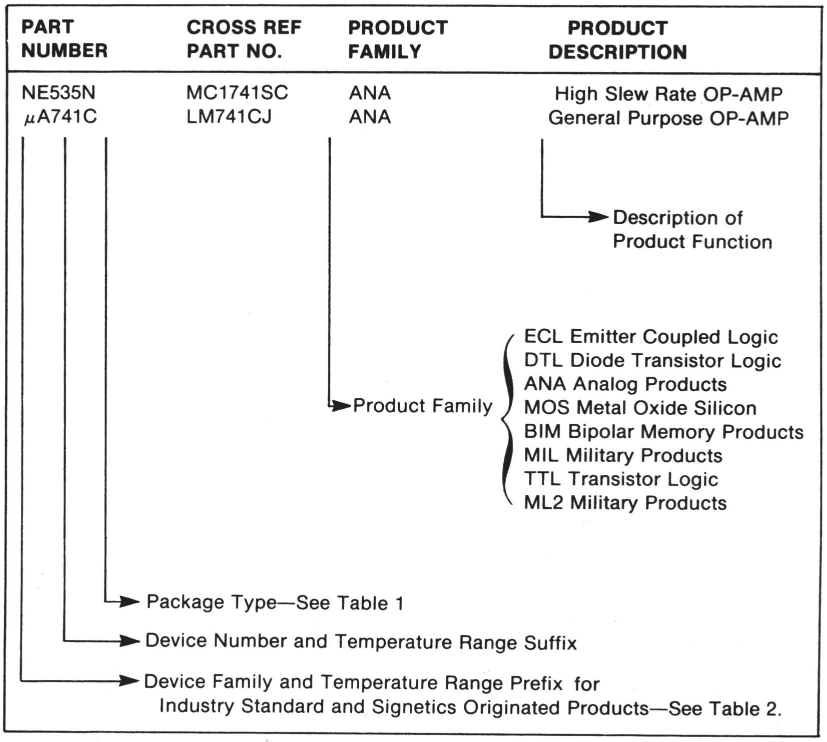

PART NUMBER
CROSS REF PART NO.
PRODUCT FAMILY
PRODUCT DESCRIPTION
NE535N
MC1741SC
ANA
High Slew Rate OP-AMP
μA741C
LM741CJ
ANA
General Purpose OP-AMP
Description of Product Function
Product Family
ECL Emitter Coupled Logic
DTL Diode Transistor Logic
ANA Analog Products
MOS Metal Oxide Silicon
BIM Bipolar Memory Products
MIL Military Products
TTL Transistor Logic
ML2 Military Products
Package Type—See Table 1
Device Number and Temperature Range Suffix
Device Family and Temperature Range Prefix for Industry Standard and Signetics Originated Products—See Table 2.

Table 1 PART NUMBER DESCRIPTION

SUFFIX		PACKAGE DESCRIPTION[2]
Old	New	
A,AA	N	14-lead plastic DIL
A	N-14	14-lead plastic DIL (Selected Analog products only)
B,BA	N	16-lead plastic DIL
DA	K	2-lead TO-3
DB	HB	3-lead TO-39
DC	DC	4-lead TO-46
DE	DE	4-lead TO-72
F	F	14, 16, 18, 22 and 24-lead ceramic (Cerdip) DIL
I,IK	I	14, 16, 18, 22, 28 and 4-lead ceramic DIL
K	K	10-lead TO-100
L	L	10-lead high-profile TO-100 can
NA,NX	N	24-lead plastic DIL
PN	PHA	12 + 1 GND pin DIL
Q,R	Q	10, 14, 16 and 24-lead ceramic flat
S	S	3-lead TO-92 plastic
SK	SK	Microprocessor kit
T,TA	T	8-lead TO-99
U	U	Plastic power TO-220
V	N	8-lead plastic DIL
W,WJ	W	10, 14, 16 and 24-lead ceramic (Cerpac) flat
XA	N	18-lead plastic DIL
XC	N	20-lead plastic DIL
XC	N	22-lead plastic DIL
XL,XF	N	28-lead plastic DIL

Table 2 PACKAGE DESCRIPTIONS

PREFIX	DEVICE TEMPERATURE RANGE
N-	0° to +70°C
S-	-55° to +125°C
NE-	0° to +70°C
SE-	-55° to +125°C
SA	-40° to +85°C
SU	-25° to +85°C

Table 3 DEVICE TEMPERATURE

PREFIX	DEVICE FAMILY
CA	Linear Industry Standard
DM	Linear Industry Standard
JB	Mil Rel—Jan Qualified—Old Designator
JM	Mil Rel—Jan Qualified—New Designator
LH	Linear Industry Standard
LM	Linear Industry Standard
M	Mil Rel—Jan Processed
MC	Linear Industry Standard
PA	Linear Industry Standard
SD	Linear DMOS
SP	DTL Series
UA	Linear Industry Standard
ULN	Linear Industry Standard

Table 4 FAMILY PREFIX

QUALITY AND RELIABILITY

Quality and reliability are two important measures of a product's merit. Quality is a measure of an integrated circuit's conformance to agreed-upon criteria at a given time, while Reliability is a measure of the circuit's ability to continue to conform over a period of time. The Signetics SUPR II Program has been designed to upgrade the basic product quality through the use of more rigorous screening criteria at the critical process steps. These additional screens constitute the Level A portion of the Program. A burn-in option is available for those users requiring enhanced reliability performance, and this option is designated as Level B.

Quality

The quality of an integrated circuit is appraised by the user based on the ability of the circuit to meet the specified electrical criteria and external visual appearance. The SUPR II Program focuses on supplying to the user a product that has a high probability of meeting the user's needs through the sampling plans defined in MIL-STD-105D and the quality levels (AQL's) stated in Table II. Many of the inspection methods at critical process steps are now based on MIL-STD-883 criteria in order to build, rather than test, quality into the product.

Reliability

System performance over a period of time is the user's measure of an integrated circuit's reliability. The SUPR II Program improves system reliability by building quality into the product via additional manufacturing inspections and the offering of a burn-in screen. In addition to the SUPR II Program, Signetics performs periodic reliability testing via the SURE II/883A Program to assure continuing uniformity and long-term reliability of all product lines. This data base is available upon request as is the ten-year reliability summary, Signetics Product Reliability Report, R-363.

How Do Integrated Circuit Failures Occur?

Results from the Signetics Failure Analysis Lab over a three-year period on product returned from board checkout, system checkout, field usage and accelerated life testing are graphically presented in Figure 1. Under typical system operating conditions, random manufacturing defects, as outlined in Table 1, are the primary cause of true device failure. Also shown in Table 1 are the process controls that have been added via the SUPR II Program to minimize these defects prior to shipment to the customer. The device failure models are categorized as:

Half of the devices analyzed were found to be electrically good. They are attributed to being "false pulls" that occur during normal troubleshooting at the board and system levels.

Devices damaged by electrical over-stress account for 25% of the failures. Typical causes for electrical over-stress are incorrect board insertion, board shorts between device pins, power supply transients, and poor handling techniques.

The remaining 25% were verified to be true failures which occurred as a result of an in-process manufacturing defect or test escape.

SIGNETICS SUPR II LEVEL A

Improved Quality Benefits

From the user's point of view, improved integrated circuit quality from the supplier means a lower cost of ownership. This cost saving can be effected through the reduction or elimination of involved incoming inspection testing, reduced PC board rework, simplified system checkout, reduced in-line inventories, and less complicated part tracking by Purchasing Management.

The SUPR II Program is Corporate in scope and covers Logic (Standard TTL, Schottky TTL, Low Power Schottky TTL, ECL, 8T Interface), Analog (Industrial, Consumer, Interface), Bipolar Memories (RAM's, ROM's, PROM's), and MOS Memories (RAM's, ROM's, Shift Registers), All package options are also available.

The SUPR II flow is detailed in Figure 5, including the test methods and Quality acceptance levels (Table 2 provides the electrical/mechanical finished product AQL's). Highlights of the flow are visual inspections, thermal shock preconditioning, hermeticity, and burn-in, all based on MIL-STD-883 criteria.

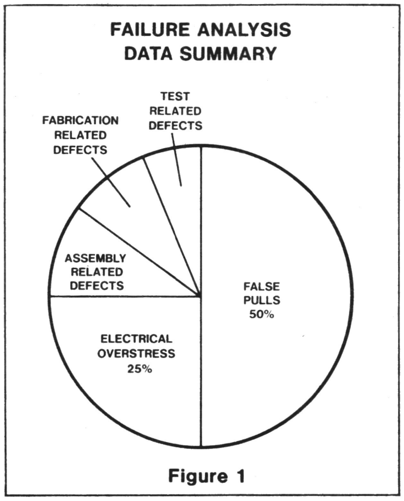


Figure 1

A good example of the savings which can be achieved by purchasing tighter inspection levels is given in Figure 2. Here we are comparing the various levels of inspection (AQL's) available for device functionality and its impact on the number of PC boards which must be reworked during system manufacturing. Using the standard commercial AQL in functionality of 1.0%, at 120 integrated circuit packages per board, typically more than 90% of boards will require rework. At 0.15% AQL, rework is reduced to 25%, and at 0.1%, typically only 12% rework is required.

SIGNETICS SUPR II LEVEL B

Infant Mortality Failures

Failure rates are most severe during the first few months of operating life. This is known as the "infant mortality" phase. A system

FAILURE MECHANISMS	CAUSES	SUPR II CONTROL
Die Fabrication Related	Metalization Oxide Defects Mechanical Scratches Contamination	SEM Monitor Visual Stabilization Bake Burn-In
Assembly Related	Bonding, Wire, Package and Seal Defects	Preseal Visual Thermal Shock Stabilization Bake Hermeticity Hot-Rail Testing
Test Related	Test Escapes	Tightened AQL Guarantees High Temperature Testing

Table 1

AQL LEVELS ON FUNCTIONALITY VERSUS BOARD REWORK RATES

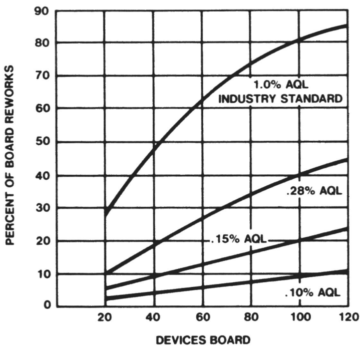


Figure 2

RELATIVE FAILURE RATE VERSUS TIME

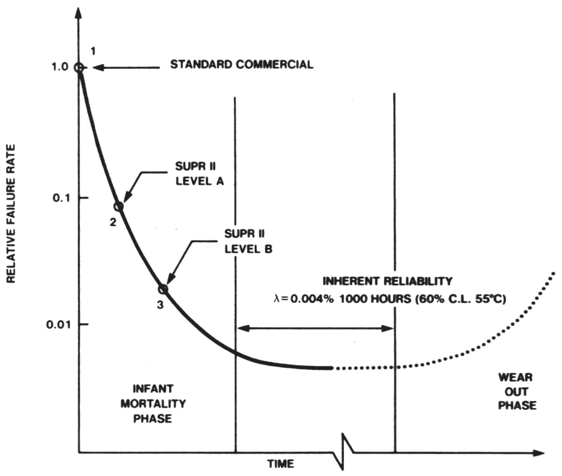


Figure 3

manufacturer has various options to solve problems arising from infant failures. He can ship his system to the end customer and repair field failures as they occur. He can operate the system in-house for this period and repair failures. Or he can purchase devices which have already been preconditioned to eliminate the early failures. Each customer must choose the most cost-effective method for his particular business. A considerable number of the reliabilty defects which cause early failures are eliminated by the manufacturing control and preconditioning steps of SUPR II Level A processing. More persistent defects can be removed by the use of "burn-in" techniques. The "burn-in" processing of SUPR II Level B effectively allows the system manufacturer to ship his equipment at Point 3 on the failure rate curve in Figure 3.

Burn-In Conditions

MIL-STD-883A, Method 1015 describes a number of different conditions for integrated

		ANALOG		BIPOLAR MEMORY		LOGIC		MOS/LSI	
		Plastic	Ceramic Metal Can	Plastic	Ceramic Metal Can	Plastic	Ceramic Metal Can	Plastic	Ceramic Metal Can
HOT OPENS	100°C	0.15%	-	0.15%	-	0.15%	-	0.15%	-
FUNCTIONALITY (NOTE 1)	25°C	0.15	0.15	0.25	0.25	0.10	0.10	0.25	0.25
	HIGH TEMPERATURE	0.25	0.25	-	-	0.10	0.10	0.25	0.25
D.C. PARAMETRIC	25°C	0.25	0.25	0.65	0.65	0.65	0.65	0.65	0.65
	OVER TEMPERATURE	0.65	0.65	0.65	0.65	0.65	0.65	0.65	0.65
A.C. PARAMETRIC	25°C	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
MECHANICAL	MAJOR	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25
	MINOR	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
SEAL TEST (CERAMIC METAL CAN ONLY)	FINE LEAK 1×10^{-7}cc/s	N/A	1.0	N/A	1.0	N/A	1.0	N/A	1.0
	GROSS LEAK 1×10^{-5}cc/s	N/A	0.65	N/A	0.65	N/A	0.65	N/A	0.65

NOTE

1. To insure AQL levels tighter than 0.65% on D.C. parameters usually requires continual correlation of test equipment between customer and vendor to avoid test interpretation problems. If the objective is to reduce system rework costs, functional operation of a device (does it switch or toggle in the system) is often more critical than the absolute value of a parameter. For this reason SUPR II focuses attention on tightened AQL's on functionality.

For analog devices, D. C. parameters, such as input current and offset voltages, tend to be more critical to system operation than for logic devices. A 0.25% AQL is therefore offered on analog D.C. parameters, with the realization that careful attention must be paid to establishing correlation at the customer's incoming inspection.

Table 2 SUPRA II AQL GUARANTEE

circuit burn-in. For SUPR II Level B, Signetics has selected Condition F. This is the accelerated burn-in method derived from MIL-STD-883A, utilizing a high temperature reversed bias condition. This bias scheme is preferred for infant mortality screening, while operating conditions are generally utilized for internal reliability programs oriented toward generating MTBF data for the system designer.

Integrated Burn-In Flow

Signetics SUPR II Level B burn-in is performed to provide reliability assurance equivalent to a 168-hour/125°C screen. This process has been integrated into the standard manufacturing flow to provide the customer with the most cost effective screen and significantly reduced delivery times.

BURN-IN FLOW

ASSEMBLY

The flow from SEM control through package seal is common to Levels A and B.

⇩

TEST

The pre-burn-in electrical screen is designed to remove assembly rejects and increase equipment efficiency.

⇩

BURN-IN

The 24-hour/155°C accelerated burn-in is well controlled to provide maximum screening effectiveness without damaging good devices.

⇩

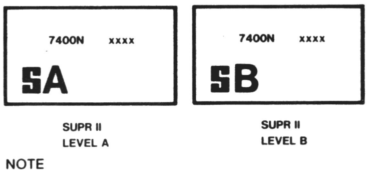
TEST

The post-burn-in electrical is a 100% production DC/function electrical test.

Figure 4

Marking Format

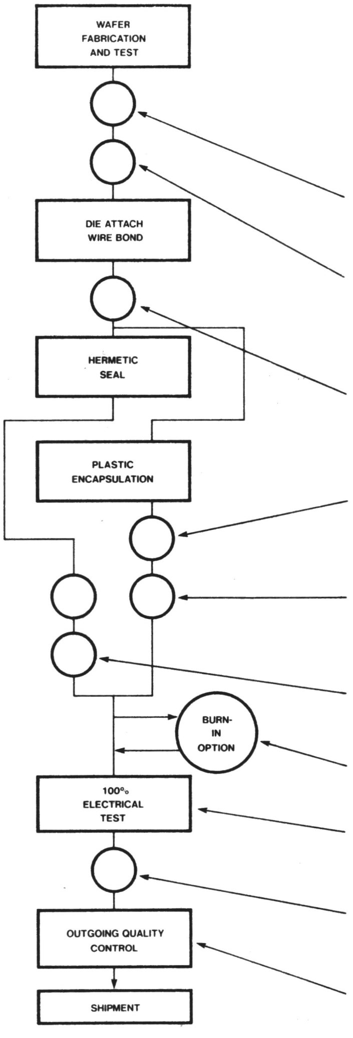
Product processed to the SUPR II manufacturing flow can be identified by an SA for Level A, and an SB for the Level B burn-in option.



NOTE
Marking for Level A in process of being implemented.

Figure 5 shows the generalized process flow for all Signetics integrated circuits purchased to the SUPR II program. Each product group (Analog, Bipolar Memory, Logic, and MOS) may follow slightly different procedures dictated by the specific device characteristics.

SUPR II PROCESS FLOW



SCANNING ELECTRON MICROSCOPE CONTROL (SEM)
Wafers are sampled daily by the Quality Control Laboratory from each fabrication area and subjected to SEM analysis. This process control reveals manufacturing defects such as contact and oxide step coverage in the metalization process which may result in early failures.

DIE SORT VISUAL ACCEPTANCE
Criteria based on MIL-STD-883, Method 2010, Condition B, are employed to detect defects caused during fabrication, wafer testing, or the mechanical scribe and break operation. Critical defects such as scratches, smears, and glassivated bonding pads are inspected to a 1% AQL. Lot acceptance for noncritical defects is to a 4% AQL.

PRE-SEAL VISUAL ACCEPTANCE
Criteria based on MIL-STD-883, Method 2010, Condition B, are employed to detect any damage incurred at the die attach and wire bonding stations. Critical defects such as scratches, contamination and smeared ball bonds are inspected to a 0.65% AQL. Lot acceptance is to 2.5% AQL.

STABILIZATION BAKE PRECONDITIONING
Plastic molded devices are baked to stress wire and die bonds and help eliminate marginal devices. It also ensures an optimum plastic seal to enhance moisture resistance.

THERMAL SHOCK PRECONDITIONING
MIL-STD-883, Method 1011, Condition A. Devices are cycled from cold to hot temperatures imposing a very severe stress which weakens loose bonds and package seals without degrading good devices. A loosened bond is later detected during high temperature "HOT-RAIL" testing. This preconditioning is especially effective in eliminating intermittent or "HOT-OPENS" problems in plastic devices.

SEAL TESTS
Package seal integrity is ensured by 100% gross leak testing per MIL-STD-883, Method 1014, Condition C and fine leak sampling per Condition A or B.

BURN-IN (LEVEL B OPTION)
Devices are burned in for the equivalent of 168 hours at 125°C in accordance with MIL-STD-883A, Method 1015, Condition F.

100% PRODUCTION ELECTRICAL TESTING
Every device is tested for functional and DC parameters at 25°C, room ambient.

HOT RAIL, HIGH TEMPERATURE TESTING
All plastic devices are subjected to testing at 100°C. In plastic devices this eliminates "HOT-OPENS" and shorts resulting from temperature sensitive intermittent bonds. In addition, logic circuits are tested 100% to a functional pattern that simulates usage in a system environment.

QA GUARANTEES
A final QA inspection step guarantees the mechanical and electrical AQL's of Table II. Every shipment is sealed and identified by QA personnel.

Figure 5

SURE II/883B RELIABILITY PROGRAM

Definition

Signetics is recognized as a manufacturer of reliable integrated circuits. Signetics realized long ago the need for a comprehensive reliability program to provide timely data representative of the entire Signetics product line. Thus the establishment of a Systematic and Uniform Reliability Evaluation program, known as SURE, which provides this data in a manner unique to the industry. Furthermore, this program is provided at no cost to customers.

The SURE Program is a Signetics in-house Qualification Test Program which has been in existence since 1963. The SURE Program is designed to monitor the continuing uniformity of all Signetics products and to demonstrate via periodic qualifications that Signetics products meet or exceed the stringent long-term reliability requirements of their intended applications.

The SURE Program is reviewed and modified annually to incorporate appropriate changes in military microelectronic test programs, products and demonstrated product capabilities, and market requirements. The 1978 SURE II/883B Reliability Program contains minor changes to the 1975 SURE II/883A Program, most significant of which is the inclusion of recent changes in military microelectronic test programs (i.e., inclusion of MIL-SD-883B, Method 5005.4 and MIL-M-3851OD). The SURE II/883B Program continues to incorporate additional environmental tests to fulfill the need for special reliability assurance of plastic products.

For more detailed information regarding the SURE II program, refer to Section 11 of the 1979 Signetics Analog Applications Manual.

SECTION I
OPERATIONAL AMPLIFIERS

Section 1—OPERATIONAL AMPLIFIERS

SE / NE530	High Slew Rate Operational Amplifier	26
SE / NE5530	High Slew Rate Operational Amplifier	26
NE / SE531	High Slew Rate Operational Amplifier	31
NE / SE532	Dual Operational Amplifier Single or Dual Power Supply	37
LM158 / 258 / 358	Dual Operational Amplifier Single or Dual Power Supply	37
NE5532 / 5532A	Internally Compensated Dual Low Noise Operational Amplifier	40
NE5533 / 5533A	Dual Low Noise Operational Amplifier	44
NE / SE5534 / 5534A	Single Low Noise Operational Amplifier	44
NE / SU536	FET Input Operational Amplifier	49
NE / SE5537	Sample and Hold Amplifier	54
NE538	Single High Slew Rate Operational Amplifier	61
NE5538	Dual High Slew Rate Operational Amplifier	61
LF155	High Performance JFET Input Op Amp (Low Supply Current)	*
LF156	High Performance JFET Input Op Amp (Wide Band)	*
LF198	Monolithic Sample and Hold Amplifier	66
LF298	Monolithic Sample and Hold Amplifier	66
LF398	Monolithic Sample and Hold Amplifier	66
LF255	High Performance JFET Input Op Amp (Low Supply Current)	*
LF256	High Performance JFET Input Op Amp (Low Supply Current)	*
LF355	High Performance JFET Input Op Amp (Low Supply Current)	*
LF356	High Performance JFET Input Op Amp (Wide Band)	*
LM301	High Performance Amplifier	*
LM124	General Purpose Quad Operational Amplifier	*
LM158	General Purpose Dual Operational Amplifier	*
LM224	General Purpose Quad Operational Amplifier	*
LM258	General Purpose Dual Operational Amplifier	*
LM324	General Purpose Quad Operational Amplifier	*
LM358	General Purpose Dual Operational Amplifier	*
MC1456	High Performance Operational Amplifier	*
MC1458	General Purpose Dual Operational Amplifier	70
MC1558	General Purpose Dual Operational Amplifier	70
μA709C	Operational Amplifier	*
μA740C	FET Input Operational Amplifier	*
μA741 / 741C	General Purpose Operational Amplifier	70
μA747 / 747C	Dual Operational Amplifier	*
μA748 / 748C	General Purpose Operational Amplifier	*

NOTE
*Any product listed in this section but not incorporated within the text may be obtained by writing Information Services at Signetics, 811 E. Arques, M/S 027, Sunnyvale, California 94086, or by calling (408) 746-1682.

OPERATIONAL AMPLIFIERS DEFINITIONS

T_A

Ambient temperature range. Range of the surrounding environment of the operating device.

T_J

Junction Temperature. The maximum temperature of the device. 150°C is standard for silicon devices.

T_{STG}

Storage temperature range. Temperature range that the device can be stored in a non-operating condition.

T_{SOLD}

Soldering Temperature. The temperature which can be applied to the lead frame of the device for short periods of time (normally specified for a duration of 10 sec).

Absolute Maximum Rating

Operating safe zones exceeding these limits could cause permanent damage to the device and are not meant to imply that devices can operate at these limits.

Power Dissipation

The power that the device can safely handle at 25°C. The dissipation must be derated as indicated for the individual package type.

Package Type Designation

See full package designations in Appendix.

V_{CC} $(-V_{CC})$

Supply Voltage. The range of power supply voltage over which the device will operate safely.

Acquisition Time

The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

Aperture Delay Time

The time elapsed from the hold command to the opening of the switch.

Aperture Jitter

Also called "aperture uncertainty time", it's the time variation or uncertainty with which the switch opens, or the time variation in aperature delay.

Aperture Time

The delay required between "hold" command and an input analog transition, so that the transition does not affect the hold output.

Bandwidth

The frequency at which the gain is down 3dB from its dc value. It's measured in sample (track) mode with a small-signal sine wave that doesn't exceed the slew rate limit.

Effective Aperture Delay

The time difference between the hold command and the time at which the input signal is at the held voltage.

Figure Of Merit

The ratio of the available charging current during sample mode to the leakage current during hold mode.

Hold-Mode Droop

The output voltage change per unit of time while in hold. Commonly specified in V/s, μV/μs or other convenient units.

Hold-Mode Feed Through

The percentage of an input sinusoidal signal that is measured at the output of a sample-hold when it's in hold mode.

Hold Settling Time

The time required for the output to settle within 1mV of final value after the "hold" logic command.

Sample-To-Hold Offset Error

The difference in output voltage between the time the switch starts to open, and the time when the output has settled completely. It is caused by charge being transferred to the hold capacitor switch as it opens.

Slew Rate

The fastest rate at which the sample & hold output can change (specified in V/μs).

Hold Step

The voltage step at the output of the sample and hold when switching from sample mode to hold mode with a steady (dc) analog input voltage. Logic swing is 5V.

Dynamic Sampling Error

The error introduced into the held output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

Gain Error

The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

Threshold

Level shall be defined as that level which causes the switch control to change state.

Average Input Offset Current T^O coeff.

The change in input offset current divided by the change to ambient temperature producing it.

Average Input Offset Voltage T^O coeff.

The change in input offset voltage divided by the change in ambient temperature producing it.

Common Mode Input Resistance

The resistance looking into both inputs, with inputs tied together.

Common Mode Rejection Ratio (CMRR)

The ratio of the change of input offset voltage to the input common mode voltage change producing it.

Full Power Bandwidth

The maximum frequency at which the full sinewave output might be obtained.

Input Bias Current

The average of the two input currents at zero output voltage. In some cases, the input current is measured for either input independently.

OPERATIONAL AMPLIFIERS DEFINITIONS (Cont'd)

Input Capacitance

The capacitance looking into either input terminal with the other grounded.

Input Current

The current into an input terminal.

Input Noise Voltage

The square root of the mean square narrow-band noise voltage referred to the input.

Input Offset Current

The difference in the currents into the two input terminals with the output at zero volts.

Input Offset Voltage

That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

Input Resistance

The resistance looking into either input terminal with the other grounded.

Input Voltage Range

The range of voltages on the input terminals for which the amplifier operates within specifications. In some cases, the input offset specifications apply over the input voltage range.

Large-Signal Voltage Gain

The ratio of the maximum output voltage swing to the change in input voltage required to drive the output to this voltage.

Output Resistance

The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

Output Short-Circuit Current

The maximum output current available from the amplifier with the output shorted to ground or to either supply.

Output Voltage Swing

The peak output swing, referred to zero, that can be obtained.

Power Consumption

The dc power required to operate the amplifier with the output at zero and with the output at zero and with no load current.

Power Supply Rejection Ratio

The ratio of the change in input offset voltage to the change in supply voltages producing it.

Rise Time

The time required for an output voltage step to change from 10% to 90% of its final value.

Slew Rate

The maximum rate of change of output voltage under large signal condition.

Supply Current

The current required from the power supply to operate the amplifier with no load and the output at zero.

Temperature Stability of Voltage Gain

The maximum variation of the voltage gain over the specified temperature range.

NOTE
Refer to Section 3 of the 1979 Analog Applications Manual for an in depth explanation of Operational Amplifiers and their applications

OPERATIONAL AMPLIFIERS CROSS REFERENCE

DEVICE	MANUFACTURED BY SIGNETICS		GENERAL DESCRIPTION	SIGNETICS REPLACEMENT PART	QRA	
	Yes	No			SUPR II	SURE II
LF Series	X		JFET Input Operational Amplifier			Yes
155/155A	X		JFET Input Operational Amplifier			Yes
156/156A	X		JFET Input Operational Amplifier			Yes
157/157A	X		JFET Input Operational Amplifier			Yes
255/255A	X		JFET Input Operational Amplifier			Yes
355/355A	X		JFET Input Operational Amplifier			Yes
356/356A	X		JFET Input Operational Amplifier			Yes
357/357A	X		JFET Input Operational Amplifier			Yes
LM107	X		General Purpose Operational Amplifier	SE530		Yes
LM207	X		General Purpose Operational Amplifier	SE530		Yes
LM307	X		General Purpose Operational Amplifier	NE530		Yes
MC1456	X		High Performance Operational Amplifier	NE530		Yes
MC1556	X		High Performance Operational Amplifier	SE530		Yes
MC1458	X		General Purpose Dual Operational Amplifier	NE5530		Yes
MC1558	X		General Purpose Dual Operational Amplifier	NE5530		Yes
SA1458	X		General Purpose Dual Operational Amplifier	NE5530		Yes
μA740C	X		FET Input Operational Amplifier	SU536		Yes
μA741/741A	X		General Purpose Operational Amplifier	NE530		Yes
SA741	X		General Purpose Operational Amplifier	SE530		Yes
μA747/747C	X		General Purpose Dual Operational Amplifier	NE5535		Yes
SA747C	X		General Purpose Dual Operational Amplifier	NE5535		Yes
μA748/748C	X		General Purpose Operational Amplifier	SE531		Yes
SA748C	X		General Purpose Operational Amplifier	SE531		Yes

MC1458 DUAL OPERATIONAL AMPLIFIER

COMPETITION	INDUSTRY VALUE	KEY PARAMETER	SIGNETICS AVAILABLE VALUE	SIGNETICS ORIGINATED DEVICES		QR&A		COMMENTS
						SURE II	SUPR II	
MOTOROLA FAIRCHILD RAYTHEON N.S.C. T.I.	0.5	Slew Rate	10 to 60 V/μ sec	NE/SE	5530	Yes		
					5538	Yes		
				NE	5532	Yes		
					5532A	Yes		
					5533	Yes		
					5533A	Yes		
	20	Full power out	30 to 300 kHz	NE/SE	5530	Yes		
					5538	Yes		
				NE	5532	Yes		
					5532A	Yes		
					5533			
					5533A			
	24	Noise	4 nv/√Hz	NE	5532			
					5532A			
					5533	Yes		
					5533A	Yes		
	5	Offset voltage	2 mv	NE	5532			
					5532A			
					5533	Yes		
					5533A	Yes		
	200	Bias current	1 to 60 na	NE/SE	5530	Yes		
					5538	Yes		
	1	Gain bandwidth	1.5 ↓ 15 MHz	NE/SE	5530	Yes		
					5538	Yes		
				NE	5533	Yes		
					5533A	Yes		
					5532			
					5532A			
	10,000	Maximum loading	600 OHM	NE	5533			
					5533A	Yes		
					5532	Yes		
					5532A			

SIGNETICS REPLACEMENT STANDARDS

μa741 SINGLE OPERATIONAL AMPLIFIER

COMPETITION	INDUSTRY VALUE	KEY PARAMETER	SIGNETICS AVAILABLE VALUE	SIGNETICS ORIGINATED DEVICES	QR&A		COMMENTS
					SURE II	SUPR II	
MOTOROLA FAIRCHILD RAYTHEON N.S.C. T.I.	0.5	Slew rate	10 to 800 V/μ sec	NE/SE 530	Yes		
				538	Yes		
				5534	Yes	Yes	
				5534A	Yes	Yes	*Not pin for pin replacement. See new products
				NE 5539*			
	20	Full power out	300 to 350,000 kHz	NE/SE 530	Yes		
				538	Yes		
				5534	Yes	Yes	
				5534A	Yes	Yes	*Not pin for pin replacement. See new products
				5539*			
	24	Noise	4 nv/$\sqrt{Hz}$	NE/SE 5534	Yes	Yes	
				5534A	Yes	Yes	
	5	Offset voltage	2 mv	NE/SE 5534	Yes	Yes	
				5534A	Yes	Yes	
	200	Bias current	1 to 60 na	NE/SE 530	Yes		
				538	Yes		
	1	Gain bandwidth	1.5 ↓ 2000 MHz	NE/SE 530	Yes		
				538	Yes		
				5534	Yes	Yes	
				5534A	Yes	Yes	*Not pin for pin replacement. See new products
				5539*			
	10,000	Maximum loading	600 OHM	NE/SE 5534	Yes	Yes	
				5534A	Yes	Yes	

HIGH SLEW RATE OPERATIONAL AMPLIFIER SE/NE530, SE/NE5530

SE/NE530-FE,N,H • SE/NE5530-F,H,N,N-14

DESCRIPTION

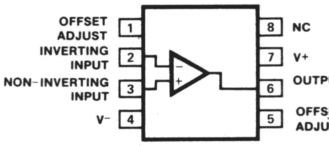
The 530/5530 are new generation operational amplifiers featuring high slew rates combined with improved input characteristics. Internally compensated, the SE530/5530 guarantee slew rates of 25V/μs with 2mV maximum offset voltage. Industry standard pinout and internal compensation allow the user to upgrade system performance by directly replacing general purpose amplifiers such as the 741, 747, 1458, 4558 and LF356 types.

FEATURES

- **Gain bandwidth product—3MHz**
- **35V/μs slew rate (Gain = -1)**
- **Internal frequency compensation**
- **Low input offset voltage 2mV max**
- **Low input bias current-60nA max**
- **Short circuit protection**
- **Offset null capability**
- **Large common mode and differential voltage ranges**

PIN CONFIGURATIONS

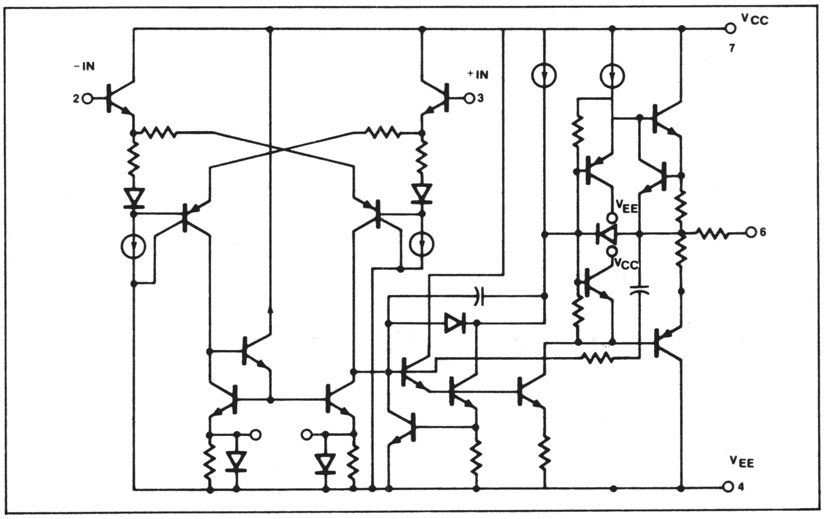
FE,N PACKAGE


OFFSET ADJUST
INVERTING INPUT
NON-INVERTING INPUT
V-
1
2
3
4
8
7
6
5
NC
V+
OUTPUT
OFFSET ADJUST

ORDER PART NO.

SE530FE, SE530N
NE530FE, NE530N

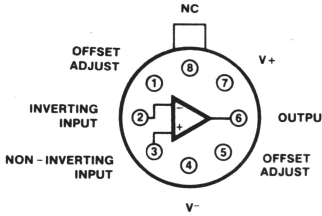
EQUIVALENT SCHEMATIC EACH AMPLIFIER


-IN
2
+IN
3
VCC
7
VEE
VCC
6
VEE
4

ABSOLUTE MAXIMUM RATINGS

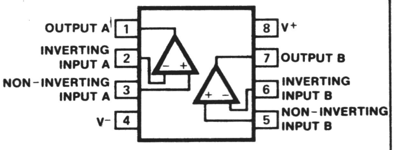
PARAMETER	RATING	UNIT
Supply voltage		
SE530/5530	±22	V
NE530/5530	±18	V
Internal power dissipation[1]		
N Package	500	mW
K/T Package	800	mW
FE, F Package	1000	mW
Differential input voltage	±30	V
Input voltage[2]	±15	V
Operating temperature range		
SE530/5530	-55 to +125	°C
NE530/5530	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature range (Solder, 60sec)	300	°C
Output short circuit[3]	Indefinite	

H PACKAGE


NC
OFFSET ADJUST
V+
INVERTING INPUT
OUTPUT
NON-INVERTING INPUT
OFFSET ADJUST
V-
1
2
3
4
5
6
7
8

ORDER PART NO.
SE530H NE530H

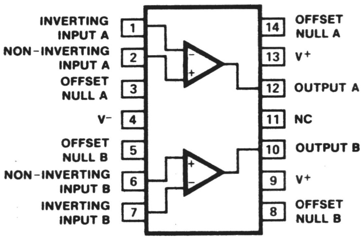
N PACKAGE


OUTPUT A
INVERTING INPUT A
NON-INVERTING INPUT A
V-
1
2
3
4
8
7
6
5
V+
OUTPUT B
INVERTING INPUT B
NON-INVERTING INPUT B

ORDER PART NO.

SE5530N
NE5530N

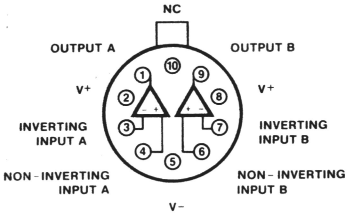
F , N-14 PACKAGE


INVERTING INPUT A
NON-INVERTING INPUT A
OFFSET NULL A
V-
OFFSET NULL B
NON-INVERTING INPUT B
INVERTING INPUT B
1
2
3
4
5
6
7
14
13
12
11
10
9
8
OFFSET NULL A
V+
OUTPUT A
NC
OUTPUT B
V+
OFFSET NULL B

ORDER PART NO.

SE5530F, SE5530N-14
NE5530F, NE5530N-14

H PACKAGE


NC
OUTPUT A
OUTPUT B
V+
V+
INVERTING INPUT A
INVERTING INPUT B
NON-INVERTING INPUT A
NON-INVERTING INPUT B
V-
1
2
3
4
5
6
7
8
9
10

ORDER PART NO.
SE5530H
NE5530H

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = \pm15V$ unless otherwise specified.[1]

PARAMETER	TEST CONDITIONS	SE530/5530			NE530/5530			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage	$R_S \leq 10k\Omega$ Over temperature		0.7	2.0 3.0		2.0	5.0 6.0	mV mV
Temperature coefficient of input offset voltage			3	15		6		µV/°C
Input offset current	 Over temperature		5	10 20		15	40 80	nA nA
Input bias current	 Over temperature		45	60 100		65	150 200	nA nA
Input resistance		3	10		1	6		MΩ
Input voltage range		±12	±13		±12	±13		V
Large signal voltage gain	$R_L \geq 2k\Omega$, $V_O = \pm10V$ Over temperature	50 25	200		50 25	200		V/mV V/mV
Output voltage swing	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V V
Output short circuit current			25			25		mA
Output resistance			100			100		Ω
Supply current	Each amplifier Over temperature		2.0 2.2	3.0 3.6		2.0 2.2	3.0	mA mA
Common mode rejection ratio	$R_S \leq 10k\Omega$ Over temperature	70	90		70	90		dB
Power supply rejection ratio	$R_S \leq 10k\Omega$ Over temperature		30	150		30	150	µV/V

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = \pm15V$ unless otherwise specified.

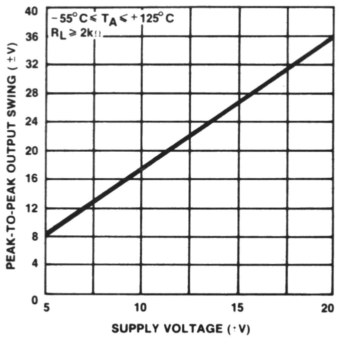
PARAMETER	TEST CONDITIONS	SE530/5530			NE530/5530			UNIT
		Min	Typ	Max	Min	Typ	Max	
Transient response								
Small signal rise time			.06			.06		µs
Small signal overshoot			13			13		%
Settling time	TO 0.1% (10V step)		0.9			0.9		µs
Slew rate	±15V supply, $V_O = \pm10V$, $R_L \geq 2k\Omega$							
Unity gain inverting		25	35		20	35		V/µs
Unity gain non-inverting		18	25		12	25		V/µs
Power bandwidth	5% THD, $V_O = \pm10V$, $R_L \geq 2k\Omega$	360	500		280	500		kHz
Small signal bandwidth	Open loop		3			3		MHz
Channel separation			120			120		dB

NOTE

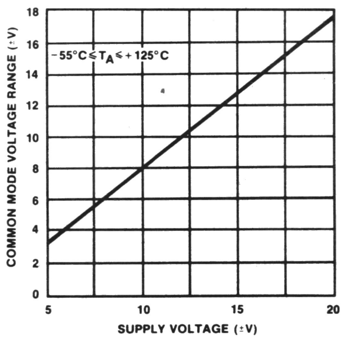
1. Operating temperature range for the SE530/5530 is -55°C to +125°C.
   Operating temperature range for the NE530/5530 is 0°C to +70°C.

TYPICAL PERFORMANCE CHARACTERISTICS

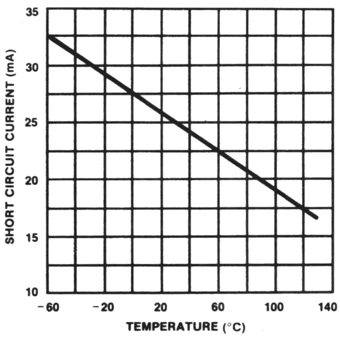
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



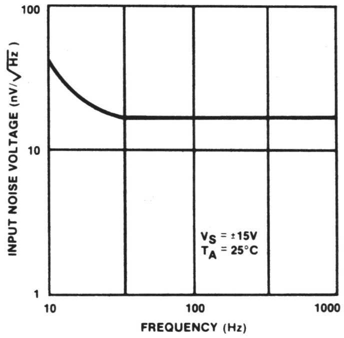
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



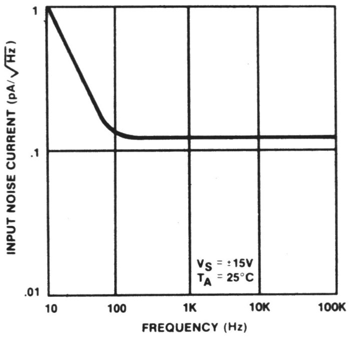
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



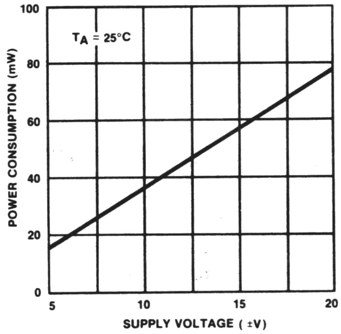
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



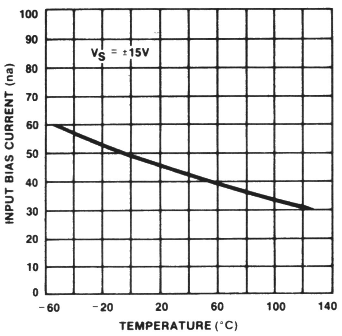
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



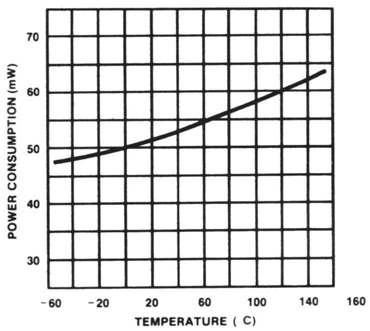
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE (EACH AMPLIFIER)



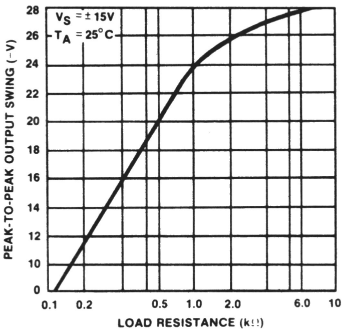
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE (EACH AMPLIFIER)

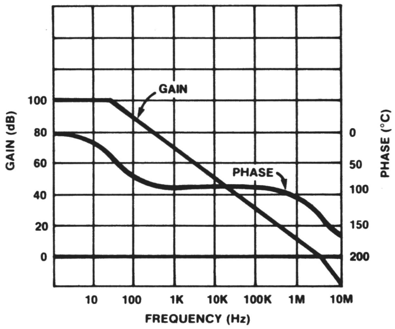


OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

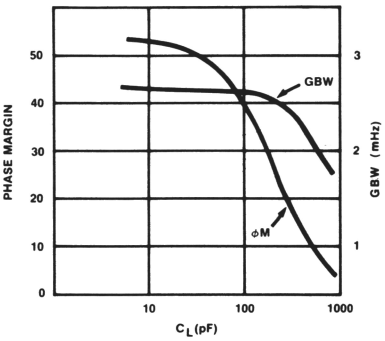


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

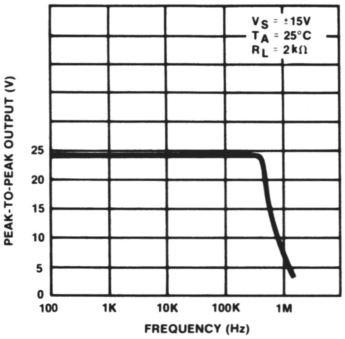
NE530 OPEN-LOOP GAIN AND PHASE vs FREQUENCY



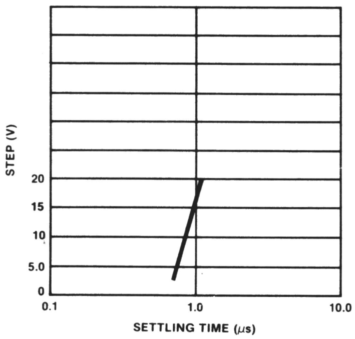
GAIN-BANDWIDTH PRODUCT AND PHASE MARGIN vs LOAD CAPACITANCE



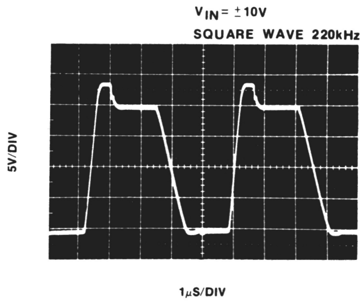
POWER BANDWIDTH



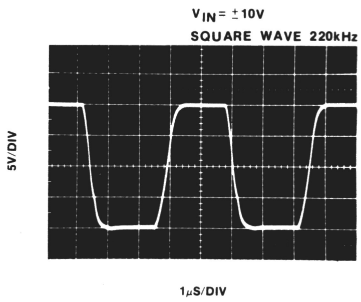
INPUT VOLTAGE STEP vs SETTLING TIME TO 10mV



SLEW RATE—VOLTAGE FOLLOWER

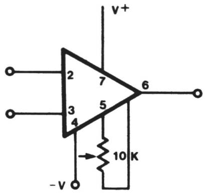


SLEW RATE (-1 AMPLIFIER)



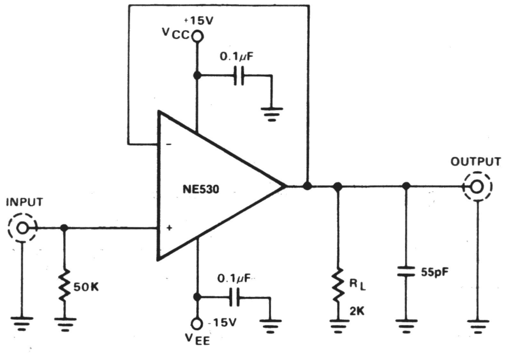
TYPICAL CIRCUIT CONNECTION

OFFSET ADJUST CIRCUIT



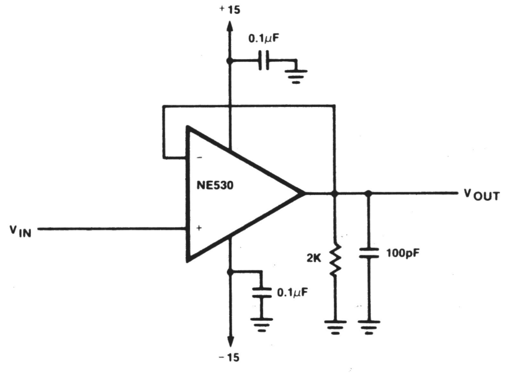
TEST LOAD CIRCUITS

SMALL SIGNAL TRANSIENT RESPONSE

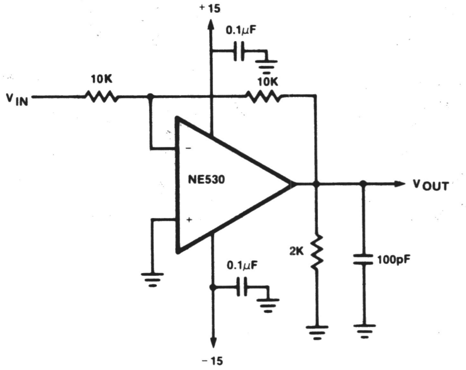

+15V
VCC
0.1μF
OUTPUT
INPUT
NE530
-
+
50K
0.1μF
-15V
VEE
RL
2K
55pF

Pins not shown are not connected.
All resistor values are typical and in ohms.

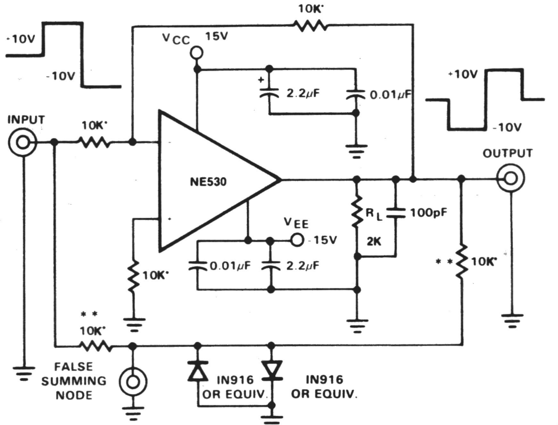
SLEW RATE—VOLTAGE FOLLOWER


+15
0.1μF
NE530
-
+
VIN
VOUT
2K
100pF
0.1μF
-15

SLEW RATE—INVERTING AMPLIFIER


+15
0.1μF
VIN
10K
10K
NE530
-
+
VOUT
0.1μF
2K
100pF
-15

SLEW RATE AND SETTLING TIME

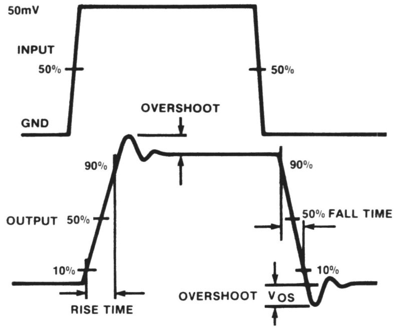

-10V
-10V
10K*
VCC 15V
2.2μF
0.01μF
+10V
-10V
INPUT
10K*
NE530
OUTPUT
RL
100pF
2K
VEE
-15V
0.01μF
2.2μF
10K*
**
10K*
**
10K*
FALSE SUMMING NODE
IN916 OR EQUIV.
IN916 OR EQUIV.

Pins not shown are not connected.
All resistor values are typical and in ohms.

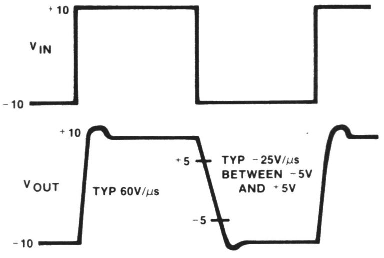
*Match to within 0.01%.
**Open for slew rate.

VOLTAGE WAVEFORMS

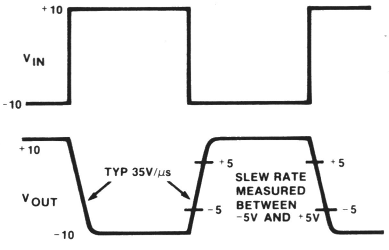
SMALL SIGNAL TRANSIENT RESPONSE DEFINITIONS


50mV
INPUT
50%
50%
GND
OVERSHOOT
90%
90%
OUTPUT 50%
50% FALL TIME
10%
10%
RISE TIME
OVERSHOOT VOS

SLEW RATE—VOLTAGE FOLLOWER


+10
VIN
-10
+10
VOUT
TYP 60V/μs
+5
TYP -25V/μs BETWEEN -5V AND +5V
-5
-10

SLEW RATE—INVERTING AMPLIFIER


+10
VIN
-10
+10
TYP 35V/μs
VOUT
-10
+5
-5
SLEW RATE MEASURED BETWEEN -5V AND +5V
+5
-5

HIGH SLEW RATE OPERATIONAL AMPLIFIER NE/SE531

NE/SE531-N,H

DESCRIPTION

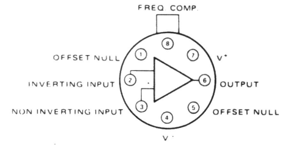
The 531 is a fast slewing high performance operational amplifier which retains dc performance equal to the best general purpose types while providing far superior large signal ac performance. A unique input stage design allows the amplifier to have a large signal response nearly identical to its small signal response. The amplifier is compensated for truly negligible overshoot with a single capacitor. In applications where fast settling and superior large signal bandwidths are required, the amplifier out performs conventional designs which have much better small signal response. Also, because the small signal response is not extended, no special precautions need be taken with circuit board layout to achieve stability. The high gain, simple compensation and excellent stability of this amplifier allow its use in a wide variety of instrumentation applications.

FEATURES

- **35V/μsec slew rate at unity gain**
- **Pin for pin replacement for μA709, μA748 or LM101**
- **Compensated with a single capacitor**
- **Same low drift offset null circuitry as μA741**
- **Small signal bandwidth 1MHz**
- **Large signal bandwidth 500KHz**
- **True op amp dc characteristics make the 531 the ideal answer to all slew rate limited operational amplifier applications.**

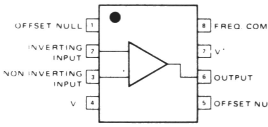
PIN CONFIGURATIONS

H PACKAGE
(Top View)


FREQ COMP
OFFSET NULL
INVERTING INPUT
NON INVERTING INPUT
V+
OUTPUT
OFFSET NULL
V-
1
2
3
4
5
6
7
8

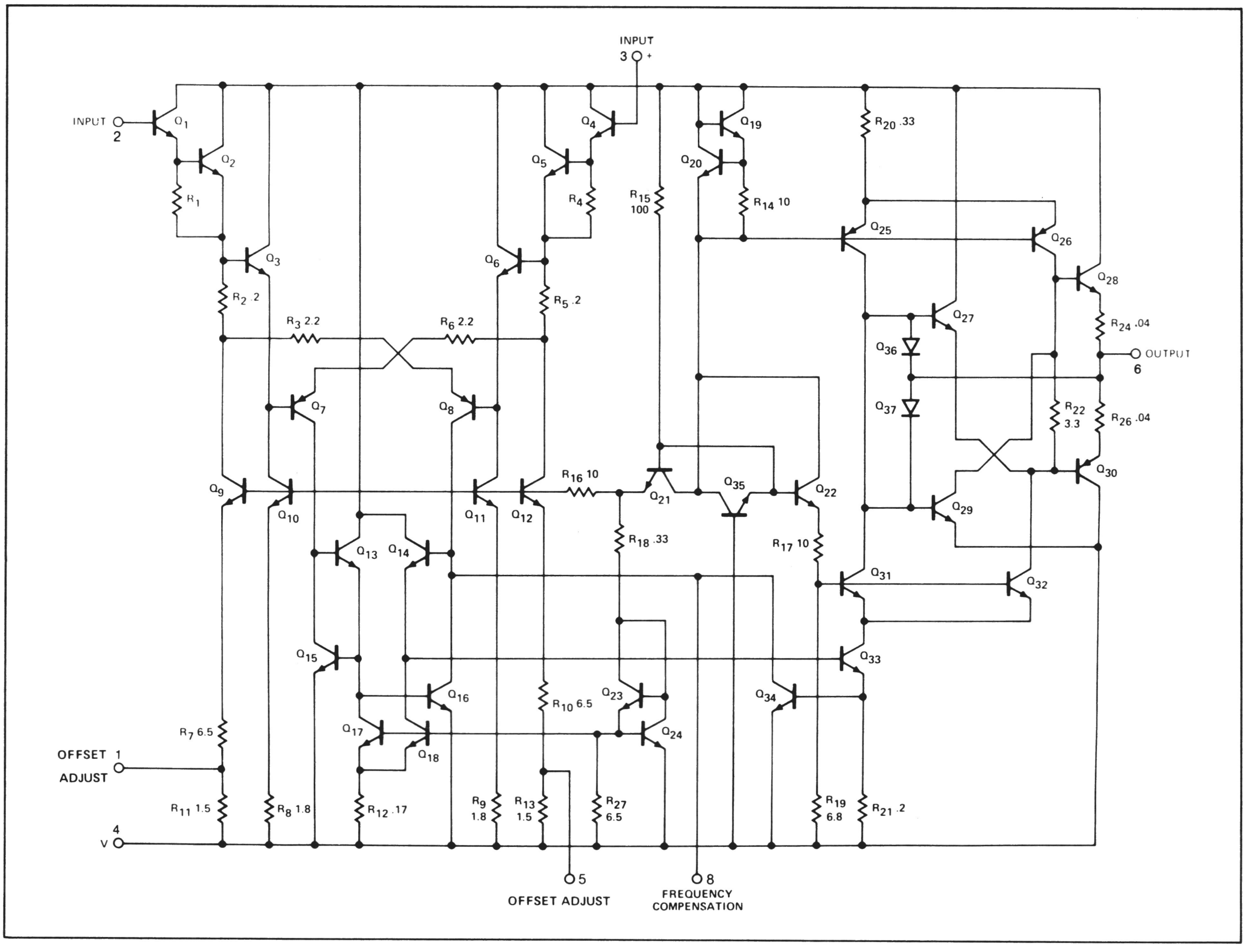
ORDER PART NO.
SE531T/NE531T

N PACKAGE


OFFSET NULL
INVERTING INPUT
NON INVERTING INPUT
V-
FREQ COMP
V+
OUTPUT
OFFSET NULL
1
2
3
4
5
6
7
8

ORDER PART NO.
NE531N

EQUIVALENT SCHEMATIC


INPUT
3 +
INPUT
2
Q1
Q2
R1
Q3
R2 .2
R3 2.2
R6 2.2
Q4
Q5
R4
Q6
R5 .2
R15 100
Q19
Q20
R14 10
R20 .33
Q25
Q26
Q28
R24 .04
OUTPUT
6
Q27
Q36
Q37
R22 3.3
R26 .04
Q30
Q29
Q7
Q8
Q9
Q10
Q11
Q12
R16 10
Q21
Q35
Q22
R18 .33
R17 10
Q13
Q14
Q31
Q32
Q15
Q33
Q16
R10 6.5
Q23
Q34
Q17
Q18
Q24
R7 6.5
OFFSET 1 ADJUST
R11 1.5
R8 1.8
R12 .17
R9 1.8
R13 1.5
R27 6.5
R19 6.8
R21 .2
4
V-
5
OFFSET ADJUST
8
FREQUENCY COMPENSATION

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	±22	V
Internal power dissipation[1]	300	mW
Differential input voltage	±15	V
Common mode input voltage[2]	±15	V
Voltage between offset null and V-	±0.5	V
Operating temperature range		
NE531	0 to +70	°C
SE531	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60 sec)	300	°C
Output short circuit duration[3]	indefinite	

NOTES

1. Rating applies for case temperature to 125°C, derate linearly at 6.5mW/°C for ambient temperatures above +75°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or to +75°C ambient temperature.

DC ELECTRICAL CHARACTERISTICS $V_S = \pm15V$ unless otherwise specified.

	PARAMETER	TEST CONDITIONS	SE531[1]			NE531			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S \leq 10k\Omega$, $T_A = 25°C$		2.0	5.0		2.0	6.0	mV
		$R_S \leq 10k\Omega$, over temp			6.0			7.5	mV
I_{OS}	Offset current	$T_A = 25°C$		30	200		50	200	nA
		T_A = HIGH			200			200	nA
		T_A = LOW			500			300	nA
I_{BIAS}	Input current	$T_A = 25°C$		300	500		400	1500	nA
		T_A = HIGH			500			1500	nA
		T_A = LOW			1500			2000	nA
V_{CM}	Common mode voltage range	$T_A = 25°C$	±10			±10			V
CMRR	Common mode rejection ratio	$T_A = 25°C$, $R_S \leq 10k\Omega$				70	100		dB
		Over temp $R_S \leq 10k\Omega$	70	90					dB
R_{IN}	Input resistance	$T_A = 25°C$		20			20		MΩ
V_{OUT}	Output voltage swing	$R_L \geq 10k\Omega$, over temp	±10	±13		±10	±13		V
I_{CC}	Supply current	$T_A = 25°C$			7.0			10	mA
		T_{MAX}			7.0			10	mA
P_D	Power consumption	$T_A = 25°C$			210			300	mW
P_{SRR}	Power supply rejection ratio	$R_S \leq 10k\Omega$, $T_A = 25°C$					10	150	μV/V
		$R_S \leq 10k\Omega$, over temp		10	150				μV/V
R_{OUT}	Output resistance	$T_A = 25°C$		75			75		Ω
A_{VOL}	Large signal voltage gain	$T_A = 25°C$, $R_L \geq 10k\Omega$, $V_{OUT} = \pm10V$	50	100		20	60		V/mV
		$R_L \geq 10k\Omega$, $V_{OUT} = \pm10V$, over temp	25			15			V/mV

NOTE

1. Temperature range:
   SE531 $-55°C \leq T_A \leq 125°C$
   NE531 $0°C \leq T_A \leq 70°C$

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

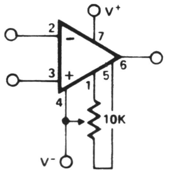
PARAMETER	TEST CONDITIONS	NE531			SE531			UNIT
		Min	Typ	Max	Min	Typ	Max	
Full power bandwidth			500			500		kHz
Settling time (1%) (.01%)	$A_V = +1$, $V_{IN} = \pm 10V$		1.5 2.5			1.5 2.5		μs μs
Large signal overshoot Small signal overshoot	$A_V = +1$, $V_{IN} = \pm 10V$ $A_V = +1$, $V_{IN} = 400mV$		2 5			2 5		% %
Small signal risetime	$A_V = +1$, $V_{IN} = 400mV$		300			300		ns
Slew rate	$A_V = 100$		35			35		V/μs
	$A_V = 10$		35			35		V/μs
	$A_V = 1$ (noninverting)		30		20	30		V/μs
	$A_V = 1$ (inverting)		35		25	35		V/μs

NOTE

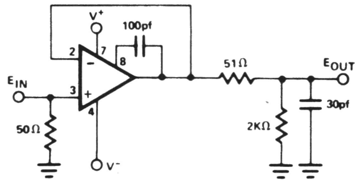
1. All AC testing is performed in the transient response test circuit.

TEST LOAD CIRCUITS

OFFSET NULL CIRCUIT

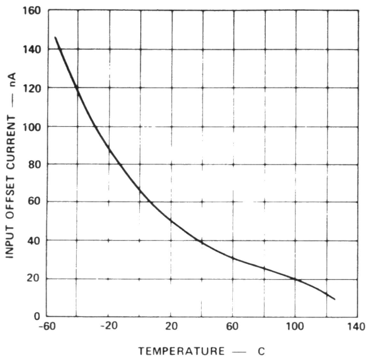


TRANSIENT RESPONSE CIRCUIT

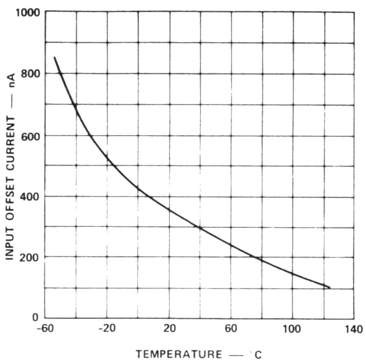


TYPICAL PERFORMANCE CHARACTERISTICS ($V_S = \pm 15V$, $T_A = +25°C$, unless otherwise specified.)

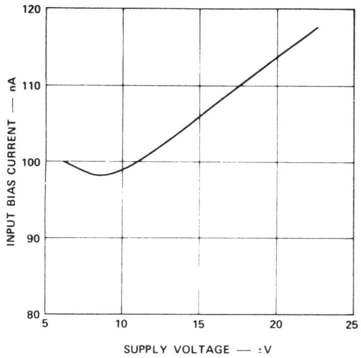
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

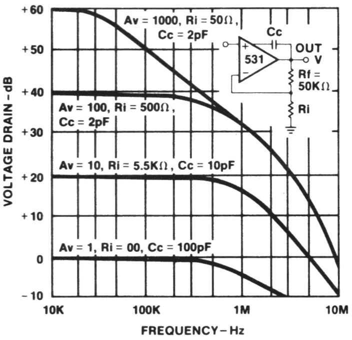


INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

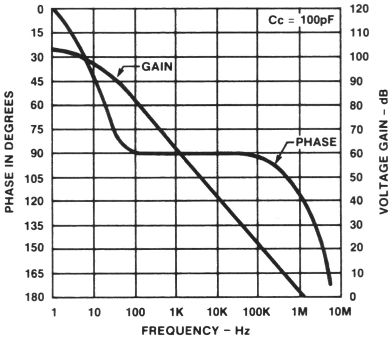


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

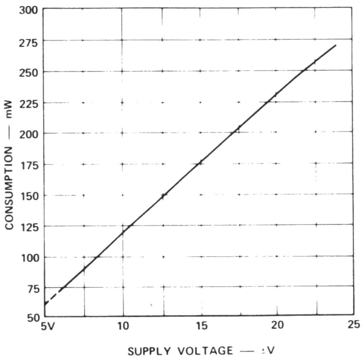
CLOSED LOOP NON-INVERTING VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



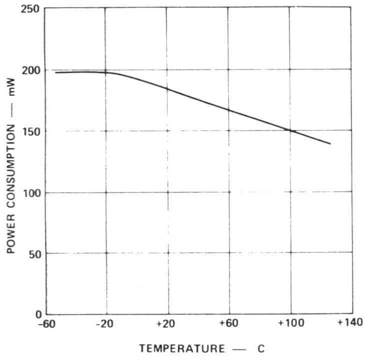
OPEN LOOP PHASE RESPONSE AND VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



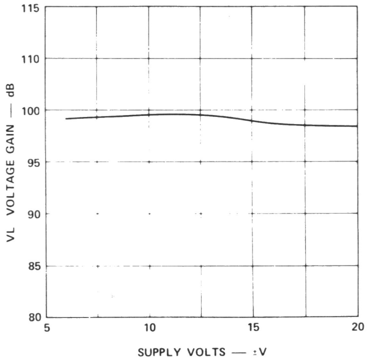
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



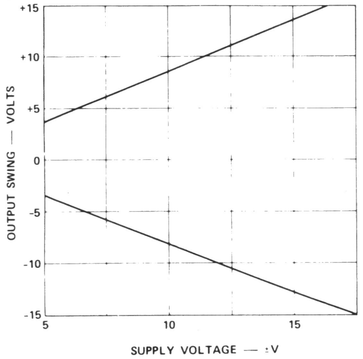
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



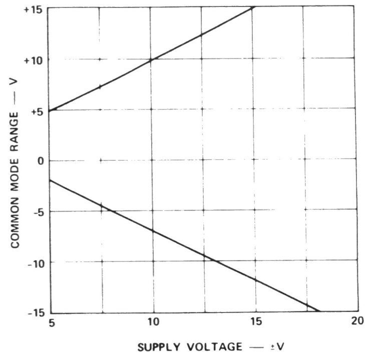
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



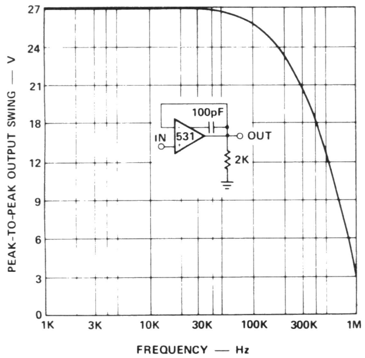
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



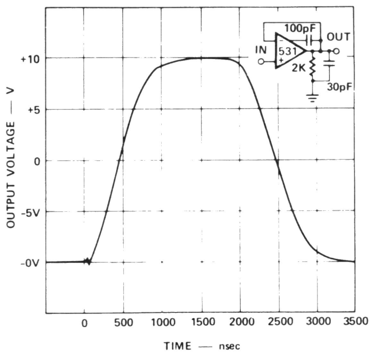
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

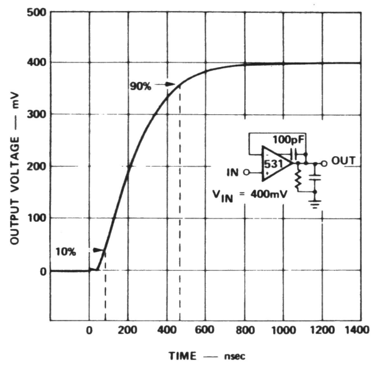


VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE

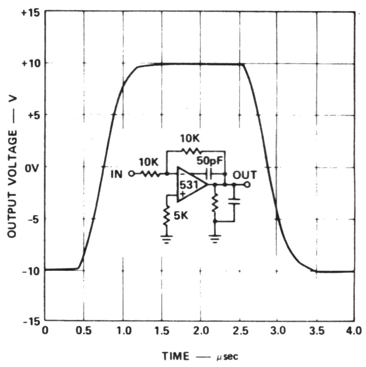


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

VOLTAGE FOLLOWER TRANSIENT RESPONSE

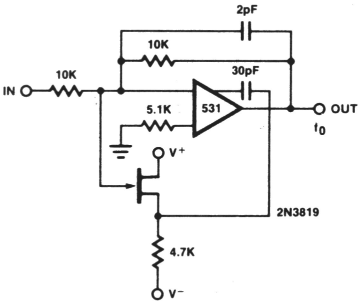


UNITY GAIN INVERTING AMPLIFIER LARGE SIGNAL RESPONSE

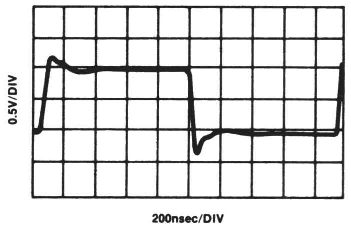


TYPICAL APPLICATIONS

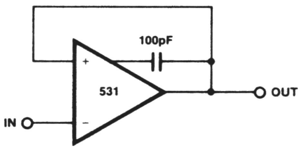
HIGH SPEED INVERTER (10MHz BANDWIDTH)


2pF
10K
10K
30pF
IN
5.1K
531
OUT
f_0
V+
2N3819
4.7K
V−

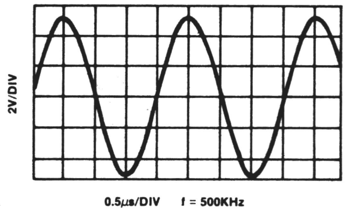
PULSE RESPONSE HIGH SPEED INVERTER



FAST SETTLING VOLTAGE FOLLOWER

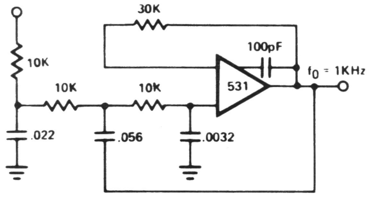

100pF
+
531
−
IN
OUT

LARGE SIGNAL RESPONSE VOLTAGE FOLLOWER

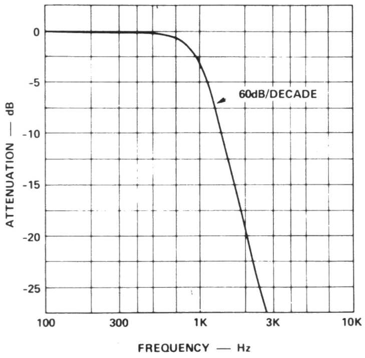


TYPICAL APPLICATIONS (Cont'd)

POLE ACTIVE LOW PASS FILTER BUTTERWORTH MAXIMALLY FLAT RESPONSE*


30K
100pF
10K
10K
10K
531
f_0 = 1KHz
.022
.056
.0032

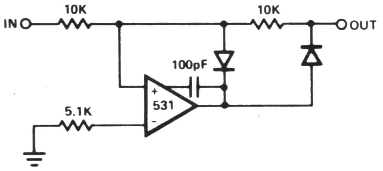
RESPONSE OF 3-POLE ACTIVE BUTTERWORTH MAXIMALLY FLAT FILTER



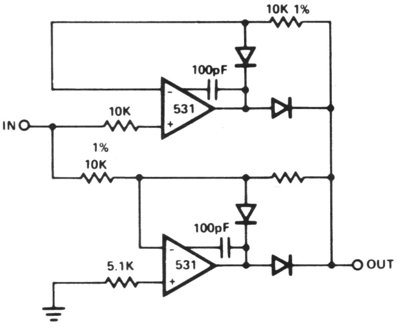
*Reference—EDN Dec. 15, 1970
Simplify 3-Pole Active Filter Design
A. Paul Brokow

PRECISION RECTIFIERS

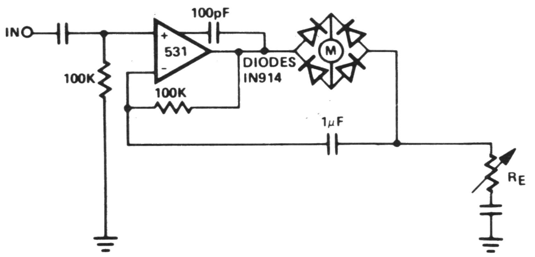
(a) HALF WAVE


IN
10K
10K
OUT
100pF
531
5.1K

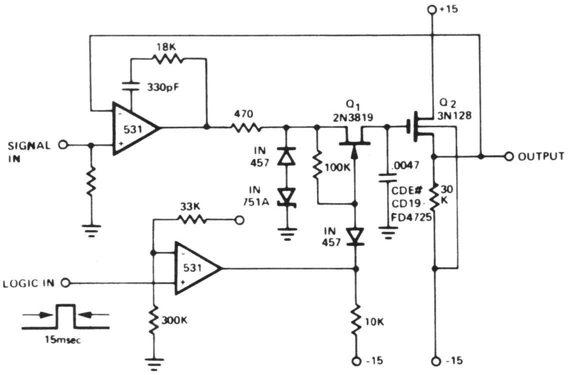
(b) FULL WAVE


10K 1%
100pF
531
10K
IN
1%
10K
100pF
531
5.1K
OUT

AC MILLIVOLTMETER


IN
100pF
531
100K
DIODES
IN914
M
100K
1μF
R_E

SAMPLE AND HOLD


+15
18K
330pF
531
470
Q_1
2N3819
Q_2
3N128
SIGNAL IN
IN 457
100K
.0047
OUTPUT
IN 751A
CDE# CD19-FD4725
30 K
33K
IN 457
531
LOGIC IN
15msec
300K
10K
-15
-15

DUAL OPERATIONAL AMPLIFIER SINGLE OR DUAL POWER SUPPLY OPERATION

NE/SE532 LM158/258/358

NE/SE532
LM158/258/358/N, H

DESCRIPTION

The 532/358 consists of two independent, high gain, internally frequency compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages. Operation from dual power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

FEATURES

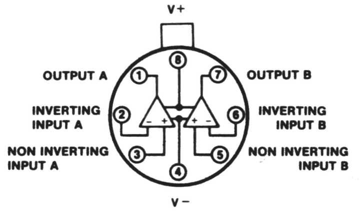
- **Internally frequency compensated for unity gain**
- **Large dc voltage gain—(100dB)**
- **Wide bandwidth (unity gain)—1MHz (temperature compensated)**
- **Wide power supply range**
  single supply—(3Vdc to 30Vdc)
  or dual supplies—(±1.5Vdc to ±15Vdc)
- **Very low supply current drain (400μA)—essentially independent of supply voltage (1mW/op amp at +5Vdc)**
- **Low input biasing current—(45nA dc temperature compensated)**
- **Low input offset voltage—(2mVdc) and offset current—(5nA dc)**
- **Differential input voltage range equal to the power supply voltage**
- **Large output voltage—(0Vdc to V+— - 1.5Vdc swing)**
- **SE532 Mil std 883A,B,C available**

UNIQUE FEATURES

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage. The unity gain cross frequency is temperature compensated. The input bias current is also temperature compensated.

PIN CONFIGURATIONS

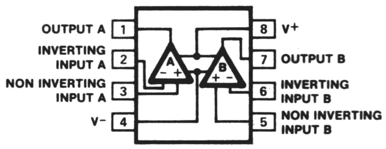
H PACKAGE
(Top View)



V+
OUTPUT A
INVERTING INPUT A
NON INVERTING INPUT A
OUTPUT B
INVERTING INPUT B
NON INVERTING INPUT B
V−
1
2
3
4
5
6
7
8

ORDER PART NO.
LM158/SE532H LM358/NE532H

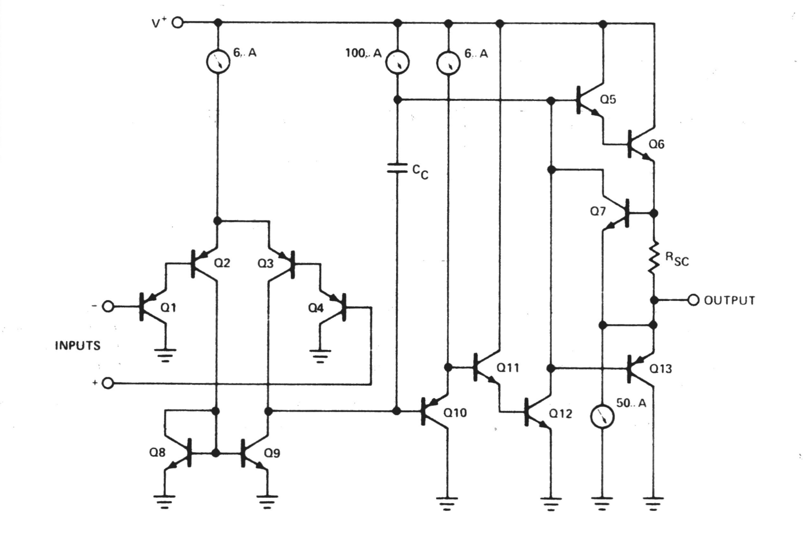
N PACKAGE
(Top View)



OUTPUT A
INVERTING INPUT A
NON INVERTING INPUT A
V−
V+
OUTPUT B
INVERTING INPUT B
NON INVERTING INPUT B
1
2
3
4
5
6
7
8
A
B

ORDER PART NO.
LM158/SE532N LM358/NE532N

EQUIVALENT CIRCUIT



V+
6μA
100μA
6μA
Q5
Q6
CC
Q7
RSC
OUTPUT
Q2
Q3
Q1
Q4
INPUTS
−
+
Q11
Q13
Q10
Q12
50μA
Q8
Q9

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage, V+	32 or ±16	Vdc
Differential input voltage	32	Vdc
Input voltage	-0.3 to +32	Vdc
Power dissipation		
T package	680	mW
N package	625	mW
Output short-circuit to GND		
V+ < 15 Vdc and T_A = 25°C	Continuous	
Operating temperature range		
NE532/LM358	0 to +70	°C
LM258	-25 to +85	°C
SE532/LM158	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 10sec)	300	°C

NE/SE532
LM158/258/358/N, H

DC ELECTRICAL CHARACTERISTICS

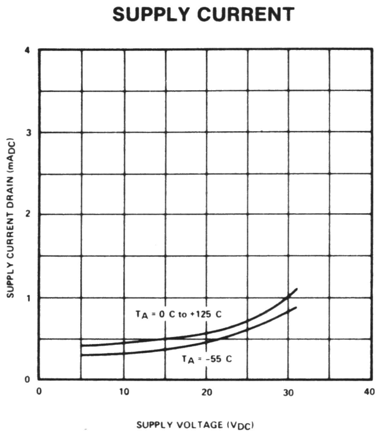
$T_A = 25°C$, $V+ = +5V$ unless otherwise specified.

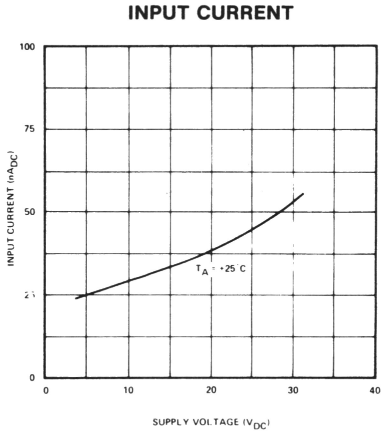
PARAMETER	TEST CONDITIONS	SE532, LM158/258			NE532/LM358			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS} Offset voltage[1]	$R_S \leq 0\Omega$		±2	±5		±2	±7	mV
	$R_S \leq 10k\Omega$, over temp.			±7			±9	mV
V_{OS} Drift	$R_S = 0\Omega$, over temp.		7			7		μV/°C
I_{OS} Offset current	$I_{IN}(+)$ or $I_{IN}(-)$		±3	±30		+5	±50	nA
I_{OS} Offset current	Over temp.			±100			±150	nA
I_{OS} Drift	Over temp.		10			10		pA/°C
I_{BIAS} Input current[2]	$I_{IN}(+)$ or $I_{IN}(-)$		45	150		45	250	nA
	Over temp., $I_{IN}(+)$ or $I_{IN}(-)$		40	300		40	500	nA
V_{CM} Common mode voltage range[3]	$V+ = 30V$	0		V+-1.5	0		V+-1.5	V
	Over temp., $V+ = 30V$			V+-2.0			V+-2.0	V
C_{MRR} Common mode rejection ratio	$R_S \leq 10k\Omega$	70	85		65	70		dB
V_{OUT} Output voltage swing (V_{OH})	$R_L \geq 2k\Omega$, $V+ = 30V$	26			26			V
	$R_L \geq 10k\Omega$, $V+ = 30V$	27	28		27	28		V
V_{OUT} Output voltage swing (V_{OL})	$R_L \leq 10k\Omega$, over temp.		5	20		5	20	mV
I_{CC} Supply current	$R_L = \infty$ on all amplifiers, over temp		0.5	1.2		0.5	1.2	mA
A_{VOL} Large signal voltage Gain	$R_L \geq 2k\Omega$, $V_{OUT} \pm 10V$, $V_S = \pm 15V$	50	100		25	100		V/mV
	Over temp.	25			15			V/mV
P_{SRR} Supply voltage rejection ratio	$R_S \leq 0\Omega$	65	100		65	100		dB
Amplifier-to-amplifier coupling[4]	f = 1kHz to 20kHz (input referred)		-120			-120		dB
Output current source	$V_{IN}+ = 1Vdc$, $V_{IN}- = 0Vdc$, $V+ = 15Vdc$	20	40		20	40		mA
Output current sink	$V_{IN}- = 1Vdc$, $V_{IN} = 0Vdc$, $V+ = 15Vdc$	10	20		10	20		mA
	$V_{IN}- = 1Vdc$, $V_{IN} = 0Vdc$; $V_{OUT} = 200mVdc$	12	50		12	50		μA
I_{SC}[5]			40	60		40	60	mA

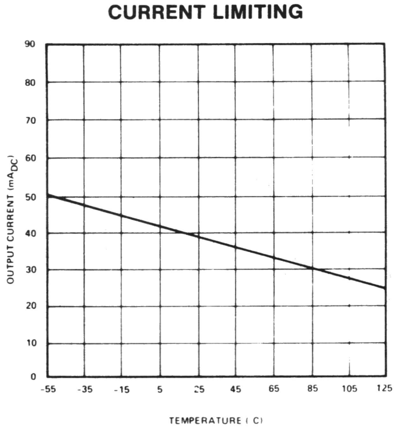
NOTES

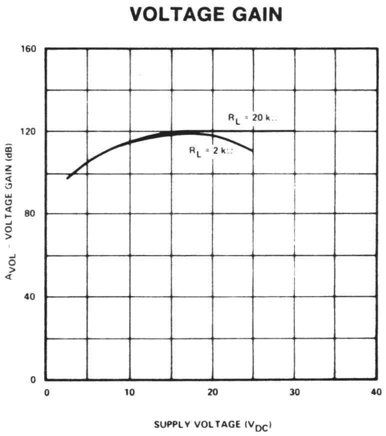
1. $V_O \cong 1.4V$, $R_S = 0\Omega$ with V+ from 5V to 30V; and over the full input common-mode range (9V to V+ -1.5V).
2. The direction of the input current is out of the IC due to the pnp input stage. This current is essentially contant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ -1.5V, but either or both inputs can go to +32V without damage.
4. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive coupling increases at higher frequencies.
5. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of +15Vdc, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.

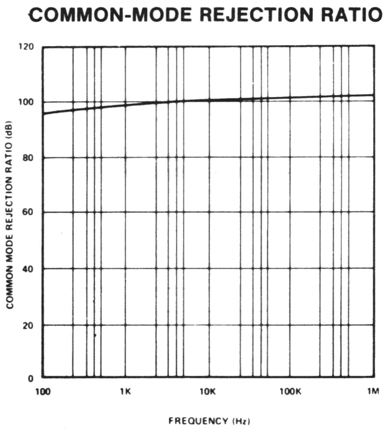
TYPICAL PERFORMANCE CHARACTERISTICS

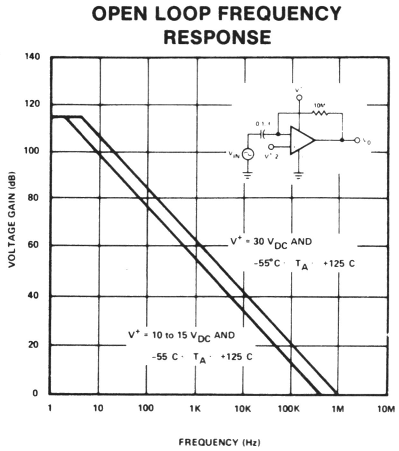

SUPPLY CURRENT

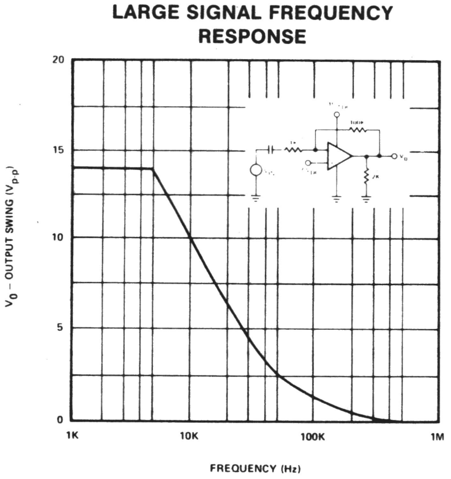

INPUT CURRENT

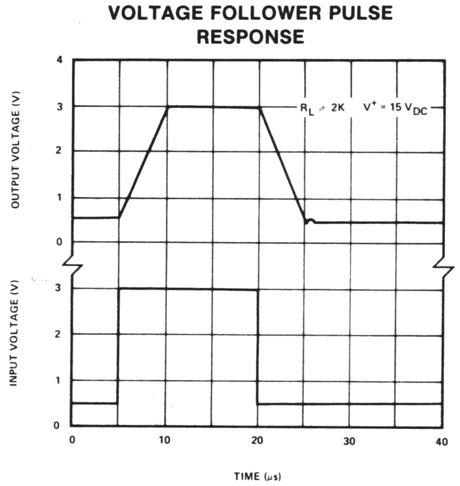

CURRENT LIMITING


VOLTAGE GAIN


COMMON-MODE REJECTION RATIO


OPEN LOOP FREQUENCY RESPONSE


LARGE SIGNAL FREQUENCY RESPONSE


VOLTAGE FOLLOWER PULSE RESPONSE

INTERNALLY COMPENSATED DUAL LOW NOISE OPERATIONAL AMPLIFIER

NE5532/5532A

NE5532/5532A-FE,H,N

DESCRIPTION

The NE5532 is a dual high-performance low noise operational amplifier. Compared to most of the standard operational amplifiers, such as the 1458, it shows better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

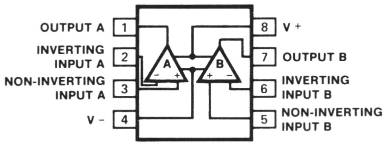
This makes the device especially suitable for application in high quality and professional audio equipment, instrumentation and control circuits, and telephone channel amplifiers. The op amp is internally compensated for gains equal to one. If very low noise is of prime importance, it is recommended that the NE5532A version be used which has guaranteed noise specifications.

FEATURES

- **Small-signal bandwidth: 10MHz**
- **Output drive capability: 600Ω, 10V (rms)**
- **Input noise voltage: 5nV/$\sqrt{Hz}$**
- **DC voltage gain: 50000**
- **AC voltage gain: 2200 at 10kHz**
- **Power bandwidth: 140kHz**
- **Slew-rate: 9V/μs**
- **Large supply voltage range: ±3 to ±20V**

PIN CONFIGURATION

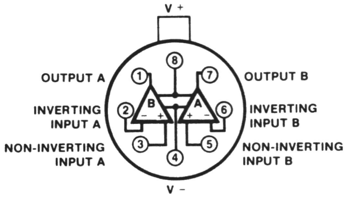
N, FE PACKAGE



OUTPUT A
INVERTING INPUT A
NON-INVERTING INPUT A
V −
1
2
3
4
A
B
8
7
6
5
V +
OUTPUT B
INVERTING INPUT B
NON-INVERTING INPUT B

ORDER PART NO.
NE5532FE,N
NE5532AFE,N

H PACKAGE

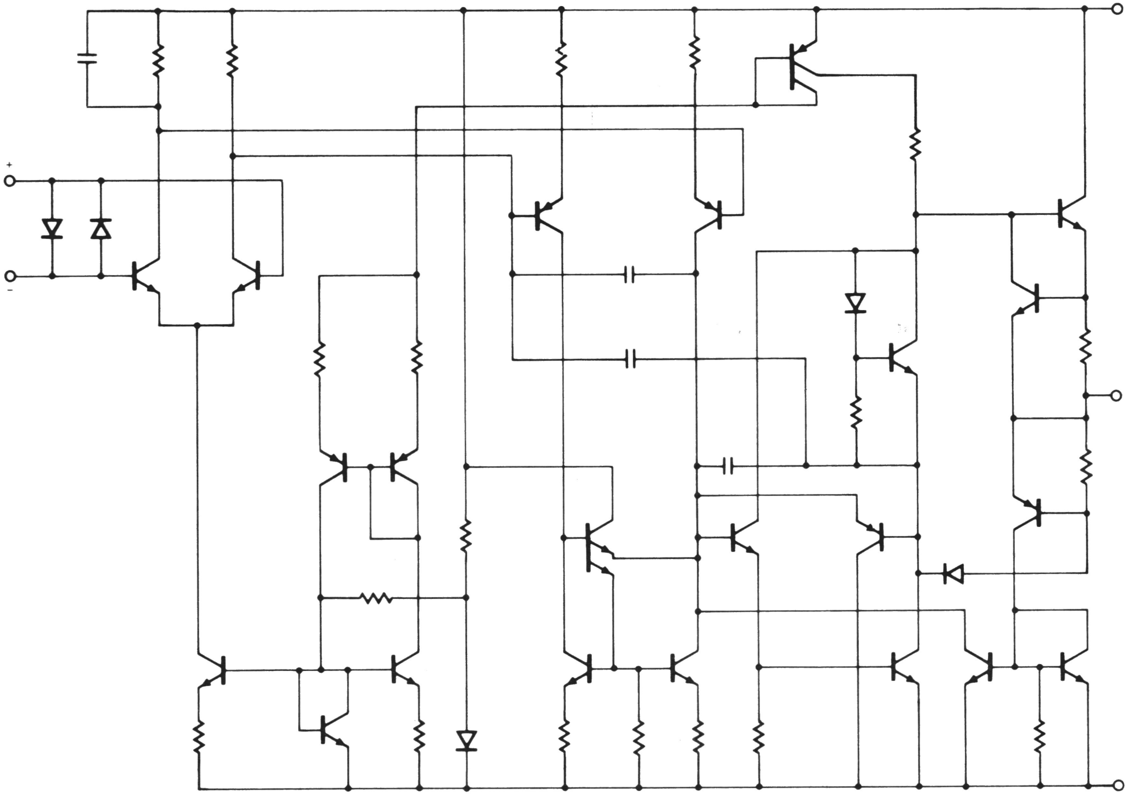


V +
OUTPUT A
INVERTING INPUT A
NON-INVERTING INPUT A
1
2
3
4
5
6
7
8
A
B
OUTPUT B
INVERTING INPUT B
NON-INVERTING INPUT B
V −

ORDER PART NO.
NE5532H
NE5532AH

EACH AMPLIFIER

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_S	Supply voltage	±22	V
V_{IN}	Input voltage	±V supply	V
V_{DIFF}	Differential input voltage[1]	±.5	V
T_A	Operating temperature range	0 to 70	°C
T_{STG}	Storage temperature	−65 to +150	°C
T_J	Junction temperature	150	°C
P_D	Power dissipation		
	5532T	800	mW
	5532FE	1000	mW
	Lead temperature (soldering, 10 sec)	300	°C

NOTES

1. Diodes protect the inputs against over-voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ± 10mA.
2. For operation at elevated temperature T package must be derated based on a thermal resistance of 150°C/W junction to ambient, 45°C/W junction to case. Thermal resistance of the FE package is 125°C/W.

DC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_S = ±15V unless otherwise specified.[1]

PARAMETER		TEST CONDITIONS	NE5532/5532A			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage			.5	4	mV
		Over temperature			5	mV
I_{OS}	Offset current			10	150	nA
		Over temperature			200	nA
I_B	Input current			200	800	nA
		Over temperature			1000	nA
I_{CC}	Supply current			8	16	mA
V_{CM}	Common mode input range		±12	±13		V
CMRR	Common mode rejection ratio		70	100		dB
PSRR	Power supply rejection ratio			10	100	µV/V
A_{VOL}	Large signal voltage gain	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	25	100		V/mV
		Over temperature	15			V/mV
		$R_L \geq 600$, $V_O = \pm 10V$	15	50		V/mV
		Over temperature	10			V/mV
V_{OUT}	Output swing	$R_L \geq 600\Omega$	±12	±13		V
		$R_L \geq 600\Omega$, $V_S = \pm 18V$	±15	±16		V
R_{IN}	Input resistance		30	300		kΩ
I_{SC}	Output short circuit current			38		mA

NOTE

1. For NE5532, NE5532A, T_{Min} = 0°C, T_{Max} = 70°C.

NE5532/5532A-FE,H,N

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

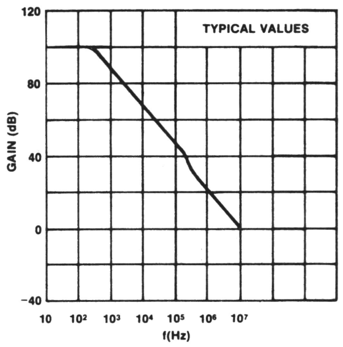
PARAMETER		TEST CONDITIONS	NE5532/5532A			UNIT
			Min	Typ	Max	
R_{OUT}	Output resistance	A_V = 30dB Closed loop f = 10kHz, R_L = 600Ω		0.3		Ω
	Overshoot	Voltage follower V_{IN} = 100mV p-p C_L = 100pF R_L = 600Ω		10		%
	Gain	f = 10kHz		2.2		v/mV
	Gain bandwidth product	C_L = 100pF R_L = 600Ω		10		mHz
	Slew rate			9		V/μs
	Power bandwidth	V_{OUT} = ±10V V_{OUT} = ±14V, R_L = 600Ω, V_{CC} = ±18V		140 100		kHz kHz

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

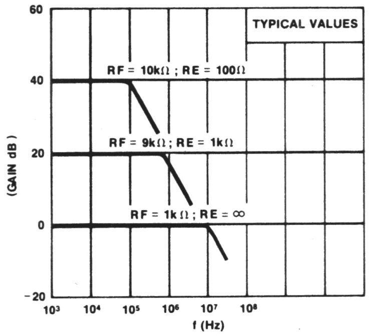
PARAMETER	TEST CONDITIONS	NE5532			NE5532A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input noise voltage	f_O = 30Hz f_O = 1kHz		8 5			8 5	10 6	nV/√Hz nV/√Hz
Input noise current	f_O = 30Hz f_O = 1kHz		2.7 0.7			2.7 0.7		pA/√Hz pA/√Hz
Channel separation	f = 1kHz, RS = 5kΩ		110			110		dB

TYPICAL PERFORMANCE CHARACTERISTICS

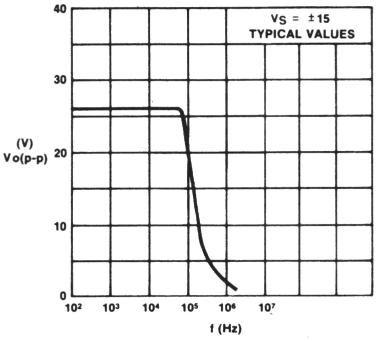
OPEN LOOP FREQUENCY RESPONSE



CLOSED LOOP FREQUENCY RESPONSE

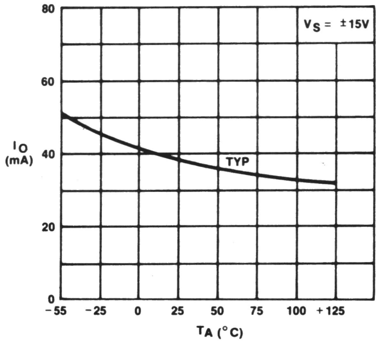


LARGE-SIGNAL FREQUENCY RESPONSE

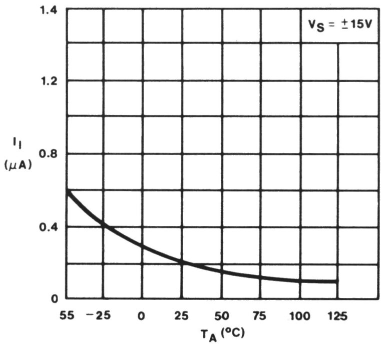


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

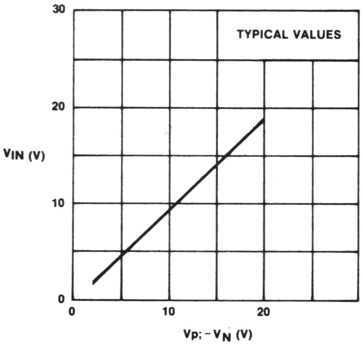
OUTPUT SHORT-CIRCUIT CURRENT



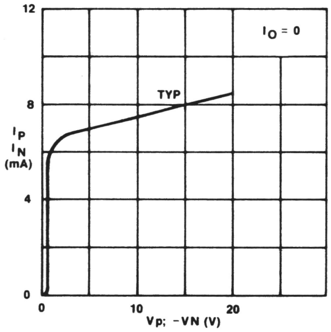
INPUT BIAS CURRENT



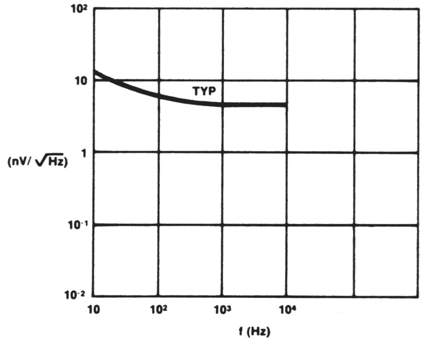
INPUT COMMON MODE VOLTAGE RANGE



SUPPLY CURRENT

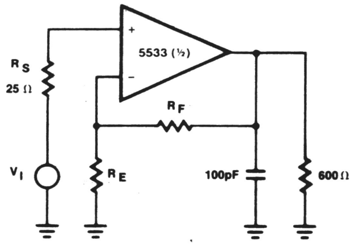


INPUT NOISE VOLTAGE DENSITY

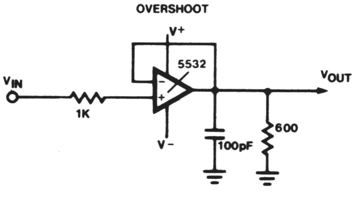


TEST CIRCUITS

CLOSED LOOP FREQUENCY RESPONSE


+
−
5533 (½)
R_S
25 Ω
R_F
V_I
R_E
100pF
600 Ω

VOLTAGE FOLLOWER


OVERSHOOT
V+
5532
−
+
V_{IN}
1K
V−
100pF
600
V_{OUT}

SINGLE AND DUAL LOW NOISE OPERATIONAL AMPLIFIER

NE/5533/5533A
NE/SE5534/5534A

NE/5533/5533A-N,F•NE/SE5534/5534A-N,H

DESCRIPTION

The 5533/5534 are single and dual high-performance low noise operational amplifiers. Compared to other operational amplifiers, such as TL083, they show better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

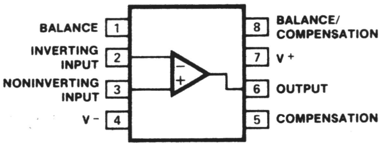
This makes the devices especially suitable for application in high quality and professional audio equipment, in instrumentation and control circuits and telephone channel amplifiers. The op amps are internally compensated for gain equal to, or higher than, three. The frequency response can be optimized with an external compensation capacitor for various applications (unity gain amplifier, capacitive load, slew-rate, low overshoot, etc.) If very low noise is of prime importance, it is recommended that the 5533A/5534A version be used which has guaranteed noise specifications.

FEATURES

- **Small-signal bandwidth: 10MHz**
- **Output drive capability: 600Ω, 10V (rms) at $V_S = \pm 18V$**
- **Input noise voltage: 4nV/$\sqrt{Hz}$**
- **DC voltage gain: 100000**
- **AC voltage gain: 6000 at 10kHz**
- **Power bandwidth: 200kHz**
- **Slew-rate: 13V/μs**
- **Large supply voltage range: ±3 to ±20V**

	5534
• Pin out	741
• Configuration	Single

N PACKAGE

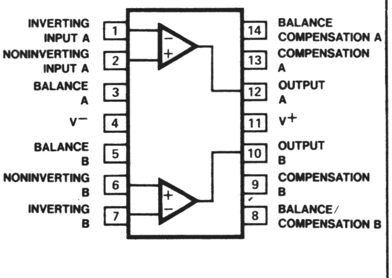

BALANCE
1
INVERTING INPUT
2
NONINVERTING INPUT
3
V-
4
8
BALANCE/ COMPENSATION
7
V+
6
OUTPUT
5
COMPENSATION
−
+

ORDER PART NO.

NE/SE5534N
NE/SE5534AN

PIN CONFIGURATION

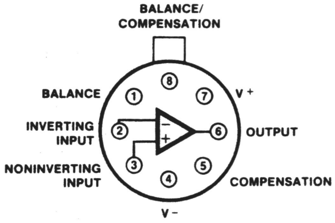
N PACKAGE


INVERTING INPUT A
1
NONINVERTING INPUT A
2
BALANCE A
3
V−
4
BALANCE B
5
NONINVERTING B
6
INVERTING B
7
14
BALANCE COMPENSATION A
13
COMPENSATION A
12
OUTPUT A
11
V+
10
OUTPUT B
9
COMPENSATION B
8
BALANCE/ COMPENSATION B
−
+
+
−

ORDER PART NO.

NE5533N/F
NE5533AN/AF

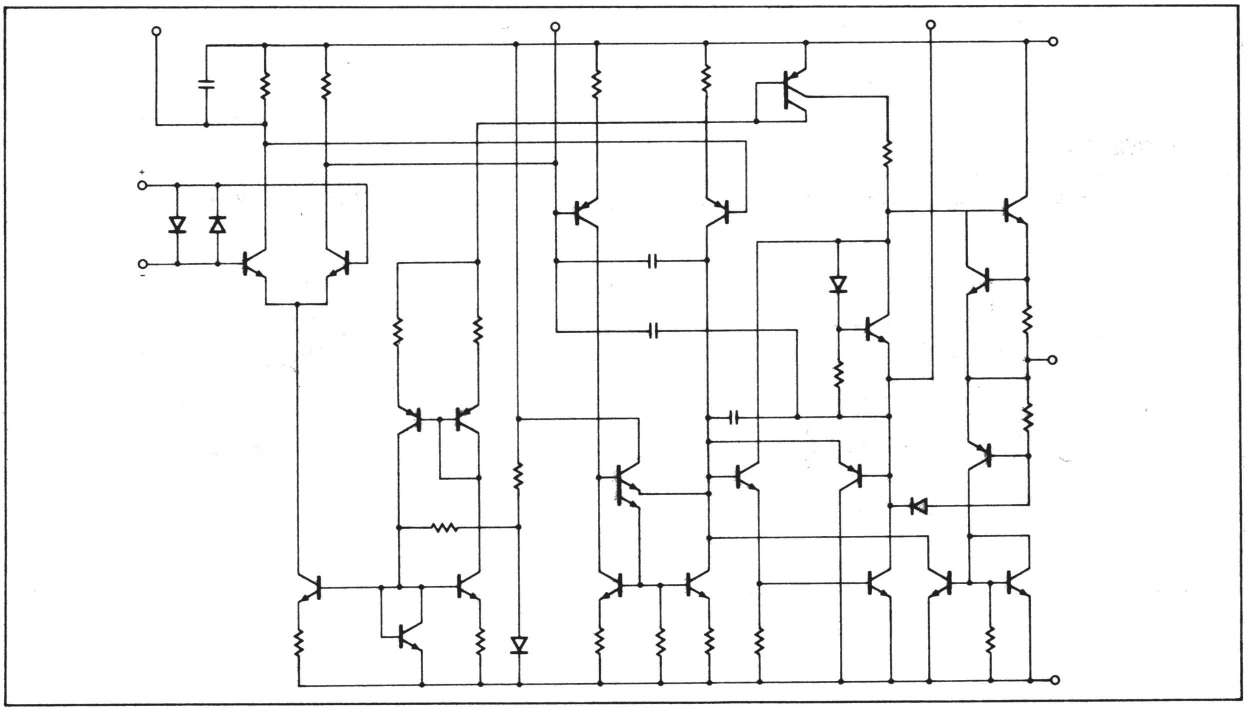
H PACKAGE


BALANCE/ COMPENSATION
BALANCE
INVERTING INPUT
NONINVERTING INPUT
V+
OUTPUT
COMPENSATION
V−
①
②
③
④
⑤
⑥
⑦
⑧
−
+

ORDER PART NO.

SE5534H
SE5534AH
NE5534H
NE5534AH

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_S	Supply voltage	±22	V
V_{IN}	Input voltage	±V supply	V
V_{DIFF}	Differential input voltage[1]	±.5	V
T_A	Operating temperature range		
	SE5534/5534A	-55 to +125	°C
	NE5533/5533A/5534/5534A	0 to 70	°C
T_{STG}	Storage temperature	-65 to +150	°C
T_J	Junction temperature	150	°C
P_D	Power dissipation at 25°C[2]		
	5533N 5534N	500	mW
	5534T	800	mW
	Output short circuit duration[3]	indefinite	
	Lead temperature (soldering 10 sec)	300	°C

NOTES

1. Diodes protect the inputs against over-voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ±10mA.
2. For operation at elevated temperature T package must be derated based on a thermal resistance of 150°C/W junction to ambient, 45°C/W junction to case. Thermal resistance of the N package is 240°C/W junction to ambient.
3. Output may be shorted to ground at $V_S = \pm 15V$, $T_A = 25°C$. Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.[1,2]

PARAMETER		TEST CONDITIONS	SE5534/5534A			NE5533/5533A 5534/5534A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage			.5	2		.5	4	mV
		Over temperature			3			5	mV
I_{OS}	Offset current			10	200		20	300	nA
		Over temperature			500			400	nA
I_B	Input current			400	800		500	1500	nA
		Over temperature			1500			2000	nA
I_{CC}	Supply current			4	6.5		4	8	mA
	Per op amp	Over temperature			9				mA
V_{CM}	Common mode input range		±12	±13		±12	±13		V
CMRR	Common mode rejection ratio		80	100		70	100		dB
PSRR	Power supply rejection ratio			10	50		10	100	$\mu V/V$
A_{VOL}	Large signal voltage gain	$R_L \geq 600\Omega$, $V_O = \pm 10V$	50	100		25	100		V/mV
		Over temperature	25			15			V/mV
V_{OUT}	Output swing	$R_L \geq 600\Omega$	±12	±13		±12	±13		V
		$R_L \geq 600\Omega$ $V_S = \pm 18V$	±15	±16		±15	±16		V
R_{IN}	Input resistance		50	100		30	100		kΩ
I_{SC}	Output short circuit current			38			38		mA

NOTES

1. For NE5533/5533A/5534/5534A, $T_{MIN} = 0°C$, $T_{MAX} = 70°C$
2. For SE 5534/5534A, $T_{MIN} = -55°C$, $T_{MAX} = +125°C$

AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = ±15V$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SE5534/5534A			NE5533/5533A 5534/5534A			UNIT
			Min	Typ	Max	Min	Typ	Max	
R_{OUT}	Output resistance	$A_V = 30dB$ closed loop $f = 10kHz, R_L = 600Ω, C_C = 22pF$		0.3			0.3		Ω
Transient response		Voltage follower, $V_{IN} = 50mV$ $R_L = 600Ω, C_C = 22pF, C_L = 100pF$							
T_R	Rise time			20			20		ns
	Overshoot			20			20		%
Transient response		$V_{IN} = 50mv, R_L = 600Ω$ $C_C = 47pF, C_L = 500pF$							
T_R	Rise time			50			50		ns
	Overshoot			35			35		%
AC	Gain	$f = 10kHz, C_C = 0$		6			6		V/mV
		$f = 10kHz, C_C = 22pF$		2.2			2.2		V/mV
	Gain bandwidth product	$C_C = 22pF, C_L = 100pF$		10			10		mHz
	Slew rate	$C_C = 0$		13			13		V/μS
		$C_C = 22pF$		6			6		V/μS
	Power bandwidth	$V_{OUT} = ±10V, C_C = 0$		200			200		kHz
		$V_{OUT} = ±10V, C_C = 22pF$		95			95		kHz
		$V_{OUT} = ±14V, R_L = 600Ω$ $C_C = 22pF, V_{CC} = ±18V$		70			70		kHz

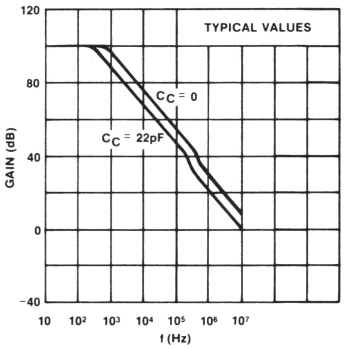
ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = ±15V$ unless otherwise specified.

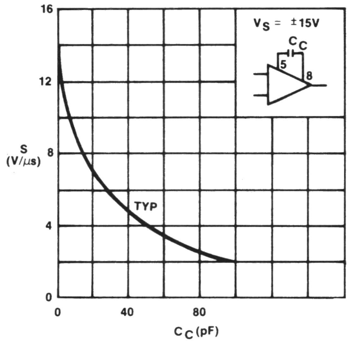
PARAMETER	TEST CONDITIONS	5533/5534			5533A/5534A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input noise voltage	$f_o = 30Hz$		7			5.5	7	$nV/\sqrt{Hz}$
	$f_o = 1kHz$		4			3.5	4.5	$nV/\sqrt{Hz}$
Input noise current	$f_o = 30Hz$		2.5			1.5		$pA/\sqrt{Hz}$
	$f_o = 1kHz$		0.6			0.4		$pA/\sqrt{Hz}$
Broadband noise figure	$f = 10Hz - 20kHz, R_S = 5kΩ$					0.9		dB
Channel separation	$f = 1kHz, R_S = 5kΩ$		110			110		dB

TYPICAL PERFORMANCE CHARACTERISTICS

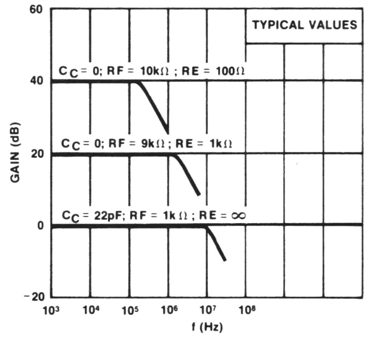
OPEN LOOP FREQUENCY RESPONSE



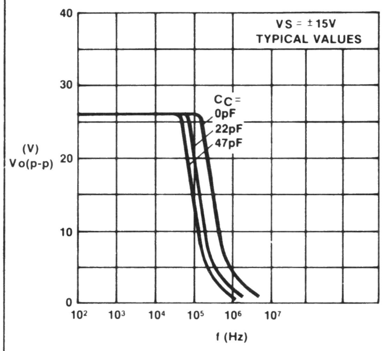
SLEW-RATE AS A FUNCTION OF COMPENSATION CAPACITANCE



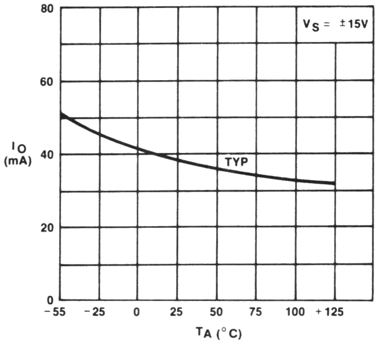
CLOSED LOOP FREQUENCY RESPONSE



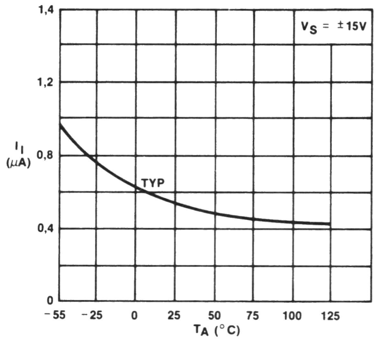
LARGE-SIGNAL FREQUENCY RESPONSE



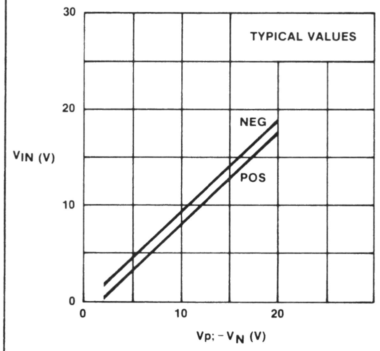
OUTPUT SHORT-CIRCUIT CURRENT



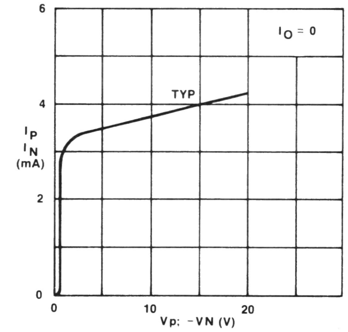
INPUT BIAS CURRENT



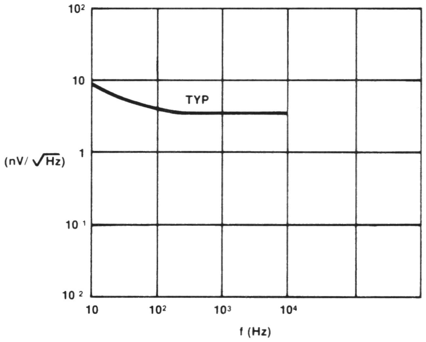
INPUT COMMON MODE VOLTAGE RANGE



SUPPLY CURRENT PER OP AMP

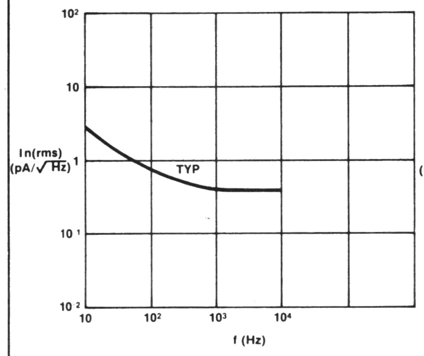


INPUT NOISE VOLTAGE DENSITY

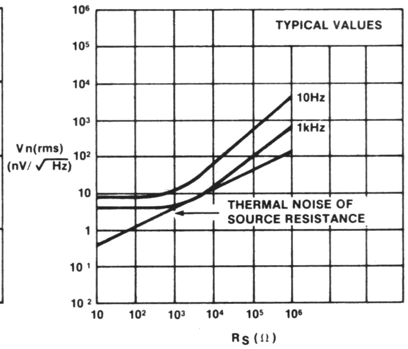


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

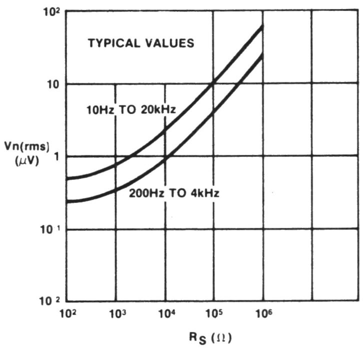
INPUT NOISE CURRENT DENSITY



TOTAL INPUT NOISE DENSITY

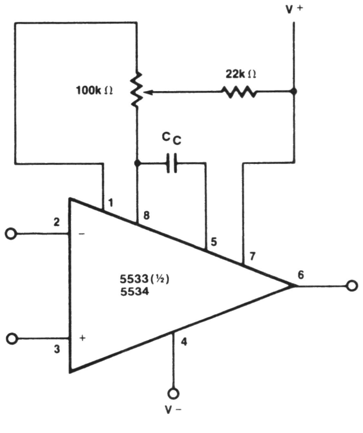


BROADBAND INPUT NOISE VOLTAGE

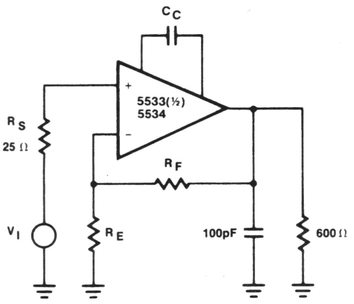


TEST LOAD CIRCUITS

FREQUENCY COMPENSATION AND OFFSET VOLTAGE ADJUSTMENT CIRCUIT


V+
100kΩ
22kΩ
C_C
1
8
5
7
2
3
6
4
−
+
5533(½)
5534
V−

CLOSED LOOP FREQUENCY RESPONSE


C_C
+
−
5533(½)
5534
R_S
25 Ω
R_F
V_I
R_E
100pF
600 Ω

FET INPUT OPERATIONAL AMPLIFIER NE/SU 536

NE/SU536-H

DESCRIPTION

The 536 is a special purpose high performance operational amplifier utilizing an FET input stage for extremely high input impedance and low input current.

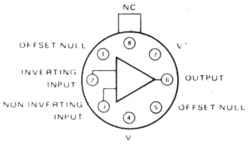
The device features internal compensation, standard pinout, wide differential and common mode input voltage range, high slew rate and high output drive capability.

FEATURES

- **5pA input bias current**
- **Input and output protection**
- **Offset null capability**
- **Internally compensated**
- **6V/µsec slew rate**
- **Standard pinout**
- **1MHz unity gain bandwidth**

PIN CONFIGURATION

H PACKAGE



ORDER PART NO.
SU536H
NE536H

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	±22	V
Differential input voltage range	±30	V
Common mode input voltage range	$\pm V_S$	
Power dissipation[1]	500	mW
Operating temperature range		
SU536T	-55 to +85	°C
NE536T	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (solder, 60sec)	300	°C
Output short circuit duration[2]	indefinite	

NOTES

1. Rating applies for case temperature to +25°C; derate linearly at 6.5mW/°C for ambient temperatures above 75°C.
2. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.[1]

PARAMETER		TEST CONDITIONS	NE536			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage	$R_S \leq 10k\Omega$		30	90	mV
		Over temp., $R_S \leq 10k\Omega$		30		mV
V_{OS}	Drift	$R_S = 0\Omega$, over temp.		30		µV/°C
I_{OS}	Offset current			5		pA
I_{BIAS}	Input current[2]			30	100	pA
V_{CM}	Common mode voltage range		±10	±11		V
CMRR	Common mode rejection ratio	$R_S \leq 10k\Omega$, $V_{IN} = \pm 10V$	64	80		dB
R_{IN}	Input resistance			10^{14}		Ω
V_{OUT}	Output voltage swing	$R_L \geq 2k\Omega$, over temp.	±10	±11		V
		R_L 10kΩ, over temp.	±12	±13		V
I_{CC}	Supply current	$V_{OUT} = OV$		6.0	8.0	mA
P_{SRR}	Supply voltage rejection ratio	$R_S \leq 10k\Omega$, $\pm 6 \leq V_S \pm 15$		100	300	µV/V
A_{VOL}	Large signal voltage gain	$V_O = \pm 10V$, R_L 2kΩ	50			V/mV
		$V_O = \pm 10V$, $R_L \geq 2k\Omega$, over temp.	25			V/mV
P_S	Power supply range		±6	±18		V

NOTES

1. Operating temperature range: NE536 is 0°C to 70°C.
2. Input current typically doubles every 10°C.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $±6V \leq V_S \leq ±20V$ unless otherwise specified.[2]

PARAMETER		TEST CONDITIONS	SU536			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage	$R_S \leq 10k\Omega$ $R_S \leq 10k\Omega$, over temp.		7.5 7.5	20 30	mV mV
V_{OS}	Drift	$R_S \leq 10k\Omega$		20		μV/°C
I_{OS}	Offset current			5		pA
I_{BIAS}	Input current[1]	 Over temp.		5 250	30 3000	pA pA
V_{CM}	Common mode voltage range	$V_S = ±15V$	±10	±11		V
CMRR	Common mode rejection ratio	$R_S \leq 10k\Omega$, $V_{IN} = ±10V$	70	80		dB
R_{IN}	Input resistance			10^{14}		Ω
V_{OUT}	Output voltage swing	$R_L \geq 2k\Omega$, $V_S = ±15V$, over temp. $R_L \geq 10k\Omega$, $V_S = ±15V$, over temp.	±10 ±12	±12 ±13		V V
I_{CC}	Supply current	$V_{OUT} = OV$, $V_S = ±20V$		6.0	8.0	mA
P_{SRR}	Supply voltage rejection ratio	$R_S \leq 10k\Omega$		50	150	μV/V
A_{VOL}	Large signal voltage gain	Over temp., $V_S = ±15V$, $V_O = ±10V$, $R_L \geq 2k\Omega$	50			V/mV
P_S	Power supply range		±6		±20	V

NOTES

1. Input current typically doubles every 10°C.
2. Operating temperature range for SU536 is -55°C to +85°C.

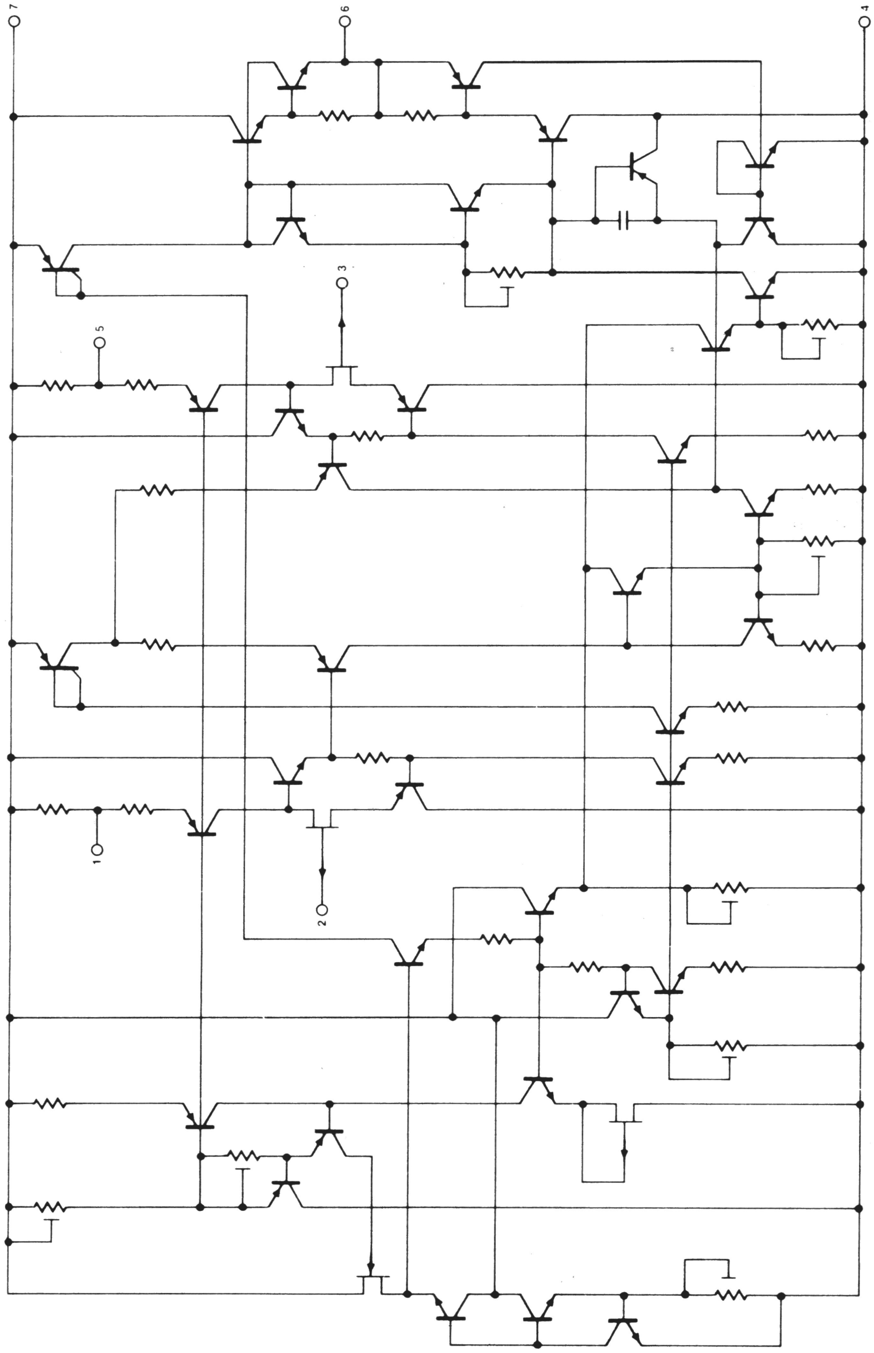
AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.[1,2]

PARAMETER	TEST CONDITIONS	NE536			SU536			UNIT
		Min	Typ	Max	Min	Typ	Max	
Differential capacitance			6			6		pF
Input noise voltage	0.1Hz — 100kHz		20			20		μVrms
Output impedance			100			100		
Unity gain frequency	$V_S = ±15V$		1			1		MHz
Full power bandwidth	$V_S = ±15V$		100			100		KHz
Slew rate, inverter	$V_S = ±15V$, $A = -1V$		6			6		V/μs
Slew rate, follower	$V_S = ±15V$, $A = +1V$		6			6		V/μs

NOTES

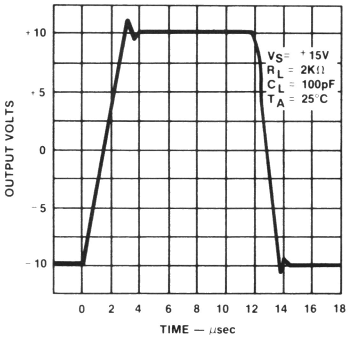
1. Temperature range for SU536 is $-55 \leq T_A \leq 85°C$
   Temperature range for NE536 is $0°C \leq T_A \leq 70°C$
2. SU536 — $±6V \leq T_A ± 20V$
   NE536 — ±15V

CIRCUIT SCHEMATIC

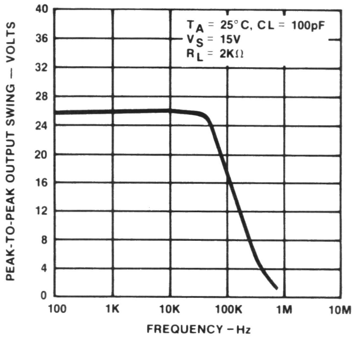


TYPICAL PERFORMANCE CHARACTERISTICS

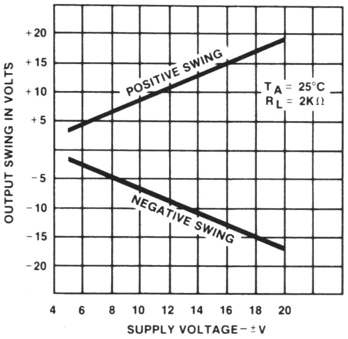
LARGE SIGNAL VOLTAGE FOLLOWER PULSE RESPONSE



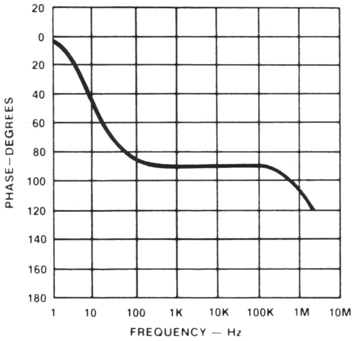
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



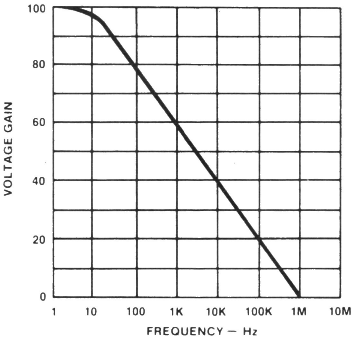
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



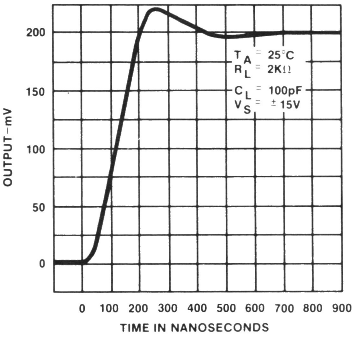
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



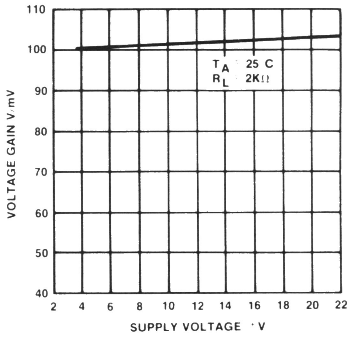
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



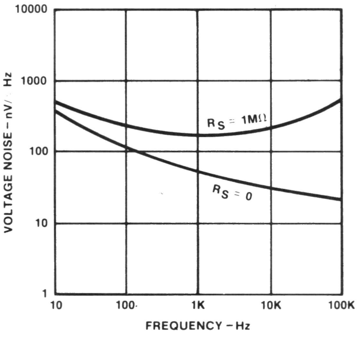
VOLTAGE FOLLOWER TRANSIENT RESPONSE



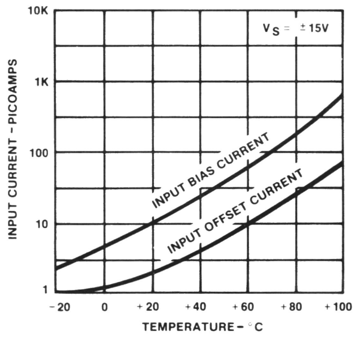
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



INPUT VOLTAGE NOISE AS A FUNCTION OF FREQUENCY

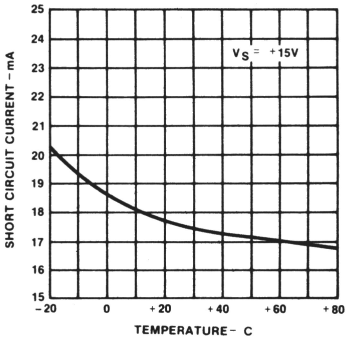


INPUT CURRENTS AS A FUNCTION OF AMBIENT TEMPERATURE



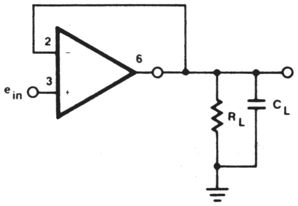
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

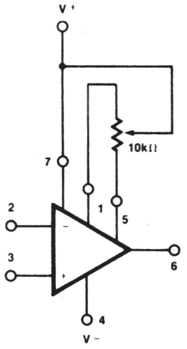


TEST CIRCUITS

VOLTAGE FOLLOWER CIRCUIT


2
3
6
e_in
R_L
C_L

OFFSET NULL CIRCUIT


V+
7
10kΩ
1
5
2
3
6
4
V–

SAMPLE AND HOLD AMPLIFIER NE/SE 5537

NE/SE 5537-H

DESCRIPTION

The NE5537 monolithic Sample and Hold amplifier combines the best features of ion implanted JFET's with bipolar devices to obtain high accuracy, fast acquisition time, and low droop rate. This device is pin compatible with the LF198, and features a superior performance in droop rate and output drive capability. The circuit shown in Figure 1 contains two operational amplifiers which function as a unity gain amplifier in the sample mode. The first amplifier has bipolar input transistors which gives the system a low offset voltage. The second amplifier has JFET input transistors to achieve low leakage current from the hold capacitor. A unique circuit design for leakage current cancellation using current mirrors gives the NE5537 a low droop rate at higher temperature. The output stage has the capability to drive a 2K load. The logic input is compatible with TTL, PMOS or CMOS logic. The differential logic threshold is 1.4V with the sample mode occurring where the logic input is high.

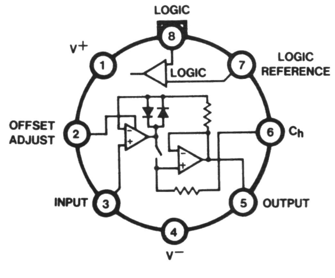
FEATURES

- **Operates from ±5V to ±18V supplies**
- **Hold leakage current 6pA @ T_j25°C**
- **Less than 10μs acquisition time**
- **TTL, PMOS, CMOS compatible logic input**
- **0.5mV typical hold step at $C_h = 0.01\mu F$**
- **Low input offset: 1MV (typical)**
- **0.002% gain accuracy with $R_L = 2k\Omega$**
- **Low output noise in hold mode**
- **Input characteristics do not change during hold mode**
- **High supply rejection ratio in sample or hold**
- **Wide bandwidth**

Logic inputs on the 5537 are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS. Differential threshold is 1.4V. The 5537 will operate from ±5V to ±18V supplies. It is available in an 8-lead TO-5 package.

PIN CONFIGURATION

H PACKAGE
Metal Can Package


LOGIC
8
V+
1
LOGIC
7
LOGIC REFERENCE
OFFSET ADJUST
2
6
Ch
INPUT
3
5
OUTPUT
4
V−

TOP VIEW

ORDER PART NO.
NE/SE 5537-H

BLOCK DIAGRAM

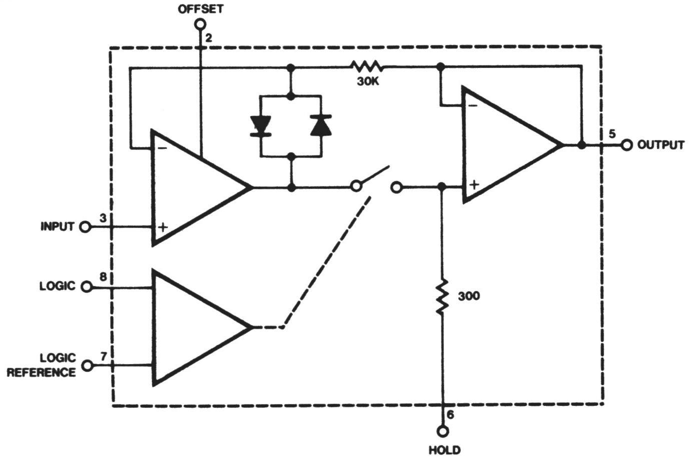

OFFSET
2
30K
5
OUTPUT
INPUT
3
LOGIC
8
LOGIC REFERENCE
7
300
6
HOLD CAPACITOR

Figure 1

TYPICAL APPLICATIONS

TYPICAL CONNECTION

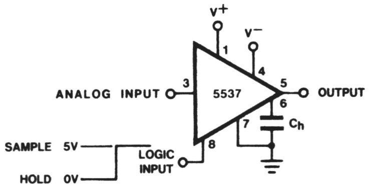

V+
1
V−
4
ANALOG INPUT
3
5537
5
OUTPUT
6
7
Ch
8
SAMPLE 5V
HOLD 0V
LOGIC INPUT

Figure 2

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	± 18	V
Power dissipation (package limitation)[1]	500	mW
Operating ambient temperature range		
SE5537	−55 to +125	°C
NE5537	0 to +70	°C
Storage temperature range	−65 to +150	°C
Input voltage	Equal to supply voltage	
Logic to logic reference differential voltage[2]	+7, −30	V
Output short circuit duration	Indefinite	
Hold capacitor short circuit duration	10	sec
Lead temperature (soldering, 10sec)	300	°C

NOTES

[1] The maximum junction temperature of the SE5537 is 150°C and for the NE5537 100°C. When operating at elevated ambient temperature, the TO-5 package must be derated based on a thermal resistance (θ_{ja}) of 150°C/W.

[2] Although the differential voltage may not exceed the limits given, the common mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

DC ELECTRICAL CHARACTERISTICS[3]

PARAMETER	TEST CONDITIONS	SE5537			NE5537			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage[6]	$T_j = 25°C$		1	3		2	7	mV
	Full temperature range			5			10	mV
Input bias current[6]	$T_j = 25°C$		5	25		10	50	nA
	Full temperature range			75			100	nA
Input impedance	$T_j = 25°C$		10^{10}			10^{10}		Ω
Gain error	$T_j = 25°C$, $-10V \leq V_{IN} \leq +10V$, RL = 2K $-11.5V \leq V_{IN} \leq +11.5V$, RL = 10K		0.002	0.007		0.004	0.01	%
	Full temperature range			0.02			0.02	%
Feedthrough attenuation ratio at 1kHz	$T_j = 25°C$, $C_h = 0.01\mu F$	86	96		80	90		dB
Output impedance	$T_j = 25°C$, "HOLD" mode		0.5	2		0.5	4	Ω
	full temperature range			4			6	
"HOLD" Step[4]	$T_j = 25°C$, $C_h = 0.01\mu F$, $V_{OUT} = 0$		0.5	2.0		1.0	2.5	mV
Supply current[6]	T_j=25°C		4.5	6.5		4.5	7.5	mA
Logic and logic reference input current	$T_j = 25°C$		2	10		2	10	μA

NOTES

[3] Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, $V_S = \pm 15V$, $T_j = 25°C$, $-11.5V$, $\pm V_{IN}$, $\pm 11.5V$, $C_h = 0.01\mu F$, and $R_L = 2k\Omega$. Logic reference voltage = 0V and logic voltage = 2.5V.

[4] Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01F hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.

[5] Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 1Φ°C increase in chip temperature. Leakage is guaranteed over full input signal range.

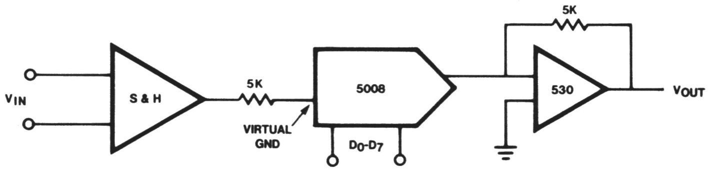
[6] These parameters guaranteed over a supply voltage range of ±5 to ±18V.

DC ELECTRICAL CHARACTERISTICS[3] (Cont'd)

PARAMETER	TEST CONDITIONS	SE5537			NE5537			UNIT
		Min	Typ	Max	Min	Typ	Max	
Leakage current into hold capacitor[6]	$T_j = 25°C$ hold mode[5]		6	50		6	100	pA
Acquisition time to 0.1%	$V_{OUT} = 10V$, $C_h = 1000pF$ $C_h = 0.01\mu f$		 4 20			 4 20		 µs µs
Hold capacitor charging current	$V_{IN} - V_{OUT} = 2V$		5			5		mA
Supply voltage rejection ratio	$V_{OUT} = 0$	80	110		80	110		dB
Differential logic threshold	$T_j = 25°C$	0.8	1.4	2.4	0.8	1.4	2.4	V

TYPICAL APPLICATIONS

MULTIPLYING DAC APPLICATION


VIN
S & H
5K
VIRTUAL GND
5008
D0-D7
5K
530
VOUT

$$V_{OUT} = V_{IN} \times \frac{1}{256} \left\{ 2^0 D_0 + 2^1 D_1 + \ldots 2^7 D_7 \right\} \quad \text{EQUATION 1}$$

Figure 3

ANALOG DATA MULTIPLEXING

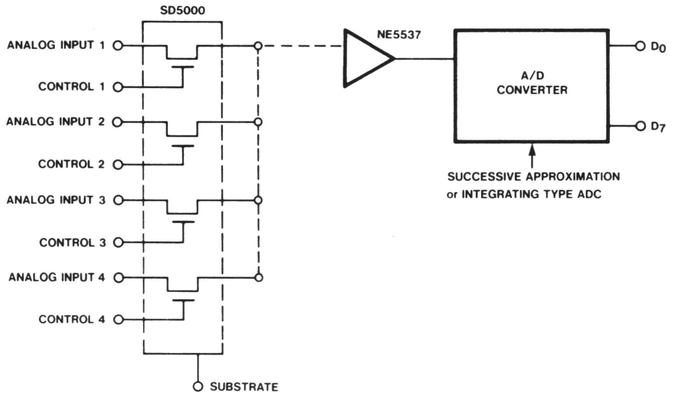
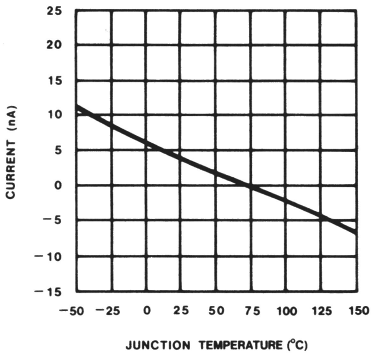

SD5000
ANALOG INPUT 1
CONTROL 1
ANALOG INPUT 2
CONTROL 2
ANALOG INPUT 3
CONTROL 3
ANALOG INPUT 4
CONTROL 4
SUBSTRATE
NE5537
A/D CONVERTER
D0
D7
SUCCESSIVE APPROXIMATION or INTEGRATING TYPE ADC

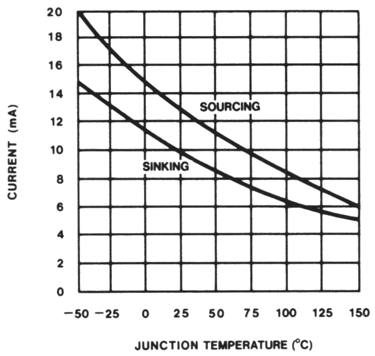
Figure 4

TYPICAL AC PERFORMANCE CHARACTERISTICS

INPUT BIAS CURRENT

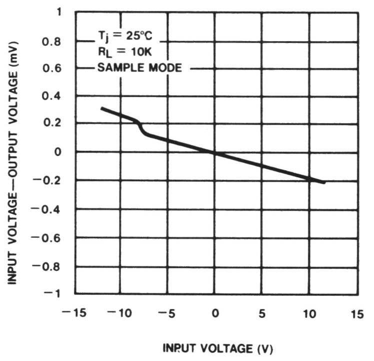


OUTPUT SHORT CIRCUIT CURRENT

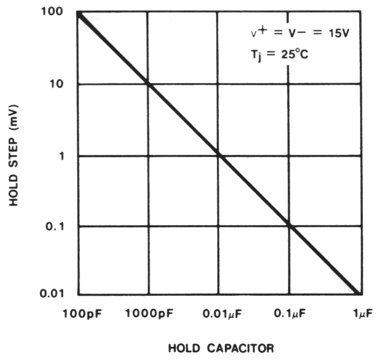


TYPICAL DC PERFORMANCE CHARACTERISTICS (Cont'd)

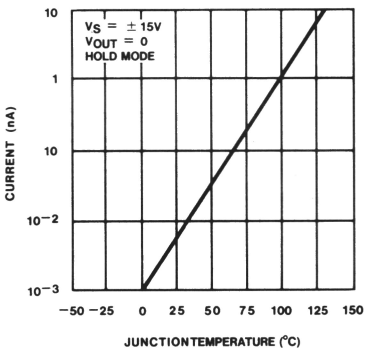
GAIN ERROR



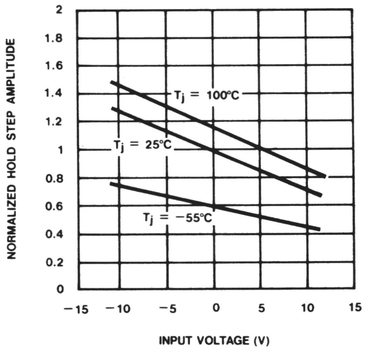
HOLD STEP



LEAKAGE CURRENT INTO HOLD CAPACITOR

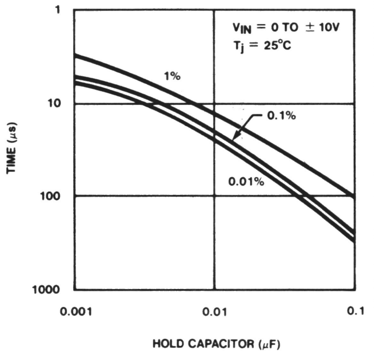


HOLD STEP vs INPUT VOLTAGE

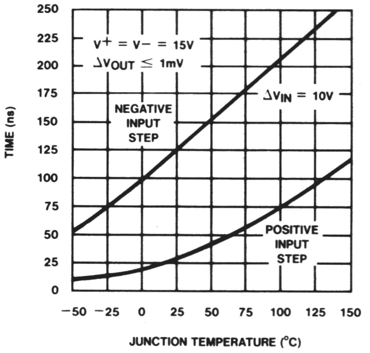


TYPICAL AC PERFORMANCE CHARACTERISTICS

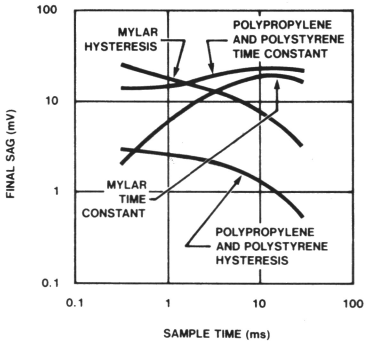
ACQUISITION TIME



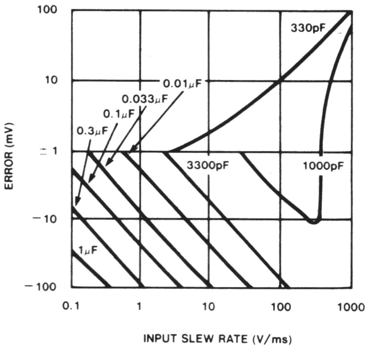
APERTURE TIME



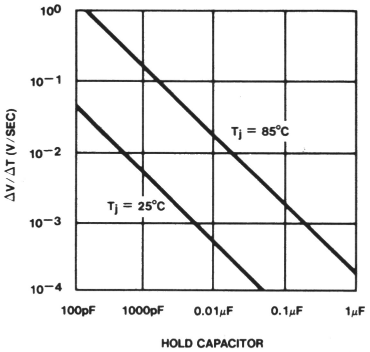
CAPACITOR HYSTERESIS



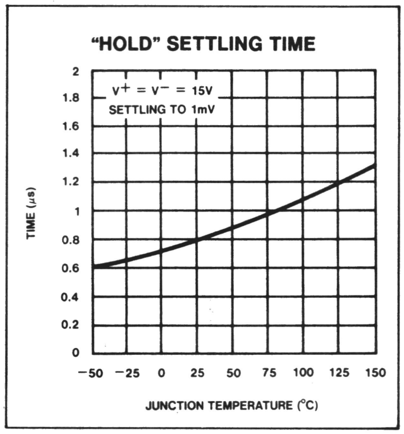
DYNAMIC SAMPLING ERROR

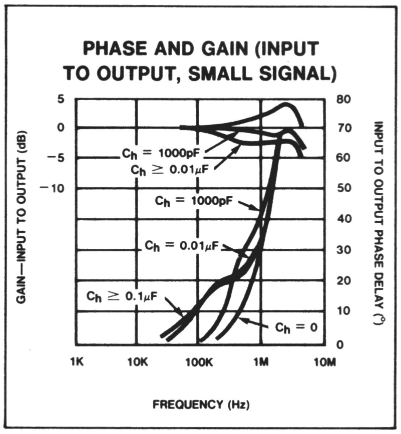


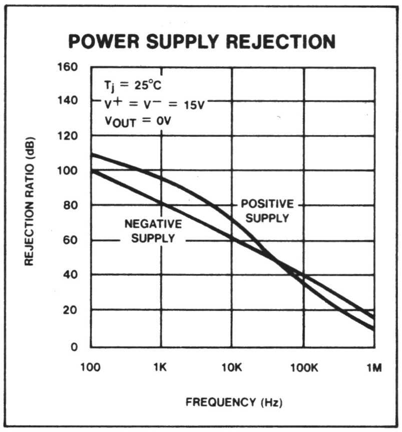
OUTPUT DROOP RATE

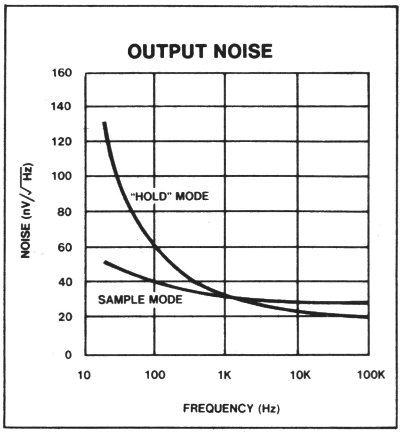


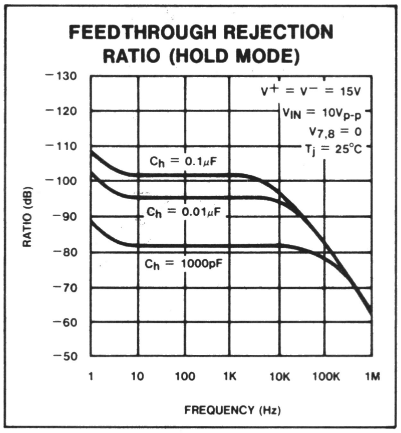
TYPICAL AC PERFORMANCE CHARACTERISTICS (Cont'd)


"HOLD" SETTLING TIME


PHASE AND GAIN (INPUT TO OUTPUT, SMALL SIGNAL)


POWER SUPPLY REJECTION


OUTPUT NOISE


FEEDTHROUGH REJECTION RATIO (HOLD MODE)

SAMPLE AND HOLD

INTRODUCTION

For many years designers have used the sample and hold (or track and hold) to operate on analog information in a time frame which is expedient.

By sampling a segment of the information and holding it until the proper timing for converting to some form of control signal or readout allows the designer certain freedom in performing predetermined manipulative functions. Therefore, the sample and hold can be defined as a "selective analog memory cell".

The memory is volatile and will also decay with time.

When using the sample and hold method for evaluating signal information, the designer is given the added feature of eliminating outside noise elements. With the analog to digital converter products available today the "dc memory" of the sample and hold can be easily converted to digital format and further incorporated into microprocessor based systems.

Parametric evaluation of the sample and hold will be discussed in the following paragraphs.

DEFINITION OF TERMS

ACQUISITION TIME: The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

APERTURE DELAY TIME: The time elapsed from the hold command to the opening of the switch.

APERTURE JITTER: Also called "aperture uncertainty time", it's the time variation or uncertainty with which the switch opens, or the time variation in aperture delay.

APERTURE TIME: The delay required between "hold" command and an input analog transition, so that the transition does not affect the held output.

BANDWIDTH: The frequency at which the gain is down 3dB from its dc value. It's measured in sample (track) mode with a small-signal sine wave that doesn't exceed the slew rate limit.

EFFECTIVE APERTURE DELAY: The time difference between the hold command and the time at which the input signal is at the held voltage.

FIGURE OF MERIT: The ratio of the available charging current during sample mode to the leakage current during hold mode.

HOLD-MODE DROOP: The output voltage change per unit of time while in hold. Commonly specified in V/s, μV/μs or other convenient units.

HOLD-MODE FEEDTHROUGH: The percentage of an input sinusoidal signal that is measured at the output of a sample-hold when it's in hold mode.

HOLD SETTLING TIME: The time required for the output to settle within 1mV of final value after the "hold" logic command.

SAMPLE-TO-HOLD OFFSET ERROR: The difference in output voltage between the time the switch starts to open, and the time when the output has settled completely. It is caused by charge being transferred to the hold capacitor switch as it opens.

SLEW RATE: The fastest rate at which the sample & hold output can change (specified in V/μs).

HOLD STEP: The voltage step at the output of the sample and hold when switching from sample mode to hold mode with a steady (dc) analog input voltage. Logic swing is 5V.

DYNAMIC SAMPLING ERROR: The error introduced into the held output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

GAIN ERROR: The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

THRESHOLD: Level shall be defined as that level which causes the switch control to change state.

BASIC BLOCK DIAGRAM

The basic circuit concept of the sample and hold circuit incorporates the use of two (2) operational amplifiers and a switch control mechanism (which determines sample, hold or track conditions). Reference figure 1.

The block diagram of the NE5537 is a closed loop non-inverting unity gain sample and hold system. The input buffer amplifier supplies the current necessary to charge the hold capacitor, while the output buffer amplifier closes the loop such that the output voltage is identical to the input voltage (with consideration for input offset voltage, offset current, and temperature variations which are common to *all* sample and hold circuits, be they monolithic, hybrid or modular).

When the sampling switch is open (in the hold mode) the clamping diodes close the loop around the input amplifier to keep it from being overdriven into saturation.

The switch control is driven by external logic levels via a timing sequence remote from the sample and hold device. Reference figure 2. The switch control has a floating reference (pin 7), referred to as the logic reference which makes the sample and hold device compatible to several types of external logic signals (TTL, PMOS, & CMOS). The switching device operates at a threshold level of 1.4V.

The switch mechanism is on (sampling an information stream) when the logic level is high (pin 8 is 1.4 volts higher than pin 7) and presents a load of 5 microamperes to the input logic signal. The analog sampled signal is amplified, stored (in the external holding capacitor), and buffered. At the end of the sampling period the internal switch mechanism turns off (switch opens) and the "stored analog memory" information on the external capacitor (pin 6) is loaded down by an operational amplifier connected in the unity gain non-inverting configuration. This amplifier, whose input impedance is effective by:

$$R = R_{IN}(A_{OL})/(1 + 1/A)$$

where R = Effective input impedance
R_{IN} = Open loop input impedance
A_{OL} = Open loop gain
A = AC loop gain

Therefore, the higher the open loop gain of the second operational amplifier, the larger the effective loading on the capacitor. The larger the load, the lower the "leakage" current and the better the droop characteristics.

In actuality the amplifiers are designed with special leakage current cancellation circuits along with FET input devices. The leakage current cancellation circuits give better high temperature operation (remember that the FET amplifiers double in required bias current for every 10 degree increase in junction temperature).

Sampling time for the NE5537 is less than 10μsec, (measured to 0.1% of input signal). Leakage current is 6pa at a rate output load of 2kΩ.

BASIC APPLICATIONS

Multiplying DAC

As depicted in the block diagram of figure 3, the sample and hold circuit is used to supply a "variable" reference to the digital to analog converter. As the input reference varies, the output will change in accordance with equation 1.

Varying the input signal reference level can aid the system in performing both compression and expansion operations. The multiplying DAC's used are the Signetics SE / NE 5008; however, if the rate of change of the reference variation is kept slow enough a microprocessor compatible DAC can be incorporated.

DATA ACQUISITION SYSTEMS

As mentioned earlier, the designer may wish to operate on several different segments of an "analog" signal; however he is limited by the fact that only one analog to digital converter channel is available to him. Figure 4 shows the means by which a multiplexing system may be accomplished.

APPLICATION HINTS

Hold Capacitor

A significant source of error in an accurate sample and hold circuit is dielectric absorption in the hold capacitor. A mylar cap, for instance, may "sag back" up to 0.2% after a quick change in voltage. A long "soak" time is required before the circuit can be put back into the hold mode with this type of capacitor. Dielectrics with very low hysteresis are polystyrene, polypropylene, and Teflon. Other types such as mica and polycarbonate are not nearly as good. Ceramic is unusable with >1% hysteresis. The advantage of polypropylene over polystyrene is that it extends the maximum ambient temperature from 85°C to 100°C. The hysteresis relaxation time constant in polystyrene, for instance, is 10-50ms. If A-to-D conversion can be made within 1ms, hysteresis error will be reduced by a factor of ten.

DC Zeroing

dc Zeroing is accomplished by connecting the offset adjust pin to the wiper of a 1Ωk potentiometer which has one end tied to V^+ and the other end tied through a resistor to ground. The resistor should be selected to give ≃0.6mA through the 1K potentiometer.

Sampling Dynamic Signals

Sampling errors due to moving (changing) input signals are of significant concern to designers employing sample and hold circuits. There exist finite phase delays through the sample and hold circuit causing an input-output phase differential for / as moving signals. In addition, the series protection resistor (300Ω to pin 6 of the NE5537) will add an RC time constant, over and above the slew rate limitation of the input buffer / current drive amplifier. This means that at the moment the "hold" command arrives, the hold capacitor voltage may be somewhat different than the actual analog input. The effect of these delays is opposite to the effect created by delays in the logic which switches the circuit from sample to hold. For example, consider an analog input of 20 Vp-p at 10kHz. Maximum dV / dt is 0.6V / μs. With no analog phase delay and 100ns logic delay, one could expect up to (0.1μs) (0.6V / μs) = 60mV error if the "hold" signal arrived near maximum dV / dt of the input. A positive going input would give a ±60mV error. Now assume a 1MHz (3dB) bandwidth for the overall analog loop. This generates a phase delay of 160ns. If the hold capacitor sees this exact delay, then error due to analog delay will be (0.16μs) (0.6V / μs) = −96mV (analog) for a total of −36mV. To add to the confusion, analog delay is proportional to hold capacitor value while digital delay remains constant. A family of curves (dynamic sampling error) is included to help estimate errors.

A curve labeled *Aperture Time* has been included for sampling conditions where the input is steady during the sampling period, but may experience a sudden change nearly coincident with the "hold" command. This curve is based on a 1mV error fed into the output.

A second curve, *Hold Settling Time* indicates the time required for the output to settle to 1mV after the "hold" command.

Digital Feedthrough

Fast rise time logic signals can cause hold errors by feeding externally into the analog input at the same time the amplifier is put into the hold mode. To minimize this problem, board layout should keep logic lines as far as possible from the analog input. Grounded guarding traces may also be used around the input line, especially if it is driven from a high impedance source. Reducing high amplitude logic signals to 2.5V will also help.

NOTE
Logic signals also couple to hold cap. Hold cap is guarded by trace connected to sample & hold output. This also minimizes board leakage.

SPECIAL NOTES

1. Not all definitions herein defined are measured parametrically for the NE5537, but are legitimate terms used in sample and hold systems.
2. Reference should be made to Design Engineering, volumes 23 (Nov. 8, 1978), 25 (Dec. 6, 1978) and 26 (Dec. 20, 1978) for articles written by Eugene Zuch of Datel Systems, Inc. for a further discussion of sample and hold circuits.
3. Reference also made to National Semiconductor Corporation's Special Functions Data Book (1976).

DUAL HIGH SLEW RATE OP AMPS NE/SE538/5538

NE/SE538-N,H,FE • NE/SE5538-H,N

DESCRIPTION

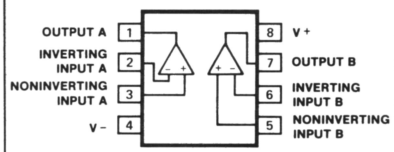
The NE/SE538/5538 are new generation operational amplifiers featuring high slew rates combined with improved input characteristics. Internally compensated for gains of 5 or larger, the SE538/5538 offers guaranteed minimum slew rates of 40V/µs or larger. Featuring 2mV max input offset voltage, the 538 is a single amplifier while the 5538 is a dual amplifier. Industry standard pin out and internal compensation allow the user to upgrade system performance by directly replacing general purpose amplifiers, such as 748, 101A, 741, 747 and 1458.

FEATURES

- **2mV max input offset voltage**
- **60nA max input offset current**
- **Short circuit protected**
- **Offset null capability**
- **Large common mode and differential voltage ranges**
- **60V/µs slew rate (gain of +5, -4 min)**
- **6MHz gain bandwidth product (gain +5, -4 minimum)**
- **Internal frequency compensation (gain of +5, -4 minimum)**
- **Pin out: 538 same as 741 (single)**
  5538 same as 747, 1458 (dual)

PIN CONFIGURATIONS

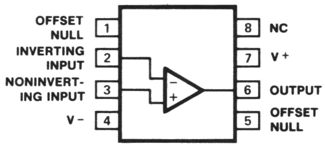
N PACKAGE


OUTPUT A
INVERTING INPUT A
NONINVERTING INPUT A
V -
1
2
3
4
8
7
6
5
V +
OUTPUT B
INVERTING INPUT B
NONINVERTING INPUT B

ORDER PART NO.

SE5538N, NE5538N

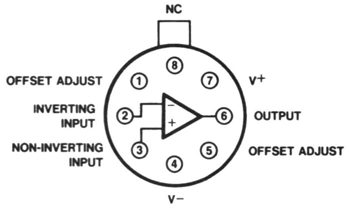
FE, N PACKAGE


OFFSET NULL
INVERTING INPUT
NONINVERTING INPUT
V -
1
2
3
4
8
7
6
5
NC
V +
OUTPUT
OFFSET NULL

ORDER PART NO.

SE538N, FE NE538N, FE

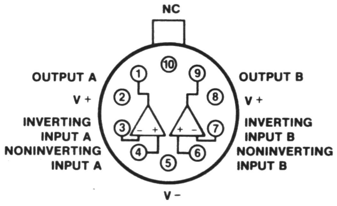
H PACKAGE


NC
OFFSET ADJUST
INVERTING INPUT
NON-INVERTING INPUT
V−
V+
OUTPUT
OFFSET ADJUST
1
2
3
4
5
6
7
8

ORDER PART NO.

SE538H NE538H

H PACKAGE


NC
OUTPUT A
V +
INVERTING INPUT A
NONINVERTING INPUT A
V -
OUTPUT B
V +
INVERTING INPUT B
NONINVERTING INPUT B
1
2
3
4
5
6
7
8
9
10

ORDER PART NO.

SE5538H NE5538H

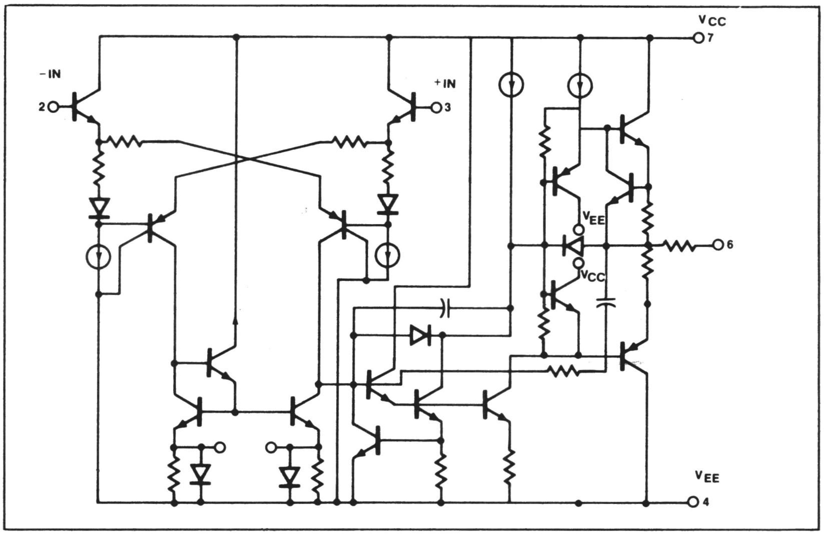
ABSOLUTE MAXIMUM RATINGS[1,2,3]

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		
	SE military grade	±22	V
	NE commercial grade	±18	V
P_D	Internal power dissipation FE package	1000	mW
P_D	Internal power dissipation[1] N package	500	mW
P_D	Internal power dissipation[1] H package	800	mW
	Differential input voltage	±30	V
	Input voltage[2]	±15	V
	Operating temperature range		
	SE military grade	-55 to +125	°C
	NE commercial grade	0 to 70	°C
	Output short circuit[3]	indefinite	
	Storage temperature range	-65 to +150	°C
	Lead temperature (solder, 60sec.)	300	°C

NOTES

1. Rating applies for thermal resistances of 240°C/W and 150°C/W junction to ambient for N and H packages. Maximum chip temperature is 150°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

EQUIVALENT SCHEMATIC (EACH AMPLIFIER)



DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = ± 15V unless otherwise specified.

PARAMETER		TEST CONDITIONS	SE538/SE5538			NE538/NE5538			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S \leq 10k\Omega$		0.7	4.0		2.0	6.0	mV
V_{OS}	Input offset voltage	$R_S \leq 10k\Omega$, over temp.			5.0			7.0	mV
ΔV_{OS}	Input offset voltage drift	$R_S = 0\Omega$, over temp.		6.0			6.0		μV/°C
I_{OS}	Input offset current			5	20		15	40	nA
I_{OS}	Input offset current	Over temp.			40			80	nA
I_B	Input current			45	80		65	150	nA
I_B	Input current	Over temp.			200			200	nA
V_{CM}	Input common mode voltage range		±12	±13		±12	±13		V
C_{MRR}	Common mode rejection ratio	$R_S \leq 10k\Omega$, over temp.	70	90		70	90		dB
P_{SRR}	Power supply rejection	$R_S \leq 10k\Omega$, over temp.		30	150		30	150	μV/V
R_{IN}	Input resistance		3	10		1	6		MΩ
A_{VOL}	Large signal voltage gain	$R_L \geq 2k\Omega$, $V_{OUT} = \pm10V$	50	200		50	200		V/mV
A_{VOL}	Large signal voltage gain	Over temp., $R_L \geq 2k\Omega$, $V_{OUT} = \pm10V$	25			25			V/mV
V_{OUT}	Output voltage	Over temp., $R_L \geq 2k\Omega$	±10	±13		±10	±13		V
V_{OUT}	Output voltage	Over temp., $R_L \geq 10k\Omega$	±12	±14		±12	±14		V
I_{CC}	Supply current	Per amplifier		2	3		2	3	mA
I_{CC}	Supply current	Over temp., per amplifier		2.2	3.6		2.2		mA
P_D	Power dissipation	Per amplifier		60	90		60	90	mW
P_D	Power dissipation	Over temp., per amplifier		66	108		66		mW
I_{SC}	Output short circuit current			25			25		mA
R_{OUT}	Output resistance			100			100		Ω

NOTE

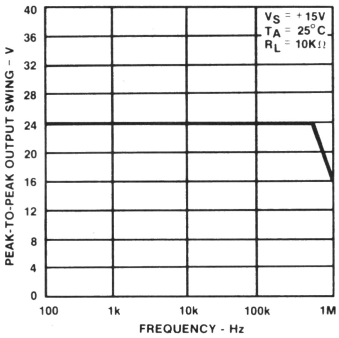
Temperature Range
SE Types -55°C ≤ T_A ≤ 125°C
NE Types 0°C ≤ T_A ≤ 70°C

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

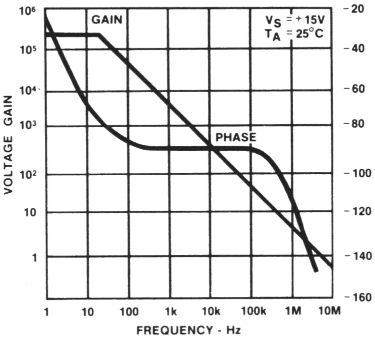
PARAMETER	TEST CONDITIONS	SE538/SE5538			SE538/NE5538			UNIT
		Min	Typ	Max	Min	Typ	Max	
Gain bandwidth product (Gain +5, -4 minimum)			6			6		MHz
Transient response Small signal rise time Small signal overshoot			0.25 6			0.25 6		μs %
Settling time	To 0.1%		1.2			1.2		μs
Slew rate	Minimum gain = 5 Noninverting $R_L \geq 2k\Omega$	40	60			60		V/μs

TYPICAL PERFORMANCE CHARACTERISTICS

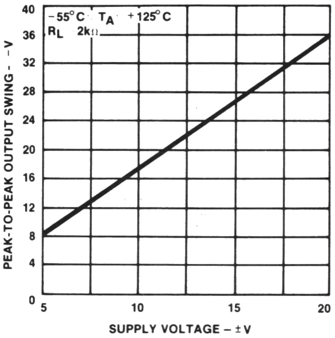
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



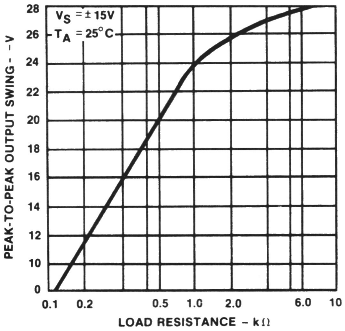
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



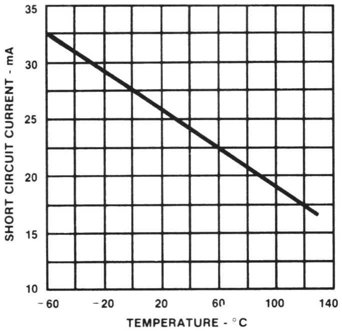
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



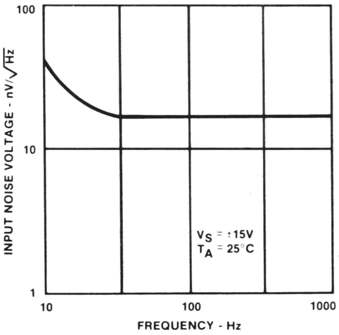
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



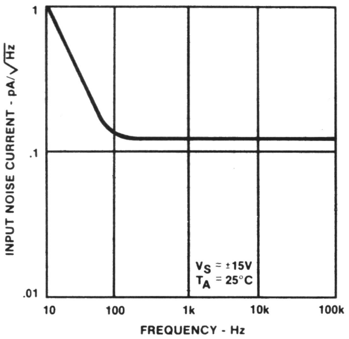
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



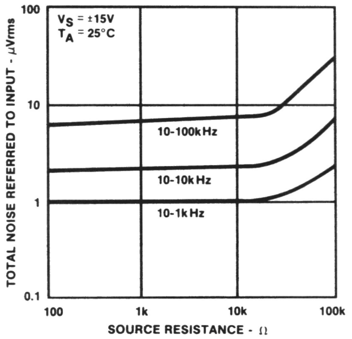
NE/SE538-N,H,FE • NE/SE5538-H,N

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

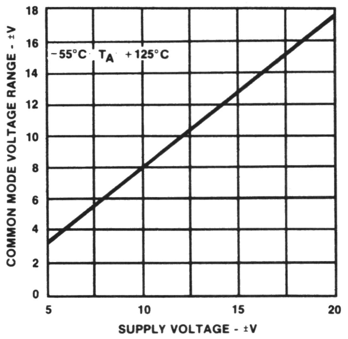
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



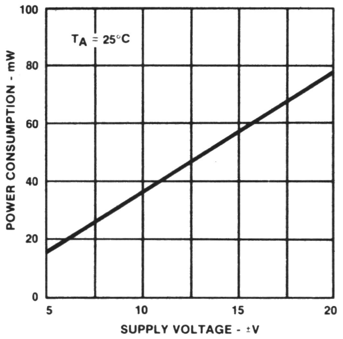
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



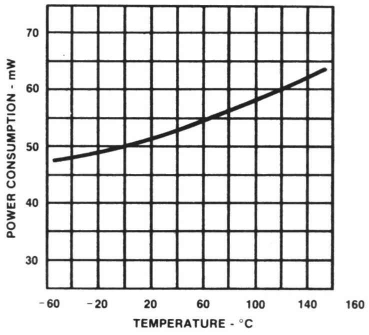
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



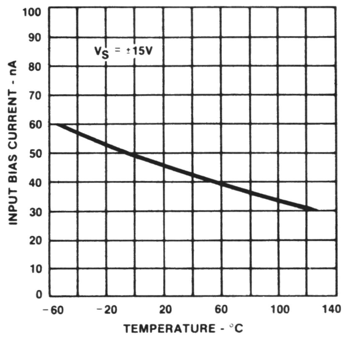
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



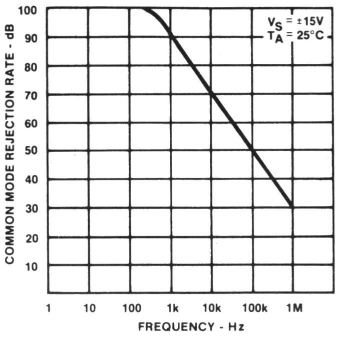
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



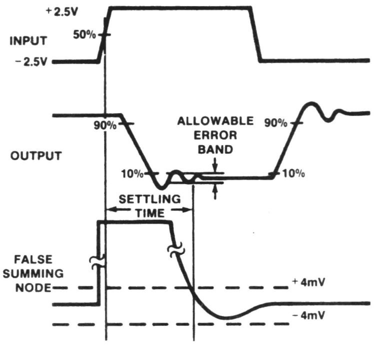
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY

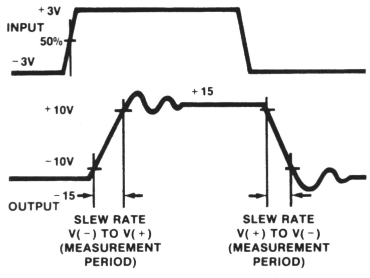


SETTLING TIME MEASUREMENT WAVEFORMS



+2.5V
INPUT
50%
-2.5V
OUTPUT
90%
ALLOWABLE ERROR BAND
90%
10%
10%
SETTLING TIME
FALSE SUMMING NODE
+4mV
-4mV

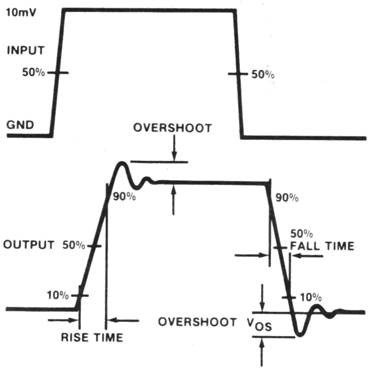
SLEW RATE MEASUREMENT VCC = ±20V



+3V
INPUT
50%
-3V
+15
+10V
-10V
-15
OUTPUT
SLEW RATE V(-) TO V(+) (MEASUREMENT PERIOD)
SLEW RATE V(+) TO V(-) (MEASUREMENT PERIOD)

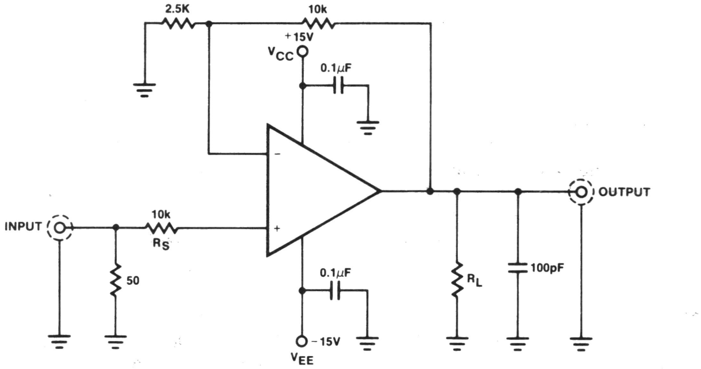
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

SMALL-SIGNAL TRANSIENT RESPONSE DEFINITIONS



TEST LOAD CIRCUITS

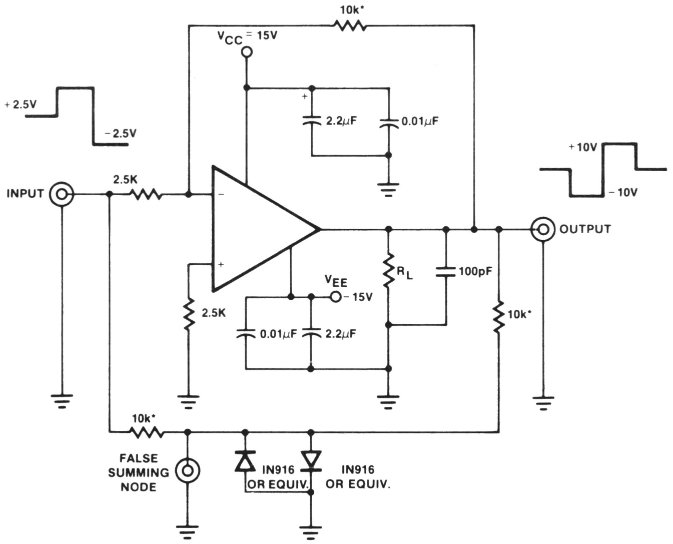
SLEW RATE AND SMALL SIGNAL TRANSIENT RESPONSE TEST CIRCUIT


2.5K
10k
+15V
V_{CC}
0.1μF
−
+
OUTPUT
INPUT
10k
R_S
50
0.1μF
−15V
V_{EE}
R_L
100pF

NOTE
Pins not shown are not connected.
All resistors values are typical and in ohms.

TEST LOAD CIRCUITS (Cont'd)

SETTLING TIME TEST CIRCUIT


10k*
V_{CC} = 15V
+2.5V
−2.5V
2.2μF
0.01μF
+10V
−10V
INPUT
2.5K
−
+
OUTPUT
V_{EE}
−15V
R_L
100pF
2.5K
0.01μF
2.2μF
10k*
10k*
FALSE SUMMING NODE
IN916 OR EQUIV.
IN916 OR EQUIV.

*Match to within 0.01%.
NOTE

Pins not shown are not connected.
All resistors values are typical and in ohms.

DESCRIPTION

The Signetics LF198/LF298/LF398 are monolithic sample and hold circuits which utilize high-voltage Ion-Inplant JFET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, dc gain accuracy is 0.002% typical and acquisition time is as low as 6µs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin and does not degrade input offset drift. The wide bandwidth allows the LF198 to be included inside the feedback loop of 1MHz op amps without having stability problems. Input impedance of $10^{10}\Omega$ allows high source impedances to be used without degrading accuracy.

P-channel junction FET's are combined with bipolar devices in the output amplifier to give droop rates as low as 5mV/min with a 1µF hold capacitor. The JFET's have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feed-through from input to output in the hold mode even for input signals equal to the supply voltages.

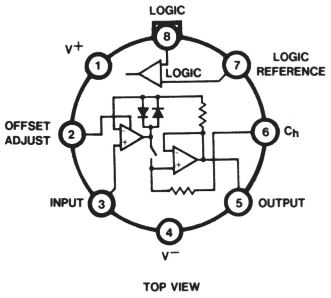
Logic inputs on the LF198 are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS. Differential threshold is 1.4V. The LF198 will operate from ±5V to ±18V supplies. It is available in an 8-lead TO-5 package.

FEATURES

- **Operates from ±5V to ±18V supplies**
- **Less than 10µs acquisition time**
- **TTL, PMOS, CMOS compatible logic input**
- **0.5mV typical hold step at C_h = 0.01µF**
- **Low input offset**
- **0.002% gain accuracy**
- **Low output noise in hold mode**
- **Input characteristics do not change during hold mode**
- **High supply rejection ratio in sample or hold**
- **Wide bandwidth**
- **The LF198/LF298/LF398 are ideally suited for a wide variety of sample and hold applications including data acquisition, analog to digital conversion, synchronous demodulation, and automatic test setup.**

PIN CONFIGURATION

H PACKAGE



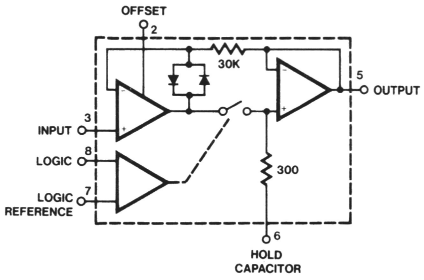
ORDER PART

NO. LF198H
LF298H
LF398H

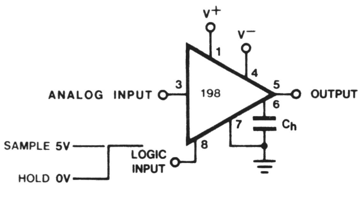
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	±18	V
Power dissipation (package limitation)[1]	500	mW
Operating ambient temperature range		
LF198	−55 to +125	°C
LF298	−25 to +85	°C
LF398	0 to +70	°C
Storage temperature range	−65 to +150	°C
Input voltage	Equal to supply voltage	
Logic to logic reference differential voltage[2]	+7, −30	V
Output short circuit duration	Indefinite	
Hold capacitor short circuit duration	10	sec
Lead temperature (soldering, 10sec)	300	°C

FUNCTIONAL DIAGRAM



TYPICAL APPLICATIONS



DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, $V_S = \pm 15V$, $T_j = 25°C$, $-11.5V \leq V_{IN} \leq +11.5V$, $C_h = 0.01\mu F$, and $R_L = 10k\Omega$. Logic reference voltage = OV and logic voltage = 2.5V.

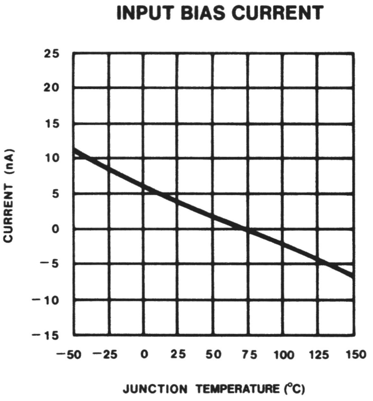
PARAMETER	TEST CONDITIONS	LF198/LF298			LF398			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage [6]	$T_j = 25°C$ Full temperature range		1	3 5		2	7 10	mV mV
Input bias current [6]	$T_j = 25°C$ Full temperature range		5	25 75		10	50 100	nA nA
Input impedance	$T_j = 25°C$		10^{10}			10^{10}		Ω
Gain error	$T_j = 25°C$, $R_L = 10K$ Full temperature range		0.002	0.005 0.02		0.004	0.01 0.02	% %
Feedthrough attenuation ratio at 1kHz	$T_j = 25°C$, $C_h = 0.01\mu F$	86	96		80	90		dB
Output impedance	$T_j = 25°C$, "HOLD" mode Full temperature range		0.5	2 4		0.5	4 6	Ω Ω
"HOLD" step [4]	$T_j = 25°C$, $C_h = 0.01\mu F$, $V_{OUT} = 0$		0.5	2.0		1.0	2.5	mV
Supply current [6]	$T_j \geq 25°C$		4.5	5.5		4.5	6.5	mA
Logic and logic reference input current	$T_j = 25°C$		2	10		2	10	μA
Leakage current into hold capacitor [6]	$T_j = 25°C$ [5] Hold mode		30	100		30	200	pA
Acquisition time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000pF$ $C_h = 0.01\mu F$		4 20			4 20		μs μs
Hold capacitor charging current	V_{IN}-$V_{OUT} = 2V$		5			5		mA
Supply voltage rejection ratio	$V_{OUT} = 0$	80	110		80	110		dB
Differential logic threshold	$T_j = 25°C$	0.8	1.4	2.4	0.8	1.4	2.4	V

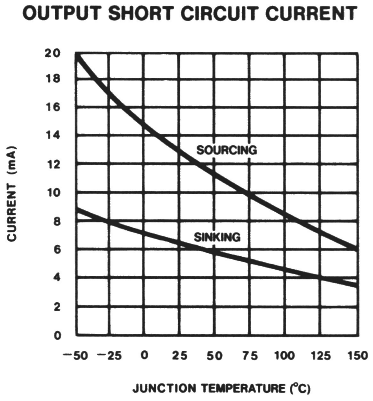
NOTES

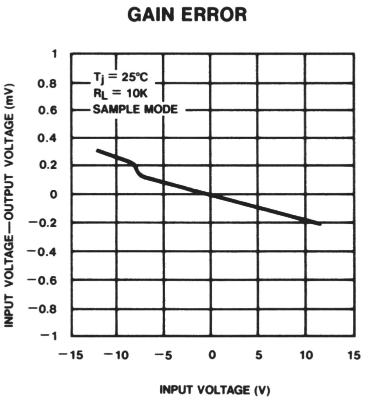
1. The maximum junction temperature of the LF198 is 150°C, for the LF298, 115°C, and for the LF398, 100°C. When operating at elevated ambient temperature, the TO-5 package must be derated based on a thermal resistance (ΘjA) of 150°C/W.
2. Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.
3. Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, $V_S = \pm 15V$, $T_j = 25°C$, $-11.5V \leq V_{IN} \leq +11.5V$, $C_h = 0.01\mu F$, and $R_L = 10k\Omega$. Logic reference voltage = OV and logic voltage = 2.5V.
4. Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01μF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.
5. Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.
6. The parameters guaranteed over a supply voltage of ±5 to ±18V.

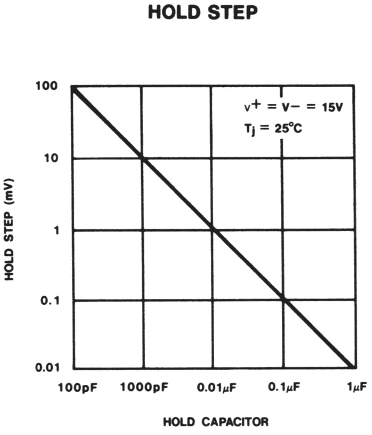
LF198/LF298/LF398-H

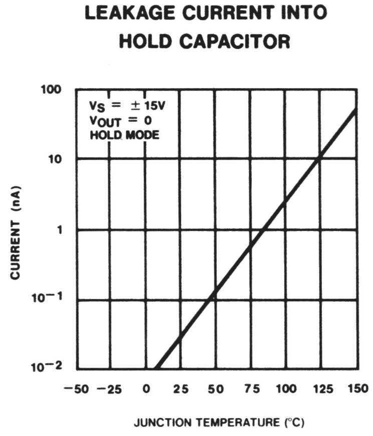
TYPICAL DC PERFORMANCE CHARACTERISTICS

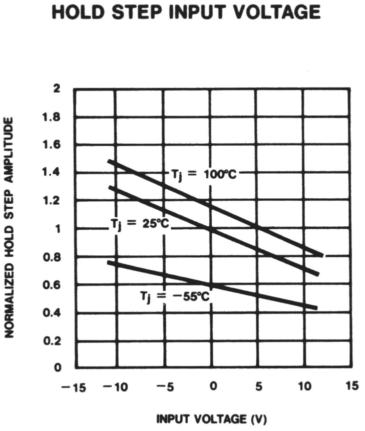

INPUT BIAS CURRENT


OUTPUT SHORT CIRCUIT CURRENT

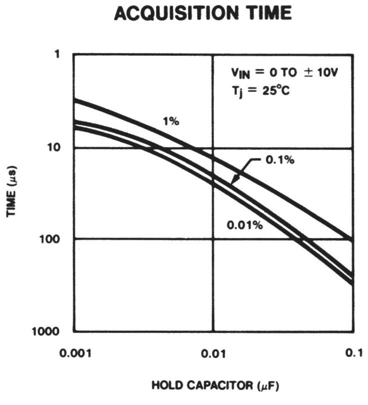

GAIN ERROR

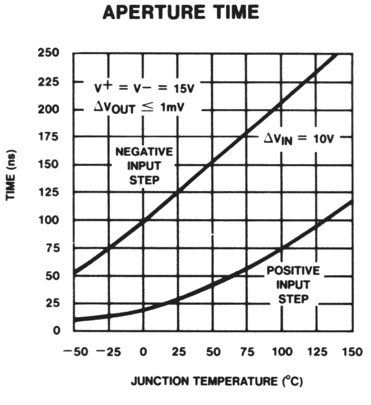

HOLD STEP

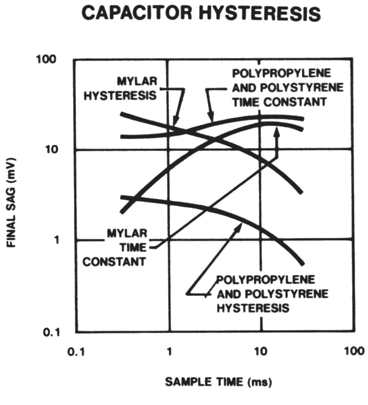

LEAKAGE CURRENT INTO HOLD CAPACITOR


HOLD STEP INPUT VOLTAGE

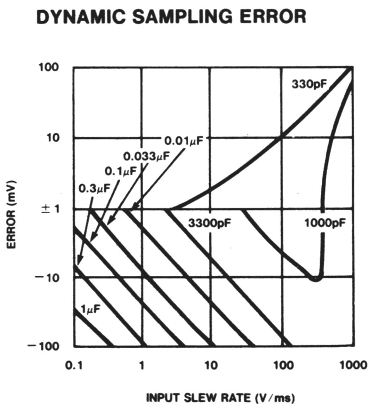
TYPICAL AC PERFORMANCE CHARACTERISTICS

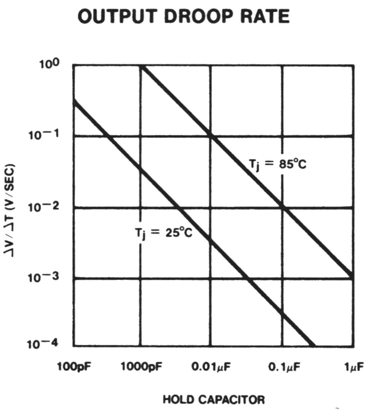

ACQUISITION TIME

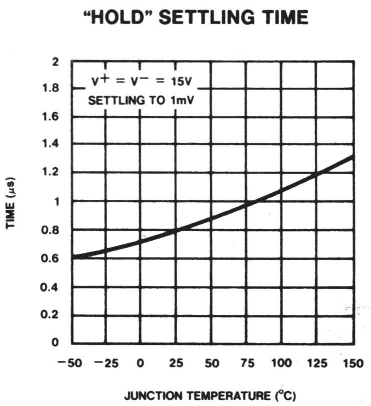

APERTURE TIME

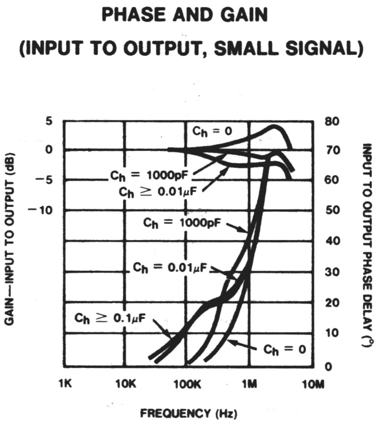

CAPACITOR HYSTERESIS

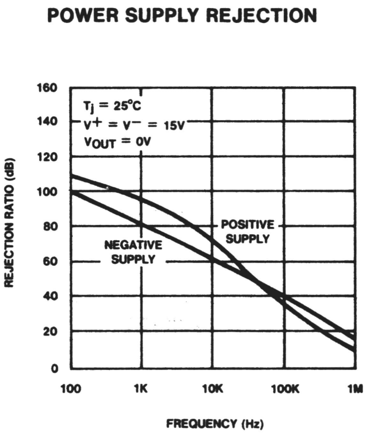
TYPICAL AC PERFORMANCE CHARACTERISTICS (cont'd)

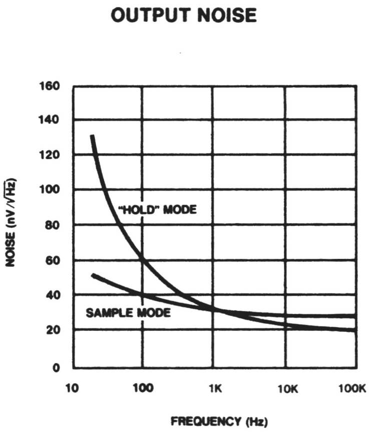

DYNAMIC SAMPLING ERROR

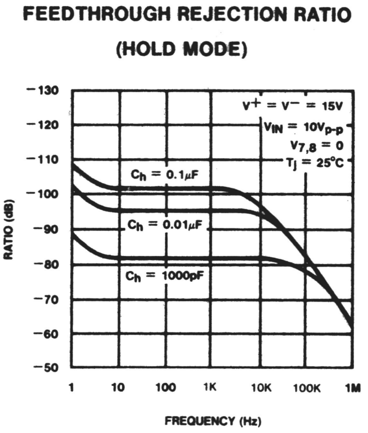

OUTPUT DROOP RATE


"HOLD" SETTLING TIME


PHASE AND GAIN
(INPUT TO OUTPUT, SMALL SIGNAL)


POWER SUPPLY REJECTION


OUTPUT NOISE


FEEDTHROUGH REJECTION RATIO
(HOLD MODE)

μA741/741C,
MC1458/1558-F,N,H

DESCRIPTION

The μA741 is a high performance operational amplifier with high open loop gain, internal compensation, high common mode range and exceptional temperature stability. The μA741 is short-circuit protected and allows for nulling of offset voltage.

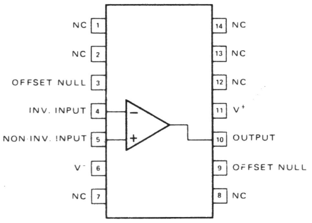
The MC1558/MC1458/SA1458 consist of a pair of 741 operational amplifiers on a single chip.

FEATURES

- **Internal frequency compensation**
- **Short circuit protection**
- **Excellent temperature stability**
- **High input voltage range**
- **No latch-up**
- **1558/1458 are 2 "op amps" in space of one 741 package**
- **MC1558 Mil std 883A,B,C available**
- **μA741 Mil std 883A,B,C available**

PIN CONFIGURATIONS

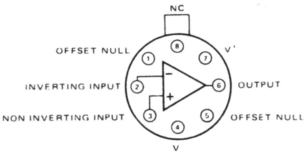
F,N-14 PACKAGE


NC 1
NC 2
OFFSET NULL 3
INV. INPUT 4
NON INV. INPUT 5
V⁻ 6
NC 7
14 NC
13 NC
12 NC
11 V⁺
10 OUTPUT
9 OFFSET NULL
8 NC
−
+

ORDER PART NO.

μA741F
μA741N-14
μA741CF
μA741CN-14

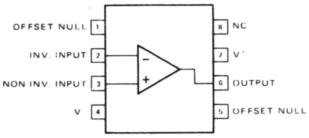
H PACKAGE


NC
OFFSET NULL
V⁺
INVERTING INPUT
OUTPUT
NON INVERTING INPUT
OFFSET NULL
V
1
2
3
4
5
6
7
8
−
+

ORDER PART NO.

μA741H
μA741CH

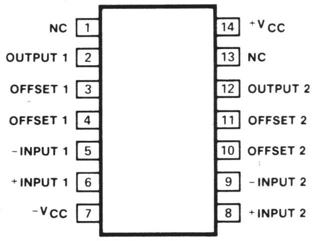
N PACKAGE


OFFSET NULL 1
INV. INPUT 2
NON INV. INPUT 3
V 4
8 NC
7 V⁺
6 OUTPUT
5 OFFSET NULL
−
+

ORDER PART NO.

μA741N
μA741CN

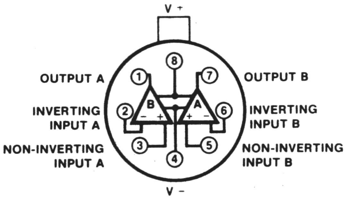
F,N-14 PACKAGE


NC 1
OUTPUT 1 2
OFFSET 1 3
OFFSET 1 4
−INPUT 1 5
+INPUT 1 6
−VCC 7
14 +VCC
13 NC
12 OUTPUT 2
11 OFFSET 2
10 OFFSET 2
9 −INPUT 2
8 +INPUT 2

ORDER PART NO.

MC1458F
MC1558F
MC1458N-14
MC1558N-14

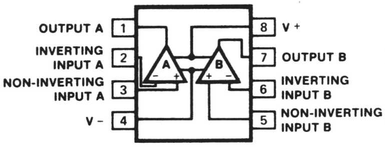
H PACKAGE


V +
OUTPUT A
INVERTING INPUT A
NON-INVERTING INPUT A
OUTPUT B
INVERTING INPUT B
NON-INVERTING INPUT B
V −
1
2
3
4
5
6
7
8
A
B

ORDER PART NO.

MC1458H
MC1558H

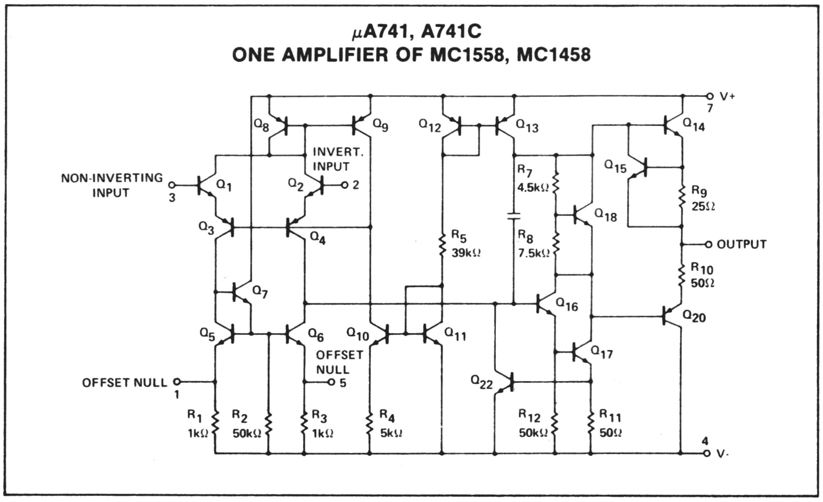
N PACKAGE


OUTPUT A 1
INVERTING INPUT A 2
NON-INVERTING INPUT A 3
V − 4
8 V +
7 OUTPUT B
6 INVERTING INPUT B
5 NON-INVERTING INPUT B
A
B

ORDER PART NO.

MC1458N
MC1558N

EQUIVALENT SCHEMATIC


μA741, A741C
ONE AMPLIFIER OF MC1558, MC1458

V+
7
Q8
Q9
Q12
Q13
Q14
INVERT. INPUT
NON-INVERTING INPUT
3
Q1
Q2
2
R7 4.5kΩ
Q15
R9 25Ω
Q18
Q3
Q4
R5 39kΩ
R8 7.5kΩ
OUTPUT
R10 50Ω
Q7
Q16
Q20
Q5
Q6
Q10
Q11
OFFSET NULL
5
Q17
OFFSET NULL
1
Q22
R1 1kΩ
R2 50kΩ
R3 1kΩ
R4 5kΩ
R12 50kΩ
R11 50Ω
4
V-

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
μA741C	±18	V
MC1458		
μA741, MC1558	±22	V
Internal power dissipation, N-14	600	mW
N package	500	mW
H package[1]	800	mW
F package	1000	mW
Differential input voltage	±30	V
Input voltage[2]	±15	V
Output short-circuit duration	Continuous	
Operating temperature range		
μA741C, MC1458	0 to +70	°C
	-40 to +85	°C
μA741, MC1558	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 60sec)	300	°C

NOTES

1. Ratings based on thermal resistances, junction to ambient, of 208°C/W, 240°C/W, 150°C/W, 110°C/W for N-14, N, H and F packages respectively, and a maximum junction temperature of 150°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm15V$, unless otherwise specified.

PARAMETER		TEST CONDITIONS	μA741			μA741C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S = 10k\Omega$		1.0	5.0		2.0	6.0	mV
		$R_S = 10k\Omega$, over temp.		1.0	6.0			7.5	mV
I_{OS}	Offset current			20	200		20	200	nA
		Over temp.						300	nA
		$T_A = +125°C$		7.0	200				nA
		$T_A = -55°C$		20	500				nA
I_{BIAS}	Input bias current			80	500		80	500	nA
		Over temp.						800	nA
		$T_A = +125°C$		30	500				nA
		$T_A = -55°C$		300	1500				nA
V_{OUT}	Output voltage swing	$R_L = 10k\Omega$	±12	±14		±12	±14		V
		$R_L = 2k\Omega$, over temp.	±10	±13		±10	±13		V
A_{VOL}	Large signal voltage gain	$R_L = 2k\Omega$, $V_O = \pm10V$	50	200		20	200		V/mV
		$R_L = 2k\Omega$, $V_O = \pm10V$, over temp.	25			15			V/mV
	Offset voltage adjustment range			±30			±30		mV
P_{SRR}	Supply voltage rejection ratio	$R_S \leq 10k\Omega$					10	150	μV/V
		$R_S \leq 10k\Omega$, over temp.		10	150				μV/V
CMRR	Common mode rejection ratio								dB
		Over temp.	70	90					dB
I_{CC}	Supply current			1.4	2.8		1.4	2.8	mA
		$T_A = +125°C$		1.5	2.5				mA
		$T_A = -55°C$		2.0	3.3				mA
V_{IN}	Input voltage range	(μA741, over temp.)	±12	±13		±12	±13		V
R_{IN}	Input resistance		0.3	2.0		0.3	2.0		MΩ
P_d	Power consumption			50	85		50	85	mW
		$T_A = +125°C$		45	75				mW
		$T_A = -55°C$		45	100				mW
R_{OUT}	Output resistance			75			75		Ω
I_{SC}	Output short-circuit current			25			25		mA

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$, $V_S = ±15V$, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MC1558			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage	$R_S = 10kΩ$ $R_S = 10kΩ$, over temp.		1.0	5.0 6.0	mV mV
I_{OS}	Offset current	 Over temp.		20	200 500	nA nA
I_{BIAS}	Input bias current	 Over temp.		80	500 1500	nA nA
V_{OUT}	Output voltage swing	$R_L = 10kΩ$ $R_L = 2kΩ$, over temp.	±12 ±10	±14 ±13		V V
A_{VOL}	Large signal voltage gain	$R_L = 2kΩ$, $V_O = ±10V$ $R_L = 2kΩ$, $V_O = ±10V$, over temp.	50 25	100		V/mV V/mV
	Offset voltage adjustment range			±30		mV
P_{SRR}	Supply voltage rejection ratio	$R_S \leq 10kΩ$		30	150	μV/V
CMRR	Common mode rejection ratio			70	90	dB
I_{CC}	Supply current			2.3	5.6	mA
V_{IN} R_{IN}	Input voltage range Input resistance	(μA741, over temp.)	±12	±13		V MΩ
P_d	Power consumption			70	150	mW
 R_{OUT} I_{SC}	Channel separation Output resistance Output short-circuit current			120 25		dB Ω mA

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$, $V_S = ±15V$, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MC1458			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage	$R_S = 10kΩ$ $R_S = 10kΩ$, over temp.		2.0	6.0 7.5	mV mV
I_{OS}	Offset current	 Over temp.		20	200 300	nA nA
I_{BIAS}	Input bias current	 Over temp.		80	500 800	nA nA
V_{OUT}	Output voltage swing	$R_L = 10kΩ$ $R_L = 2kΩ$, over temp.	±12 ±10	±14 ±13		V V
A_{VOL}	Large signal voltage gain	$R_L = 2kΩ$, $V_O = ±10V$ $R_L = 2kΩ$, $V_O = ±10V$, over temp.	25 15	200		V/mV V/mV
	Offset voltage adjustment range			±30		mV
P_{SRR}	Supply voltage rejection ratio	$R_S \leq 10kΩ$		30	170	μV/V
CMRR	Common mode rejection ratio			70	90	dB
I_{CC}	Supply current			2.3	5.0	mA
V_{IN} R_{IN}	Input voltage range Input resistance	(μA741, over temp.)	±12	±13		V MΩ
P_d	Power consumption			70	170	mW
 I_{SC}	Channel separation Output short-circuit current			120 25		dB mA

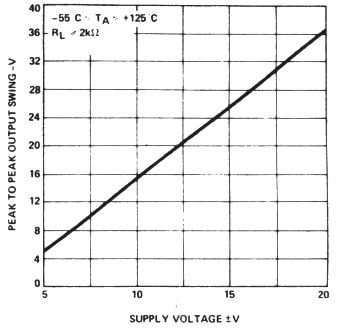
µA741/741C,
MC1458/1558-F,N,H

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm15V$, unless otherwise specified.

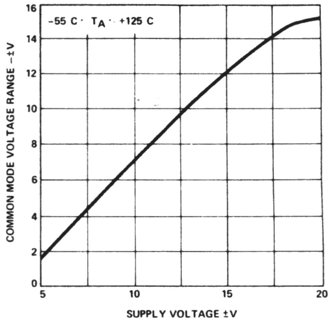
PARAMETER	TEST CONDITIONS	µA741, µA741C			MC1558, MC1458			UNIT
		Min	Typ	Max	Min	Typ	Max	
Parallel input resistance	Open loop, f = 20Hz				0.3			MΩ
Parallel input capacitance	Open loop, f = 20Hz		1.4					pF
Common mode input impedance	f = 20Hz					200		MΩ
Equivalent input noise voltage	$A_V = 100$, $R_S = 10k\Omega$, $B_W = 1.0kHz$ f = 1.0kHz					45		$nV\sqrt{Hz}$
Power bandwidth	$A_V = 1$, $R_L = 2.0k\Omega$, THD ≤ 5% $V_{OUT} = 20Vp\text{-}p$					14		kHz
Phase margin						65		degrees
Gain margin						11		dB
Unity gain crossover frequency	Open loop		1.0			1.0		MHz
Transient response unity gain	$V_{IN} = 20mV$, $R_L = 2k\Omega$, $C_L \leq 100pf$							
Rise time			0.3			0.3		µs
Overshoot			5.0			5.0		%
Slew rate	C ≤ 100pf, $R_L \geq 2k$, $V_{IN} = \pm10V$		0.5			0.8		V/µs

TYPICAL PERFORMANCE CHARACTERISTICS

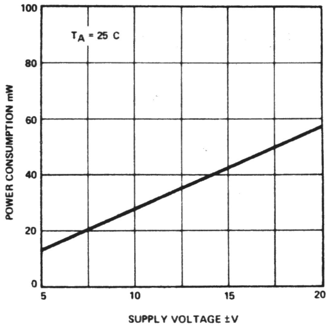
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



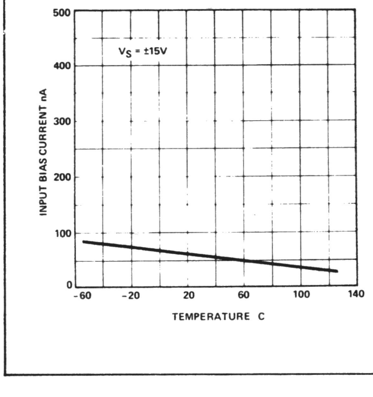
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



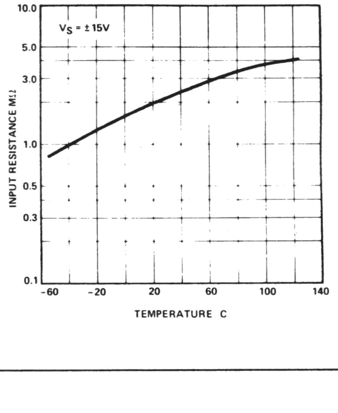
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



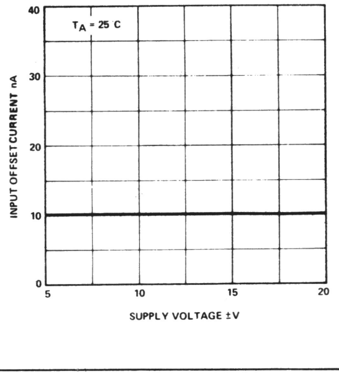
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

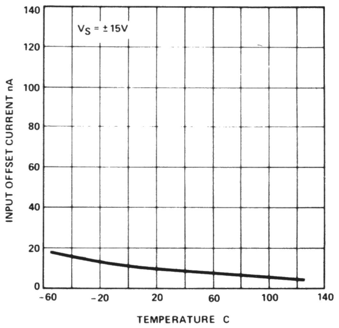


INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

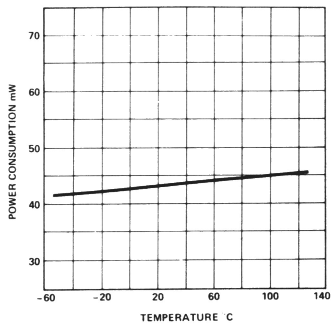


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

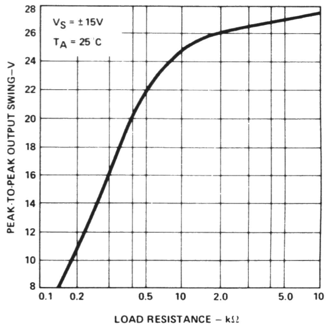
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



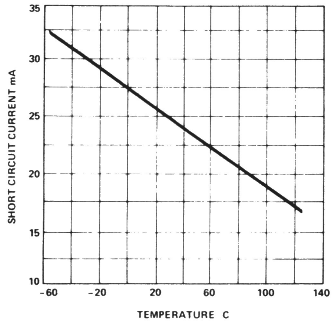
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



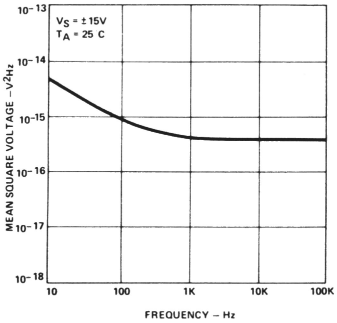
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



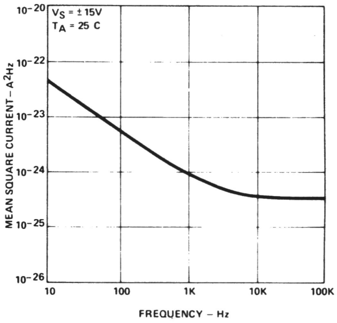
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



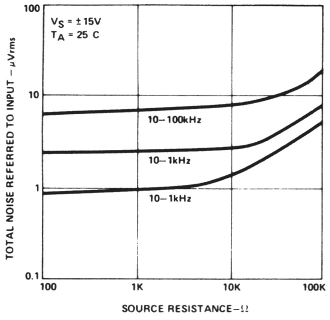
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



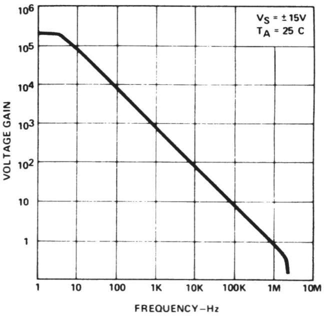
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



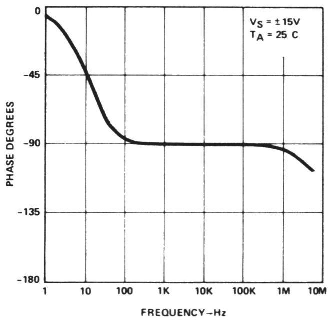
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

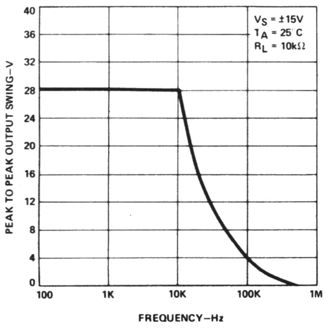


OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY

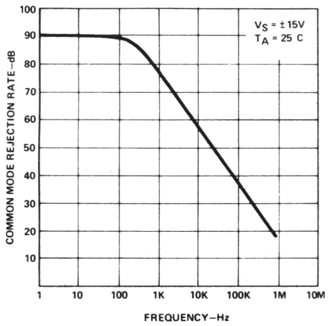


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

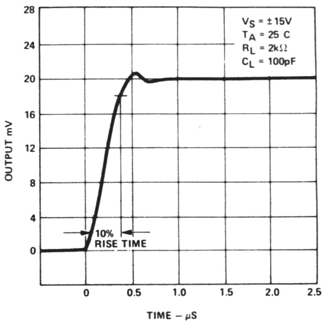
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



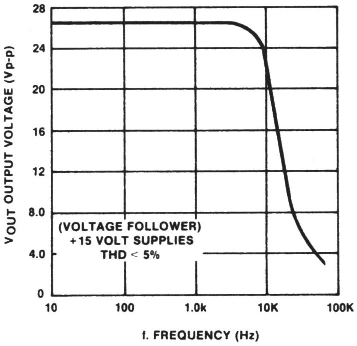
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



TRANSIENT RESPONSE



POWER BANDWIDTH (Large Signal Swing vs Frequency)



SECTION 2
VIDEO AMPLIFIERS

Section 2—VIDEO AMPLIFIERS

NE/SE592 Video Amplifier 81
**μA733 Video Amplifier .... *

**See NE/SE592 for pin to pin replacement.

NOTE

*Any product listed in this section but not incorporated within the text may be obtained by writing Information Services at Signetics, 811 E. Arques, M/S 027, Sunnyvale, California 94086, or by calling (408) 746-1682.

DESCRIPTION

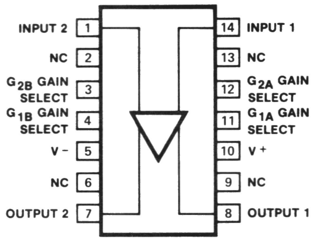
The SE/NE592 is a monolithic, two stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display and video recorder systems. The 592 is a pin-for-pin replacement for the μA733.

FEATURES

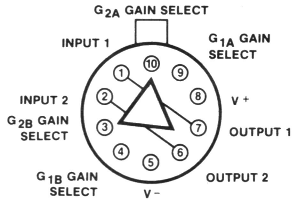
- **120MHz bandwidth**
- **Adjustable gains from 0 to 400**
- **Adjustable pass band**
- **No frequency compensation required**
- **Wave shaping with minimal external components**

PIN CONFIGURATION

F,N PACKAGE

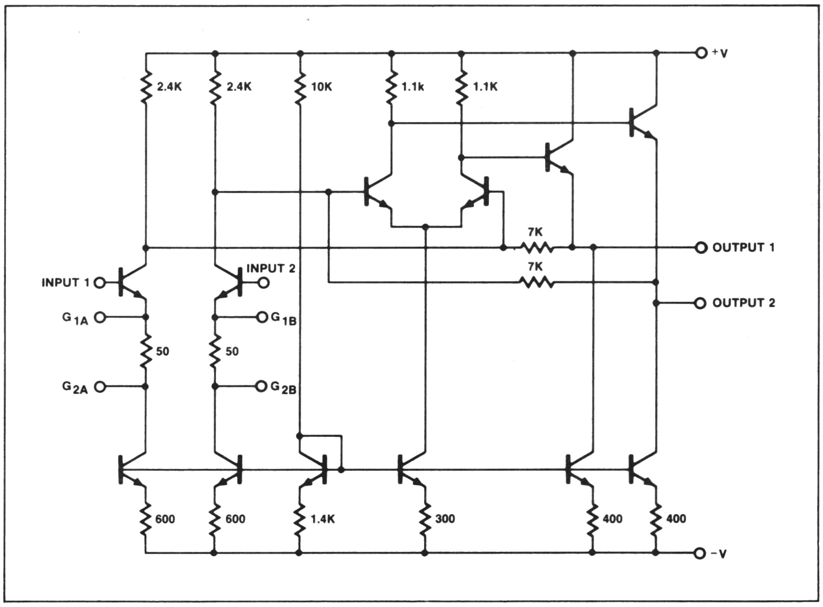

INPUT 2 1
NC 2
G2B GAIN SELECT 3
G1B GAIN SELECT 4
V− 5
NC 6
OUTPUT 2 7
14 INPUT 1
13 NC
12 G2A GAIN SELECT
11 G1A GAIN SELECT
10 V+
9 NC
8 OUTPUT 1

H PACKAGE


G2A GAIN SELECT
INPUT 1
G1A GAIN SELECT
INPUT 2
G2B GAIN SELECT
V+
OUTPUT 1
G1B GAIN SELECT
V−
OUTPUT 2
1
2
3
4
5
6
7
8
9
10

NOTE
Pin 5 connected to case.

EQUIVALENT CIRCUIT


+V
2.4K
2.4K
10K
1.1k
1.1K
7K
7K
OUTPUT 1
OUTPUT 2
INPUT 1
INPUT 2
G1A
G1B
50
50
G2A
G2B
600
600
1.4K
300
400
400
−V

ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$ unless otherwise specified.

PARAMETER	RATING	UNIT
Supply voltage	±8	V
Differential input voltage	±5	V
Common mode		
Input voltage	±6	V
Output current	10	mA
Operating temperature range		
SE592K	-55 to +125	°C
NE592K	0 to +70	°C
Storage temperature range	-65 to +150	°C
Power dissipation	500	mW

DC ELECTRICAL CHARACTERISTICS

T_A = +25°C, V_S = ±6V, V_{CM} = 0 unless otherwise specified
Recommend operating supply voltages V_S = ±6.0V

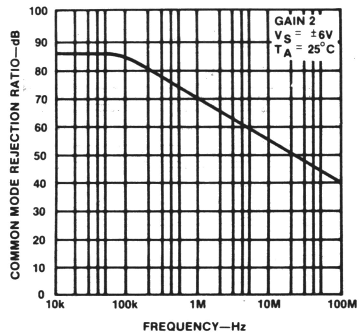
PARAMETER	TEST CONDITIONS	NE592			SE592			UNITS
		Min	Typ	Max	Min	Typ	Max	
Differential voltage gain								
Gain 1[1]	R_L = 2kΩ, V_{OUT} = 3V p-p	250	400	600	300	400	500	V/V
Gain 2[2]		80	100	120	90	100	110	V/V
Bandwidth								
Gain 1[1]			40			40		MHz
Gain 2[2]			90			90		MHz
Rise time								
Gain 1[1]	V_{OUT} = 1V p-p		10.5			10.5		ns
Gain 2[2]			4.5	12		4.5	10	ns
Propagation delay								
Gain 1[1]	V_{OUT} = 1V p-p		7.5			7.5		ns
Gain 2[2]			6.0	10		6.0	10	ns
Input resistance								
Gain 1[1]			4.0			4.0		kΩ
Gain 2[2]		10	30		20	30		kΩ
Input capacitance[2]	Gain 2		2.0			2.0		pF
Input offset current			0.4	5.0		0.4	3.0	μA
Input bias current			9.0	30		9.0	20	μA
Input noise voltage	BW 1kHz to 10kHz		12			12		μVrms
Input voltage range				±1.0			±1.0	V
Common mode rejection ratio								
Gain 2	VCM ±1V,F < 100kHz	60	86		60	86		dB
Gain 2	VCM ±1V,F = 5MHz		60			60		dB
Supply voltage rejection ratio								
Gain 2	ΔVS = ±0.5V	50	70		50	70		dB
Output offset voltage								
Gain 3[3]	$R_L = \infty$		0.35	0.75		0.35	0.75	V
Output common mode voltage	$R_L = \infty$	2.4	2.9	3.4	2.4	2.9	3.4	V
Ouptut voltage swing	R_L = 2K	3.0	4.0		3.0	4.0		
Ouput resistance			20			20		Ω
Power supply current	$R_L = \infty$		18	24		18	24	mA

NOTES

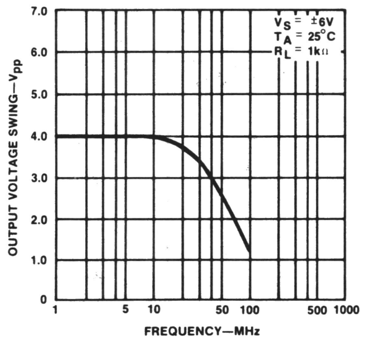
1. Gain select pins G_{1A} and G_{1B} connected together.
2. Gain select pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.

TYPICAL PERFORMANCE CHARACTERISTICS

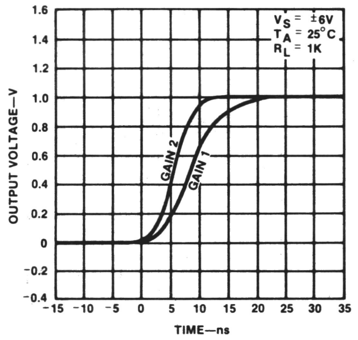
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



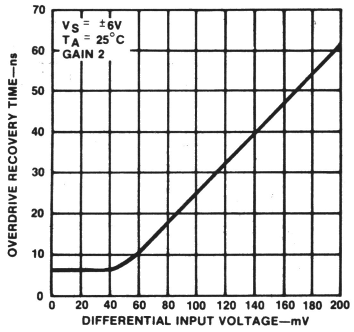
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



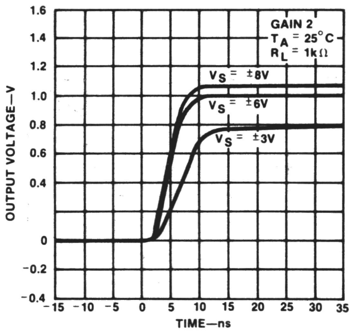
PULSE RESPONSE



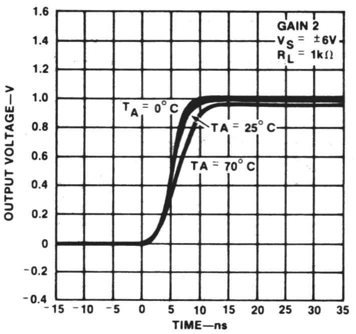
DIFFERENTIAL OVERDRIVE RECOVERY TIME



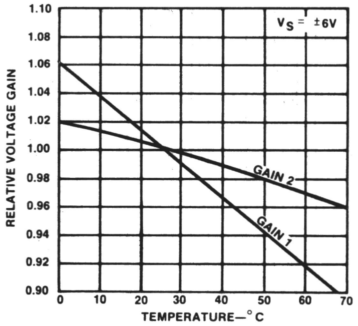
PULSE RESPONSE AS A FUNCTION OF SUPPLY VOLTAGE



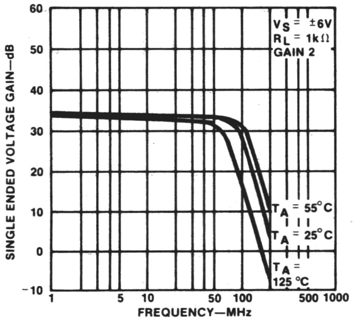
PULSE RESPONSE AS A FUNCTION OF TEMPERATURE



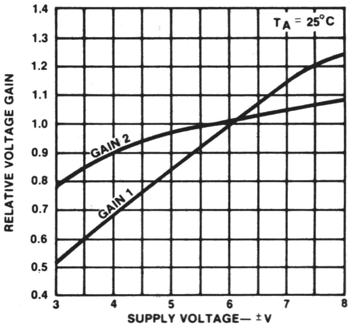
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



GAIN vs FREQUENCY AS A FUNCTION OF TEMPERATURE

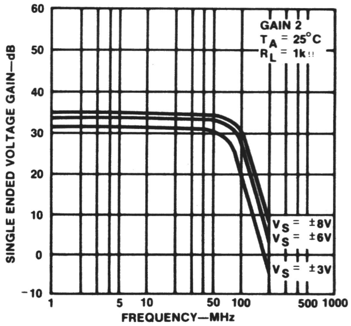


VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

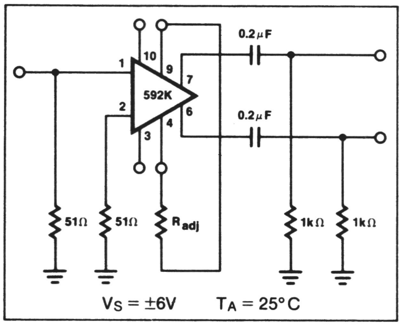


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

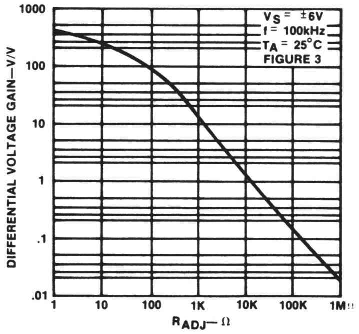
GAIN vs FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



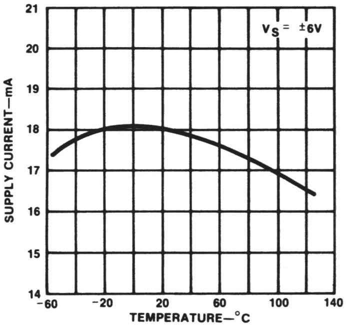
VOLTAGE GAIN ADJUST CIRCUIT



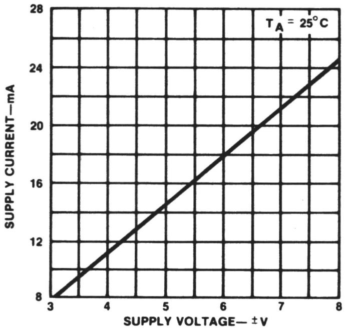
VOLTAGE GAIN AS A FUNCTION OF RADJ (FIGURE 3)



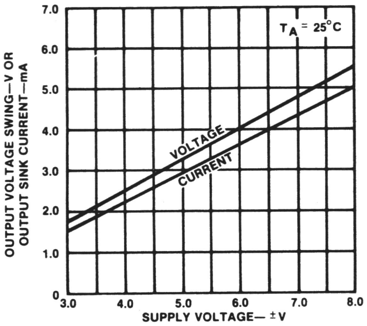
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



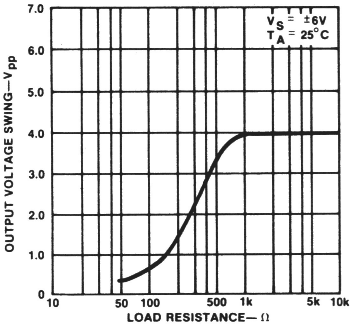
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



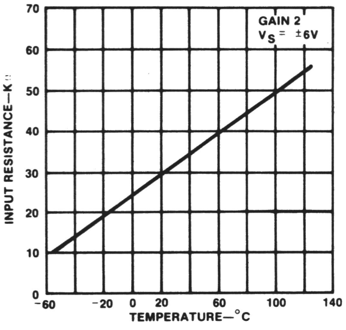
OUTPUT VOLTAGE AND CURRENT SWING AS A FUNCTION OF SUPPLY VOLTAGE



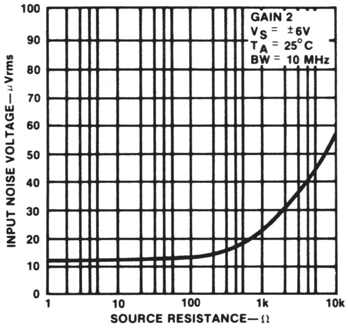
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



INPUT RESISTANCE AS A FUNCTION OF TEMPERATURE

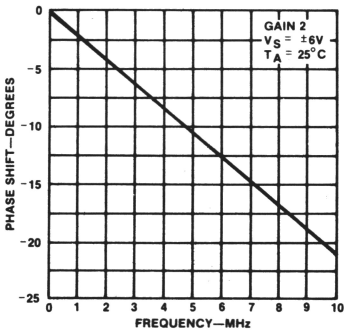


INPUT NOISE VOLTAGE AS A FUNCTION OF SOURCE RESISTANCE

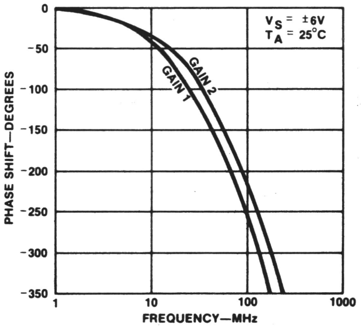


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

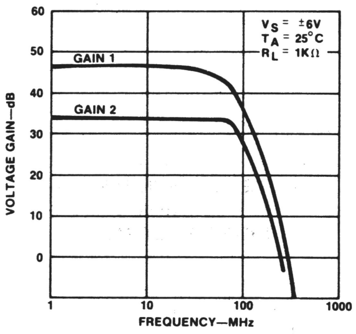
PHASE SHIFT AS A FUNCTION OF FREQUENCY



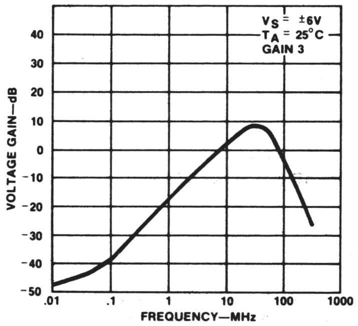
PHASE SHIFT AS A FUNCTION OF FREQUENCY



VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

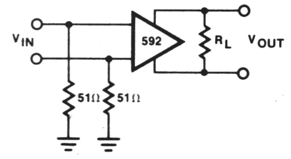


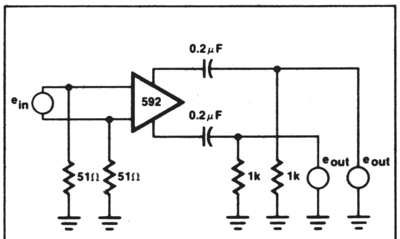
VOLTAGE GAIN AS A FUNCTION OF FREQUENCY (ALL GAIN SELECT PINS OPEN)



TEST CIRCUITS

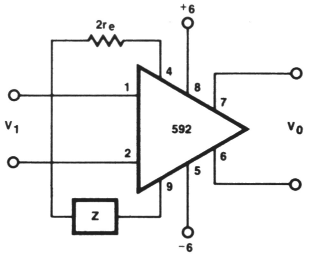
$T_A = 25°C$ unless otherwise specified


V_{IN}
592
R_L
V_{OUT}
51Ω
51Ω


0.2μF
0.2μF
e_{in}
592
51Ω
51Ω
1k
1k
e_{out}
e_{out}

TYPICAL APPLICATIONS

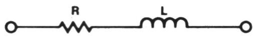
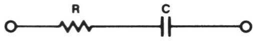
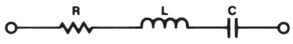
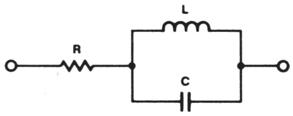
FILTER NETWORKS


2re
+6
4
8
1
7
V1
592
Vo
2
6
5
9
Z
-6

$$\frac{V_0(s)}{V_1(s)} \cong \frac{1.4 \times 10^4}{Z(s) + 2r_e}$$

$$\cong \frac{1.4 \times 10^4}{Z(s) + 32}$$

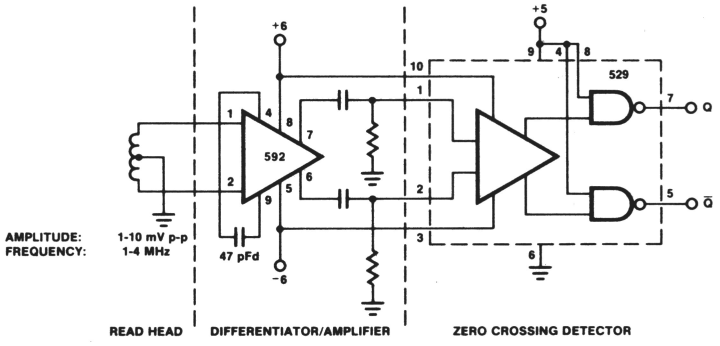
BASIC CONFIGURATION

Z NETWORK	FILTER TYPE	$V_0(s)$ TRANSFER $V_1(s)$ FUNCTION
	LOW PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
	HIGH PASS	$\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$
	BAND PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/L\, s + 1/LC}\right]$
	BAND REJECT	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

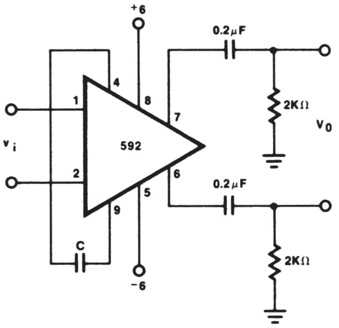
NOTE

In the networks above, the R value used is assumed to include $2r_e$, or approximately 32Ω.

DISC/TAPE PHASE MODULATED READBACK SYSTEMS


+6
+5
9
4
8
10
529
1
7
Q
1
4
8
7
592
6
2
5
9
2
5
Q̄
3
6
47 pFd
-6
AMPLITUDE: 1-10 mV p-p
FREQUENCY: 1-4 MHz
READ HEAD
DIFFERENTIATOR/AMPLIFIER
ZERO CROSSING DETECTOR

DIFFERENTIATION WITH HIGH COMMON MODE NOISE REJECTION


+6
0.2μF
4
8
1
2KΩ
7
Vi
592
Vo
2
6
0.2μF
5
9
C
2KΩ
-6

FOR FREQUENCY $F_1 << 1/2\,\pi\,(32)\,C$

$V_0 \cong 1.4 \times 10^4 C \frac{dV_i}{dT}$

SECTION 3
VOLTAGE REGULATORS

Section 3—VOLTAGE REGULATORS

NE/SE5553	Dual Polarity Regulator	95
NE/SE5554	Dual Polarity Regulator	95
NE/SE550	Precision Adjustable Regulator	99
μA723/723C	Precision Voltage Regulator	*
NE/SE5560	Switched Mode Power Supply Controller	106
SG1524	Regulating Pulse Width Modulator	110
SG2524	Regulating Pulse Width Modulator	110
SG3524	Regulating Pulse Width Modulator	110
μA78HV12	Three Terminal Positive Voltage Regulator	*
μA78HV12C	Three Terminal Positive Voltage Regulator	*
μA78HV15	Three Terminal Positive Voltage Regulator	*
μA78HV15C	Three Terminal Positive Voltage Regulator	*
μA78HV24	Three Terminal Positive Voltage Regulator	*

NOTE

*Any product listed in this section but not incorporated within the text may be obtained by writing Information Services at Signetics, 811 E. Arques, M/S 027, Sunnyvale, California 94086, or by calling (408) 746-1682.

VOLTAGE REGULATOR DEFINITIONS

T_A

Ambient temperature range. Range of the surrounding environment of the operating device.

T_J

Junction Temperature. The maximum temperature of the device. 150°C is standard for silicon devices.

T_{STG}

Storage temperature range. Temperature range that the device can be stored in a non-operating condition.

T_{SOLD}

Soldering Temperature. The temperature which can be applied to the lead frame of the device for short periods of time (normally specified for a duration of 10 sec).

Truth Tables

0 is logic level low
1 is logic level high
X - don't care condition - has no effect under circuit conditions listed.

Absolute Maximum Rating

Operating safe zones exceeding these limits could cause permanent damage to the device and are not meant to imply that devices can operate at these limits.

Power Dissipation

The power that the device can safely handle at 25°C. The dissipation must be derated as indicated for the individual package type.

Package Type Designation

See full package designations in Appendix.

V_{CC} ($-V_{CC}$)

Supply Voltage. The range of power supply voltage over which the device will operate safely.

Line Regulation

Sometimes referred to as "static regulation". This term refers to the changes in the output as the input is varied slowly from its rated minimum value to its rated maximum value (from 105 VAC_{RMS} to 125 VAC_{RMS}). Measured in mv/V.

Load Regulation

Sometimes referred to as "dynamic regulation". This term refers to the changes in the output when load conditions are suddenly changed (from no load to full load). Measured in mv/V.

Thermal Regulation

Referred to as changes due to ambient variations or thermal drift. Also referred to as temperature coefficient, measured in ppm/°C or mv/°C.

Transient Response

The ability of a regulator to respond to rapid changes in line variations, load variations, or intermittent transient input conditions. (Transient Response is often referred to as "recovery time"). Measured in milliseconds (ms).

Voltage Limiting

The ability of the regulator to "shut down" in the event that the internal reference sources fail to function properly. Measured in Volts.

Current Limiting

The ability of the amplified segment to limit the output current of the device when safe operating limits are exceeded. Measured in amperes (pre-determined).

Thermal Shutdown

The ability of the regulator to shut itself down when the maximum die temperature is exceeded. Measured in degrees Celsius (C).

Power Dissipation

The ability of the regulator to tolerate excessively high levels of input power while maintaining its operation within the safe operating area of its active devices. Measured in watts.

Efficiency

Regarding a regulator, the ratio of the total power input to the usable power output. Expressed as a percentage. (For example, if a regulator has a 50 watt input and a 40 watt output, its efficiency is 80 percent).

EMI/RFI

("Electromagnetic Interference/Radio Frequency Interference") regarding regulators, magnetic field disturbance and radio frequency interference signals generated especially by SMPS devices. Measurement is generally unspecified.

Safe Operating Area Restriction (SOAR)

Limits the output current of the amplifier to maintain safe (no thermal runaway) operating conditions. (Accomplished through internal sensor amplifiers).

NOTE
Refer to Section 4 of Analog Applications Manual for an in-depth explanation of Voltage Regulators

DUAL TRACKING VOLTAGE REGULATOR

COMPETITION	INDUSTRY VALUE	KEY PARAMETER	SIGNETICS AVAILABLE VALUE	SIGNETICS ORIGINATED DEVICES	QR&A		COMMENTS
					SURE II	SUPR II	
NATIONAL MOTOROLA RAYTHEON		Line Regulator	1 %	SE/NE 555X	Yes		I_{OUT} 400mA
LM125, −6, −7	0.1 %	Line Regulator	0.25 %				
Raytheon 4194	±.05 to ±40	V_{OUT}	± 5 to ±20 Volts	SE/NE 5553/4	Yes		
Motorola 1568	100 mA	I_{OUT}	±400 mA	SE/NE 5553/4			
		Package Power Dissipation	8 Watts	SE NE 5553/4 Series in SIL-9 package			

OBJECTIVE SPECIFICATION

NE/SE5553/5554-N,H,U

DESCRIPTION

The NE/SE5553,4 are dual polarity tracking regulators designed to produce balanced or unbalanced output voltages from 5 to 20 volts with up to 300 mA output current. Similar in specifications to the 78MXX and 79MXX fixed regulators, the 5551 series can be continuously adjusted, balanced or unbalanced. Standard fixed voltages available are ±5, ±6, ±12, ±15, and +5, -12 volts. Employing current limiting and thermal shutdown protection, these dual polarity regulators are ideal for local on-card regulation.

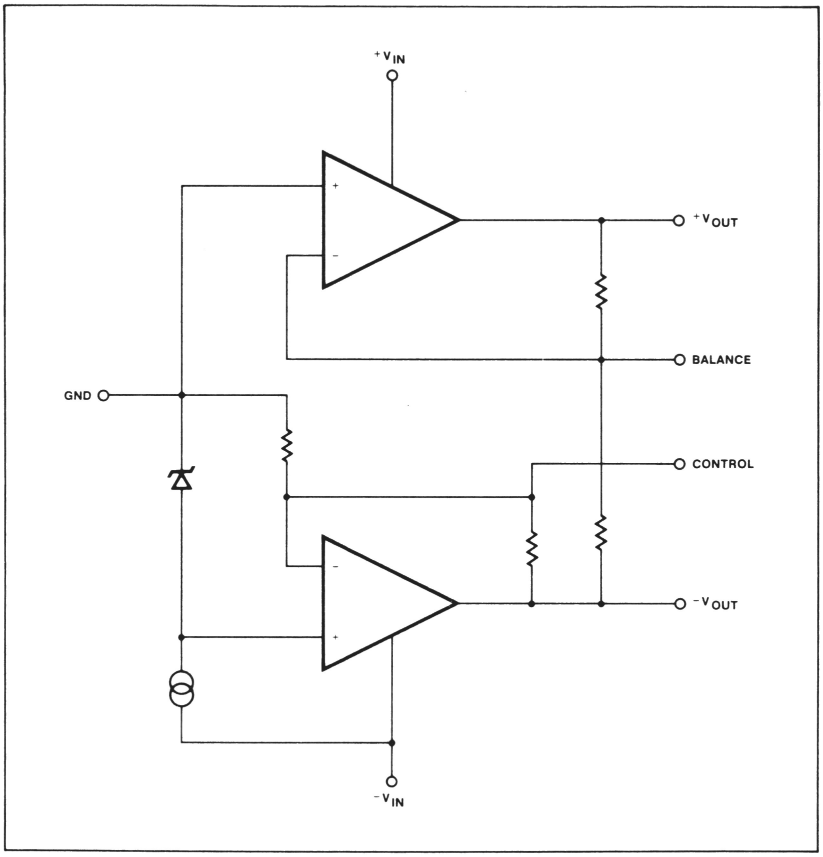
FEATURES

- **Output current to 300mA**
- **Internally current limited**
- **Thermal overload protected**
- **Input voltage to ±32V**
- **Output balance 1% typ.**
- **External balance control**
- **Continuously adjustable from 5 to 20 volts, balanced or unbalanced**
- **No external components required**
- **Short circuit current 400mA**
- **Heat sink available for increased power dissipation**

ABSOLUTE MAXIMUM RATINGS

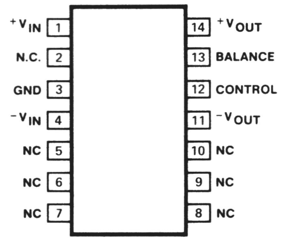
PARAMETER	RATING	UNIT
V_{IN} input voltage	±32	V
T_{SG} storage temperature	-65 to +150	°C
T_J operating junction temperature		
NE5553,4	0 to +125	°C
SE5553,4	-55 to +150	°C
Lead temperature 10 sec.	300	°C

BLOCK DIAGRAM


+VIN
+
-
+VOUT
BALANCE
GND
CONTROL
-
+
-VOUT
-VIN

PIN CONFIGURATIONS

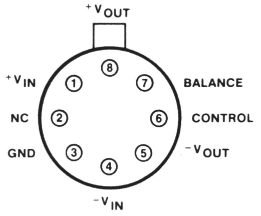
N PACKAGE


+VIN 1
N.C. 2
GND 3
-VIN 4
NC 5
NC 6
NC 7
14 +VOUT
13 BALANCE
12 CONTROL
11 -VOUT
10 NC
9 NC
8 NC

ORDER PART NUMBERS

VOLTAGE	PART NO.
±12V	SE/NE5553N
±15V	SE/NE5554N

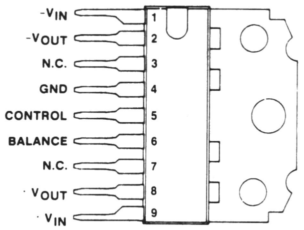
H PACKAGE


+VOUT
+VIN
1
8
7
BALANCE
NC
2
6
CONTROL
GND
3
4
5
-VOUT
-VIN

ORDER PART NUMBERS

VOLTAGE	PART NO.
±12V	SE/NE5553H
±15V	SE/NE5554H

U PACKAGE


-VIN 1
-VOUT 2
N.C. 3
GND 4
CONTROL 5
BALANCE 6
N.C. 7
+VOUT 8
+VIN 9

ORDER PART NUMBERS

VOLTAGE	PART NO.
±12V	SE/NE 5553 U
±15V	SE/NE 5554 U

Power dissipation (without heat sink)

H Package: Θ_{JC} = 20°C/W Θ_{JA} = 150°

N Package: Θ_{JC} = 33°C/W Θ_{JA} = 95°

U Package: Θ_{JC} = 30°C/W Θ_{JA} = 62°

DC ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	SE5553			NE5553			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage		+11.5 -12.5	+12 -12	+12.5 -11.5	+11.5 -12.5	+12 -12	+12.5 -11.5	V
	Line regulation	$\pm20 \leq V_{IN} \leq \pm30V$		100	150		100	300	mV
	Load regulation	$1mA \leq I_{Load} \leq 50mA$		10	25		10	50	mV
		$1mA \leq I_{Load} \leq 200mA$		30	100		30	200	mV
V_{OUT}	Output voltage	$1mA \leq I_L \leq 100mA$ $\pm20V \leq V_{IN} \leq \pm30V$ over temp.1	+11.4 -12.6	+12 -12	+12.6 -11.4	+11.4 -12.6	+12 -12	+12.6 -11.4	V V
I_Q+	Positive quiescent current	$I_{Load} = 0$		1.70	3.5		1.70	3.5	mA
I_Q-	Negative quiescent current	$I_{Load} = 0$		5.60	8.5		5.60	8.5	mA
	Input/output differential voltage			2.5			2.5		V
V_{BAL}	Output voltage balance			.2			.2		V
	Output noise voltage	100Hz to 10kHz		55			55		μVrms
I_{Peak}	Peak output current			400			400		mA
	Temperature stability of output voltage			1			1		mV/°C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) $V_{IN} = \pm20V$, $I_L = 100mA$, $T_J = 25°C$, $C_{IN} = C_{OUT} = 0.1\mu F$ unless otherwise specified.

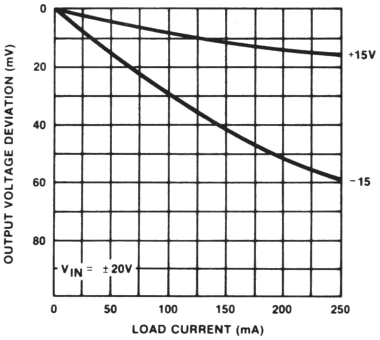
PARAMETER		TEST CONDITIONS	SE5554			NE5554			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage		+14.4 -15.6	+15 -15	+15.6 -14.4	+14.4 -15.6	+15 -15	+15.6 -14.4	V
	Line regulation	$\pm20 \leq V_{IN} \leq \pm30V$		100	150		100	300	mV
	Load regulation	$1mA \leq I_{Load} \leq 50mA$		10	25		10	50	mV
		$1mA \leq I_{Load} \leq 200mA$		30	100		30	200	mV
V_{OUT}	Output voltage	$1mA \leq I_L \leq 100mA$ $\pm20V \leq V_{IN} \leq \pm30V$ over temp.1	+14.25 -15.75	+15 -15	+15.75 -14.25	+14.25 -15.75	+15 -15	+15.75 -14.25	V V
I_Q+	Positive quiescent current	$I_{Load} = 0$		1.70	3.5		1.70	3.5	mA
I_Q-	Negative quiescent current	$I_{Load} = 0$		5.60	8.5		5.60	8.5	mA
	Input/output differential voltage			2.5			2.5		V
V_{BAL}	Output voltage balance			.2			.2		V
	Output noise voltage	100Hz to 10kHz		55			55		μVrms
I_{Peak}	Peak output current			400			400		mA
	Temperature stability of output voltage			1			1		mV/°C

NOTES

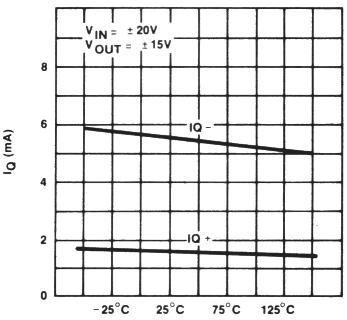
1. Junction temperature range
   SE prefix $-55°C < T_J < 150°C$
   NE prefix $0°C < T_J < 125°C$
2. C_{IN} needed only when isolated from filter capacitors
   C_{OUT} needed only if dynamic regulation is to be improved.
3. Thermal resistance, DIP
   $\theta_{JA} = 95°C/W$ $\theta_{JC} = 35°C/W$, TO-5
   $\theta_{JA} = 150°C/W$ $\theta_{JC} = 25°C/W$
   SIL $\theta_{JA} = 62.4°C/w$ $\theta_{JC} = 30°C/w$

TYPICAL PERFORMANCE CHARACTERISTICS

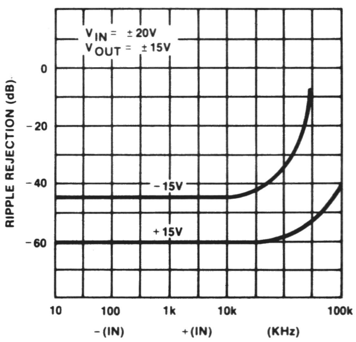
LOAD REGULATION



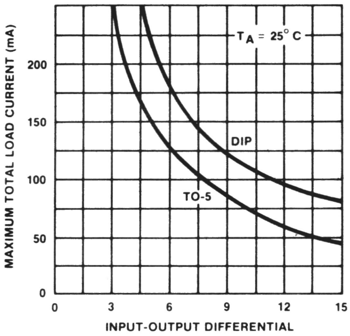
IQ +, IQ -



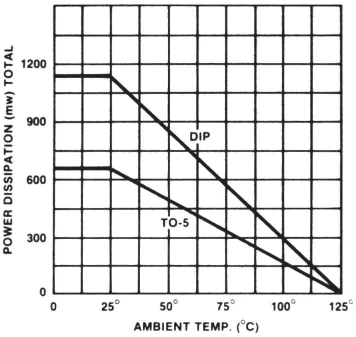
RIPPLE REJECTION



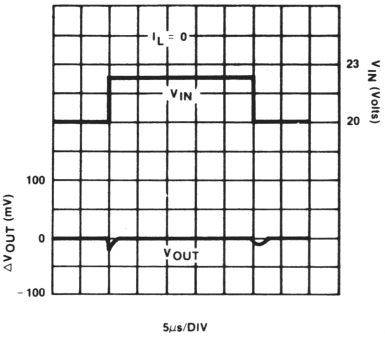
MAXIMUM CURRENT CAPABILITY



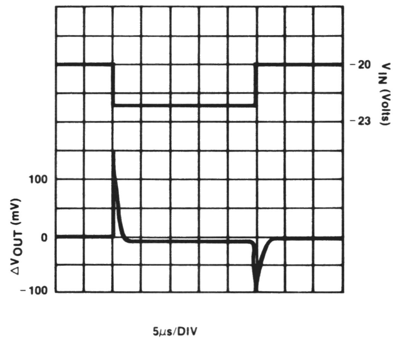
MAXIMUM POWER DISSIPATION[4]



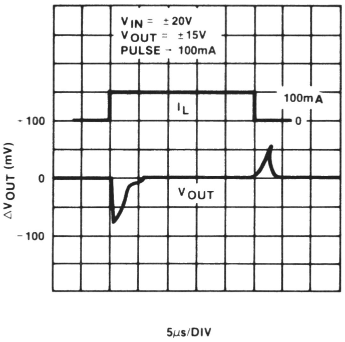
LINE TRANSIENT RESPONSE, POSITIVE



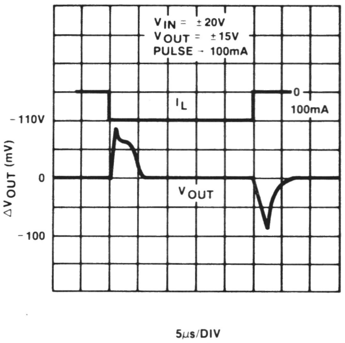
LINE TRANSIENT RESPONSE, NEGATIVE



LOAD TRANSIENT RESPONSE, POSITIVE



LOAD TRANSIENT RESPONSE, NEGATIVE



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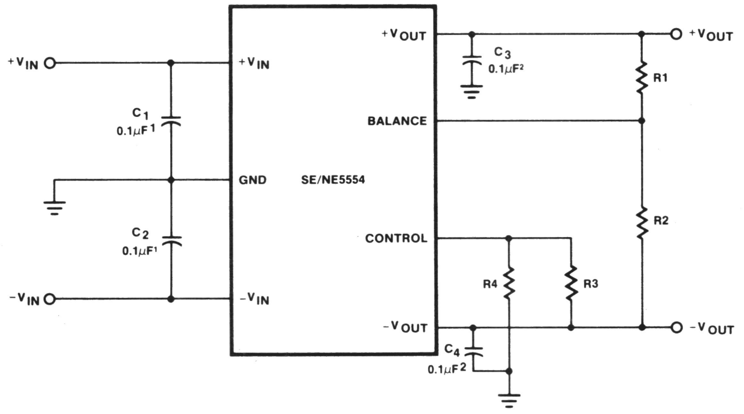
4. Device capability in free air.

BLOCK DIAGRAM

TYPICAL CONNECTION


+VOUT
+VOUT
C3
0.1µF2
+VIN
+VIN
R1
C1
0.1µF 1
BALANCE
GND
SE/NE5554
R2
C2
0.1µF1
CONTROL
R4
R3
-VIN
-VIN
-VOUT
-VOUT
C4
0.1µF 2

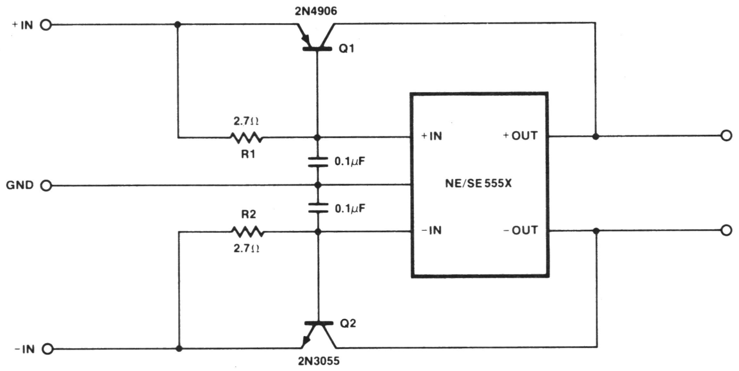
R1 and R2 adjust $+V_{OUT}$
with respect to $-V_{OUT}$
R3 and R4 adjust $-V_{OUT}$
From -5V to -20V

NOTES

1. Required if regulator is operated any distance from filter capacitor.
2. Not required for stability, but improves dynamic regulation.

TYPICAL APPLICATIONS

HIGH CURRENT TRACKING REGULATOR


2N4906
+IN
Q1
2.7Ω
R1
+IN
+OUT
0.1µF
GND
NE/SE 555X
0.1µF
R2
2.7Ω
-IN
-OUT
Q2
-IN
2N3055

$$R1 = R2 = \frac{V_{BE}}{I_{REG}(max)\ (\beta + 1) - I_{out}(max)}$$

For

$$\beta(Q) \geq \frac{I_{out\ (max)}}{I_{reg\ (max)}}$$

DESCRIPTION

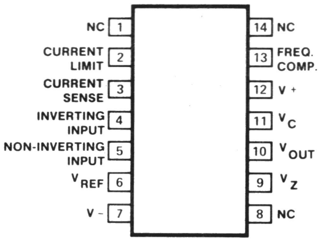
The 550 is a precision monolithic voltage regulator capable of positive or negative supply operation as series, shunt, switching or floating regulator. Guaranteed line regulation is provided for input voltages ranging from 8.5 volts to as high as 50 volts. The output voltage can be continuously adjusted from 2 volts to 40 volts. Foldback current limiting can be accomplished through the use of one external resistor. Internal circuitry permits on and off strobing with DTL and TTL logic inputs and latched shut-down with a pulsed input.

FEATURES

- **Line regulation guaranteed over input voltage range of 8.5 volts to as high as 50 volts.**
- **Output voltage continuously adjustable from 2 volts to 40 volts**
- **.01% line and load regulation**
- **Adjustable limiting of short circuit current**
- **Foldback current limiting with one external resistor**
- **Remote and latching shutdown**
- **Output current up to 150mA without external power transistors**

PIN CONFIGURATIONS

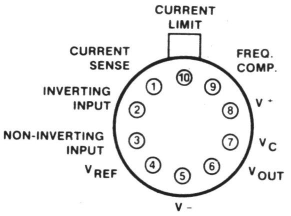
F,N PACKAGE


NC 1
CURRENT LIMIT 2
CURRENT SENSE 3
INVERTING INPUT 4
NON-INVERTING INPUT 5
VREF 6
V- 7
14 NC
13 FREQ. COMP.
12 V+
11 VC
10 VOUT
9 VZ
8 NC

ORDER PART NO.

SE550F	NE550N
SE550F	NE550F

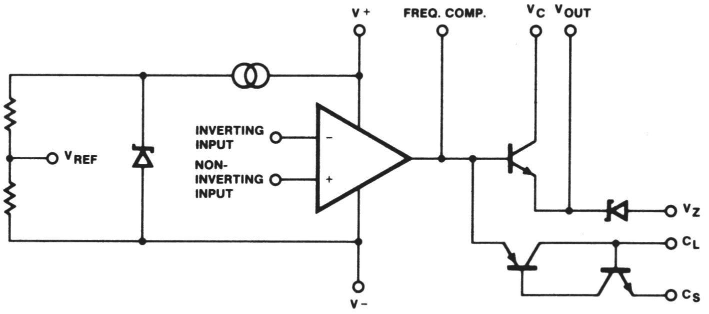
H PACKAGE


CURRENT LIMIT
FREQ. COMP.
CURRENT SENSE
INVERTING INPUT
NON-INVERTING INPUT
VREF
V+
VC
VOUT
V-
1
2
3
4
5
6
7
8
9
10

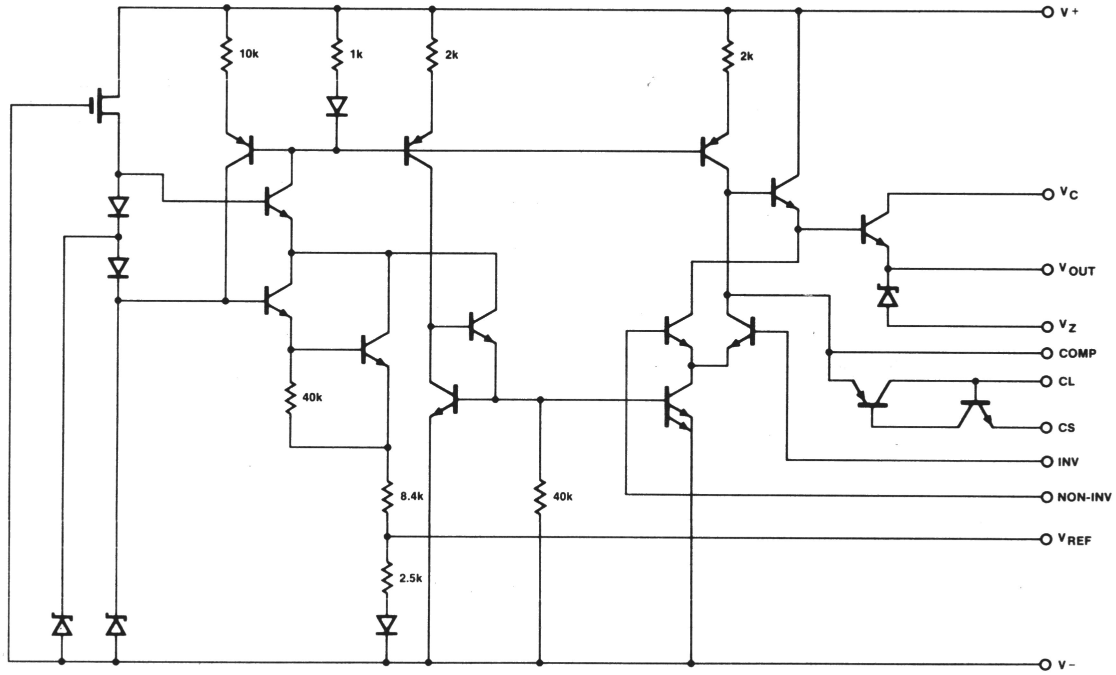
ORDER PART NO.

SE550H NE550H

CIRCUIT SCHEMATIC


V+
FREQ. COMP.
VC
VOUT
VREF
INVERTING INPUT
NON-INVERTING INPUT
-
+
VZ
CL
CS
V-

EQUIVALENT CIRCUIT


V+
10k
1k
2k
2k
VC
VOUT
VZ
COMP
CL
CS
INV
NON-INV
VREF
V-
40k
8.4k
40k
2.5k

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Voltage from V+ to V-		
SE550	50	V
NE550	40	V
Input-output voltage differential		
SE550	45	V
NE550	37	V
Maximum output current		
SE550	150	mA
NE550	150	mA
Current from V_Z		
SE550	15	mA
NE550	15	mA
Internal power dissipation[1]		
SE550	800	mW
NE550	800	mW
Operating temperature range		
SE550	-55 to +125	°C
NE550	0 to 70	°C
Storage temperature range		
SE550	-65 to +150	°C
NE550	-65 to +150	°C
Lead temperature		
SE550	300	°C
NE550	300	°C

NOTE

1. Rating applies for case temperatures to 125°C; derate linearly at 6.5mW/°C for ambient termperature above +75°C.

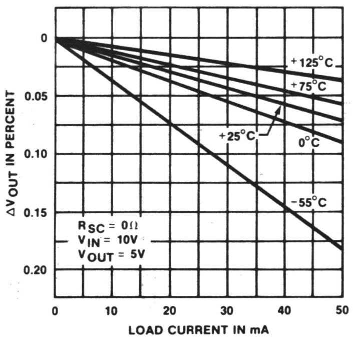
DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.[1,2]

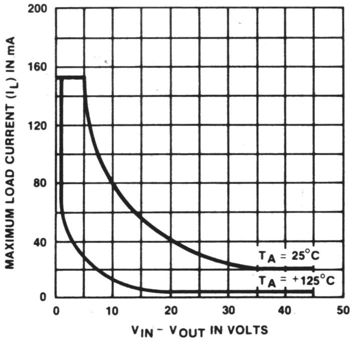
PARAMETER	TEST CONDITIONS	NE550			SE550			UNIT
		Min	Typ	Max	Min	Typ	Max	
Line regulation	$V_{IN} = 8.5$ to 40V		.08	0.3				%V_{OUT}
	$0°C \leq T_A \leq 70°C$, $V_{IN} = 12$ to 40V			0.35				%V_{OUT}
	$V_{IN} = 12$ to 40V					0.05	0.1	%V_{OUT}
	$V_{IN} = 8.5$ to 50V					0.2	0.6	%V_{OUT}
	$-55°C \leq T_A \leq +125°C$, $V_{IN} = 12$ to 40V						0.25	%V_{OUT}
Load regulation	$I_L = 1$mA to 50mA		.03	0.2		0.03	.10	%V_{OUT}
	$0°C \leq T_A \leq 70°C$			0.4				%V_{OUT}
	$-55°C \leq T_A \leq +125°C$						.6	%V_{OUT}
Ripple rejection	f = 50Hz to 10kHz							dB
	$C_{REF} = 0$		75			75		dB
	$C_{REF} = 5\mu F$		90			90		dB
Average temperature coefficient of output voltage	$-55° \leq T_A \leq +125°C$					.002	.012	%/°C
	$0°C \leq T_A \leq 70°$		.002	.015				%/°C
Short circuit limit	RSC = 10Ω, $V_{OUT} = 0$	50	60	70	50	60	70	mA
Reference voltage		1.58	1.63	1.73	1.58	1.63	1.68	V
Output noise voltage	BW = 100Hz to 10kHz, $C_{REF} = 0$		20			20		μVrms
	BW = 100Hz to 10kHz, $C_{REF} = 5\mu F$		2.5			2.5		μVrms
Long term stability						0.1		%/1000hrs.
Standby current drain	$I_L = 0$, $V_{IN} = 50V$					1.3	2.0	mA
	$I_L = 0$, $V_{IN} = 40V$		1.6	3.0				mA
Input voltage range		8.5		40	8.5		50	V
Output voltage range		2.0		40	2.0		37	V
Input-output voltage differential		3.0		38	3.0		45	V

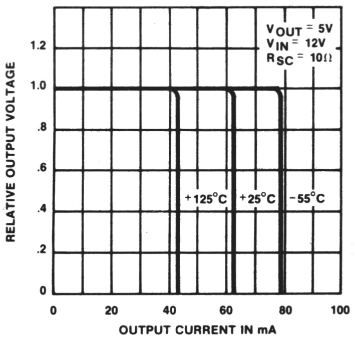
NOTES

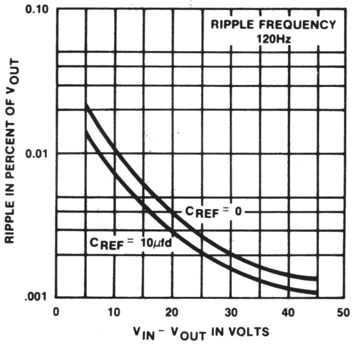
1. $V_{IN} = V+ = V_C = 12V$, $V- = 0V$, $V_{OUT} = 5V$, $I_L = 1mA$, $R_{SC} = 0_1CI = 100pF$, and divider impedance as seen by error amplifier ≃ 2kΩ.
2. The load and line regulation specifications are for constant temperature junction. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high or varying dissipation.

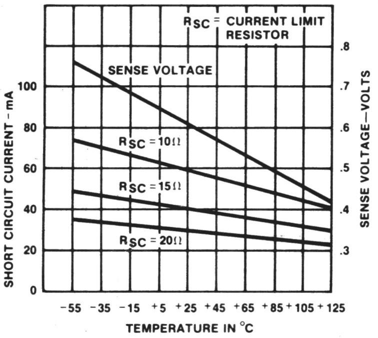
TYPICAL PERFORMANCE CHARACTERISTICS

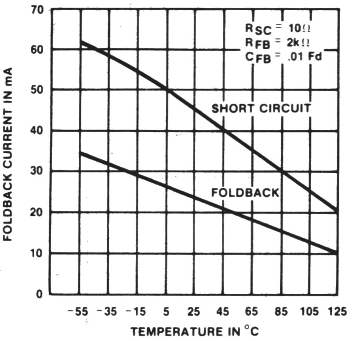

LOAD REGULATION AS A FUNCTION OF LOAD CURRENT

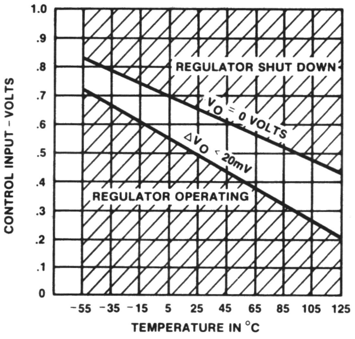

MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

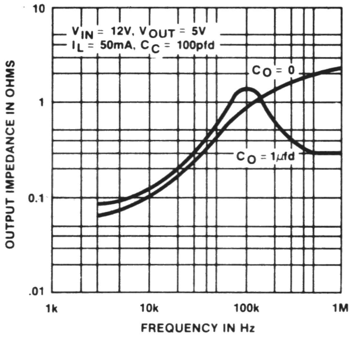

RELATIVE OUTPUT VOLTAGE AS A FUNCTION OF LIMITED OUTPUT CURRENT

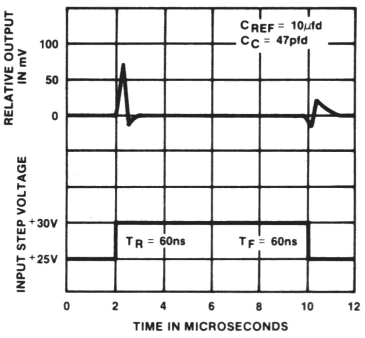

RIPPLE REJECTION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL


SENSE VOLTAGE AND SHORT CIRCUIT CURRENT LIMIT AS A FUNCTION OF TEMPERATURE


SHORT CIRCUIT AND FOLDBACK CURRENTS AS A FUNCTION OF TEMPERATURE

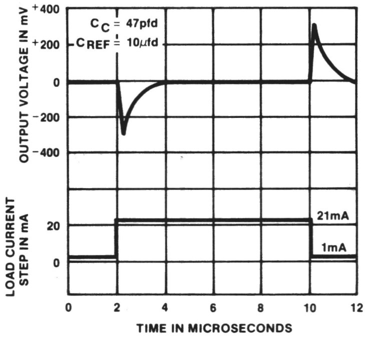

REMOTE CONTROL CHARACTERISTICS AS A FUNCTION OF TEMPERATURE


OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY

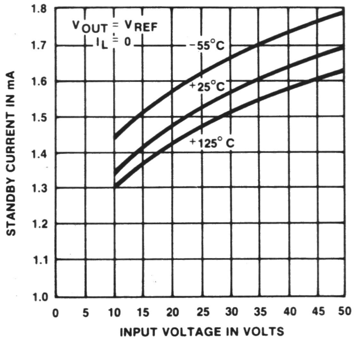

LINE TRANSIENT RESPONSE

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

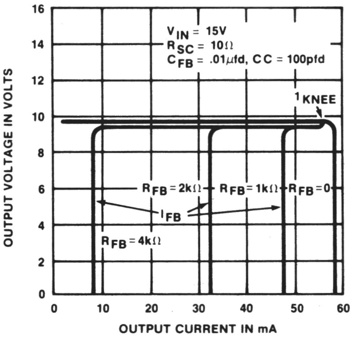
LOAD TRANSIENT RESPONSE



STANDBY CURRENT AS A FUNCTION OF INPUT VOLTAGE

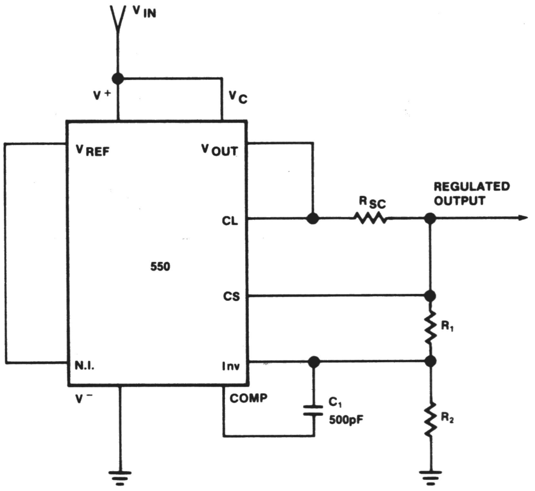


FOLDBACK CURRENT LIMITED OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



TYPICAL APPLICATIONS

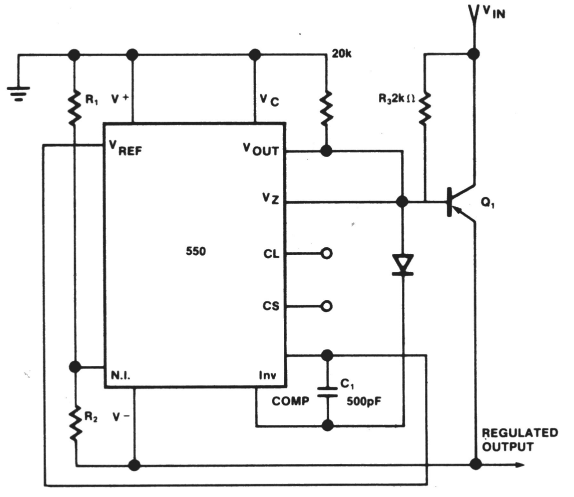
BASIC POSITIVE VOLTAGE REGULATOR


V_{IN}
V^+
V_C
V_{REF}
V_{OUT}
CL
550
CS
N.I.
Inv
V^-
COMP
R_{SC}
REGULATED OUTPUT
R_1
C_1
500pF
R_2

$$V_{OUT} = V_{REF}\frac{R_1 + R_2}{R_2} \quad ISC = \frac{V_{SENSE}}{RSC}$$

$$\frac{R_1R_2}{R_1 + R_2} = 2k\Omega \text{ for minimum temperature drift}$$

NEGATIVE VOLTAGE REGULATOR


V_{IN}
20k
R_1
V^+
V_C
$R_3$2kΩ
V_{REF}
V_{OUT}
V_Z
Q_1
550
CL
CS
N.I.
Inv
C_1
COMP
500pF
R_2
V^-
REGULATED OUTPUT

$$V_{OUT} = -V_{REF}X\frac{R_1 + R_2}{R_2}$$

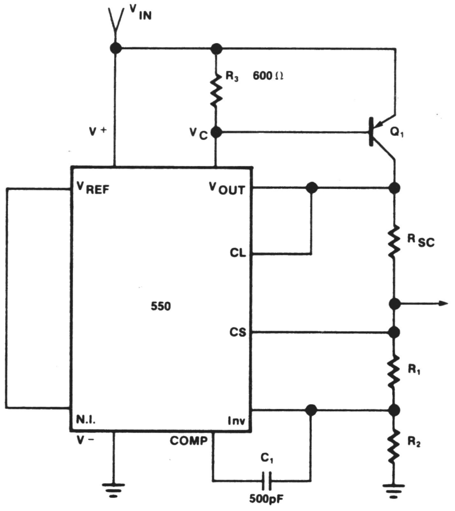
$$\frac{R_1R_2}{R_1 + R_2} = 2k\Omega \text{ for minimum temperature drift}$$

NOTE

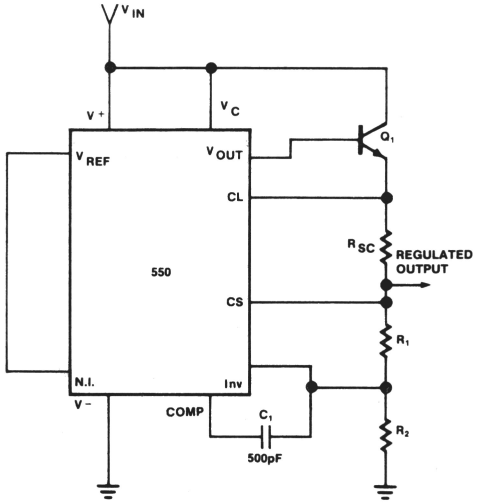
To utilize the SE550L in applications which require Vz, an external 6.2 volt zener diode should be connected in series with V_{OUT}.

TYPICAL APPLICATIONS (Cont'd)

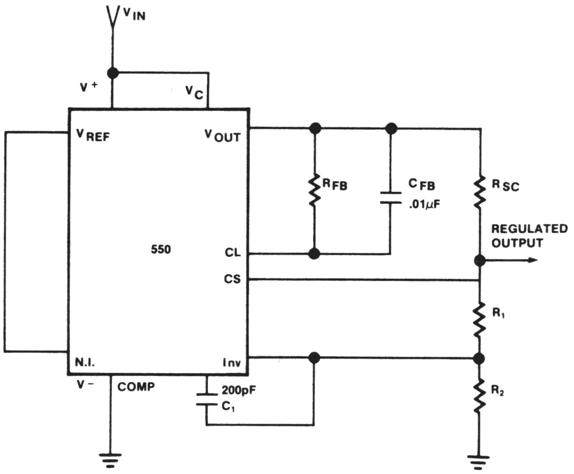
POSITIVE VOLTAGE REGULATOR (External PNP Pass Transistor)


V IN
R3 600 Ω
V+
VC
Q1
VREF
VOUT
CL
550
CS
N.I.
Inv
V−
COMP
RSC
R1
R2
C1
500pF

POSITIVE VOLTAGE REGULATOR (External NPN Pass Transistor)


V IN
V+
VC
Q1
VREF
VOUT
CL
550
CS
N.I.
Inv
V−
COMP
C1
500pF
RSC
REGULATED OUTPUT
R1
R2

FOLDBACK CURRENT LIMITED REGULATOR

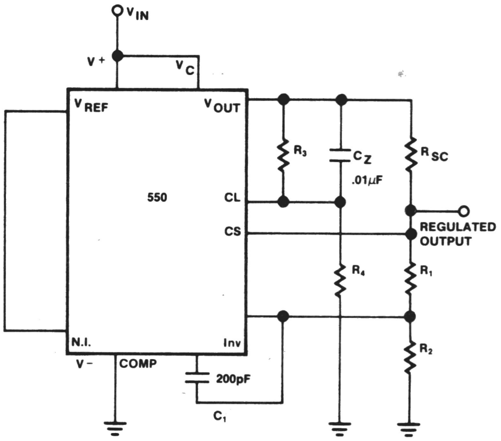

V IN
V+
VC
VREF
VOUT
550
CL
CS
N.I.
Inv
V−
COMP
200pF
C1
RFB
CFB
.01µF
RSC
REGULATED OUTPUT
R1
R2

$$I_{KNEE} = \frac{V_{SENSE}}{R_{SC}}$$

$$I_{FB} = \frac{V_{SENSE} - (R_{FB} - I_{CL})}{R_{SC}}$$

$I_{CL} = 125\mu A$

SECOND ORDER FOLDBACK CURRENT LIMITED REGULATOR


V IN
V+
VC
VREF
VOUT
550
CL
CS
N.I.
Inv
V−
COMP
200pF
C1
R3
CZ
.01µF
R4
RSC
REGULATED OUTPUT
R1
R2

$$R_3 = \frac{V_{SENSE}\,(I_{KNEE} - I_{FB})\,V_{OUT}}{I_{CL}\,(I_{KNEE} - I_{FB} + I_{SC})\,V_{OUT} - (I_{FB} - I_{SC})\,V_{SENSE}}$$

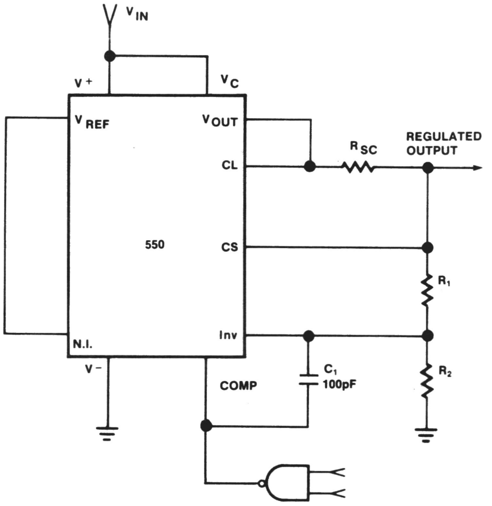
$$\frac{R_3}{R_4} = \frac{(V_{SENSE} - I_{CL}\,R_3)\,(I_{FB} - I_{SC})}{V_{OUT}\,I_{SC} - V_{SENSE}\,(I_{FB} - I_{SC})}$$

$$R_{SC} = \frac{(V_{OUT} + V_{SENSE})\,R_3/R_4 + V_{SENSE}}{I_{KNEE}}$$

$I_{CL} = 125\mu A$

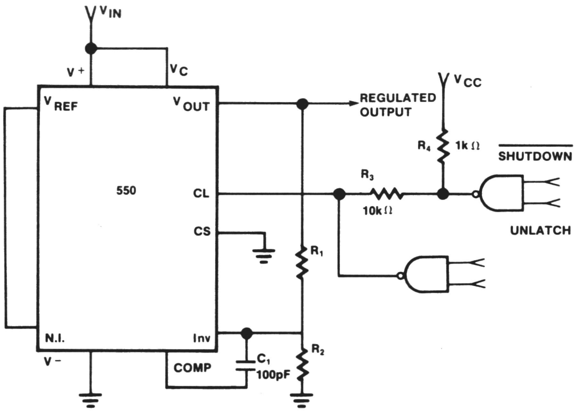
TYPICAL APPLICATIONS (Cont'd)

REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING


V IN
V+
VC
VREF
VOUT
CL
RSC
REGULATED OUTPUT
550
CS
R1
N.I.
Inv
V−
COMP
C1 100pF
R2

1/4 8T80, 1/6 8T90, 1/10 8TO1B, etc.

REMOTE LATCHING SHUTDOWN REGULATOR

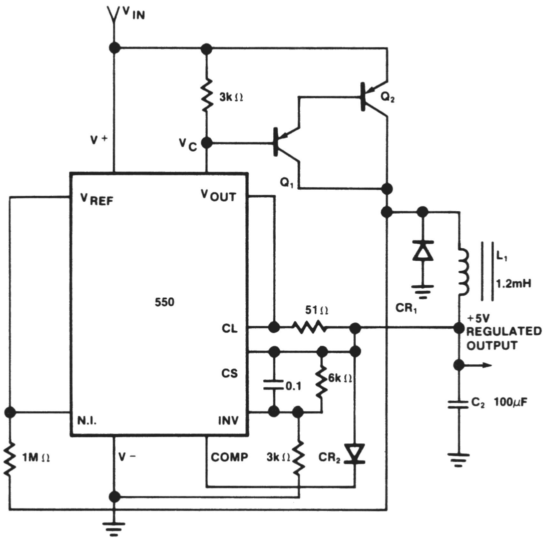

V IN
V+
VC
VREF
VOUT
REGULATED OUTPUT
V CC
R4
1k Ω
SHUTDOWN
550
CL
R3
10k Ω
CS
R1
UNLATCH
N.I.
Inv
V−
COMP
C1 100pF
R2

8415, 8417, 2/3 8471, 1/3 8891, 8T90, 1/2 8481, 8881, 8T90

NOTE

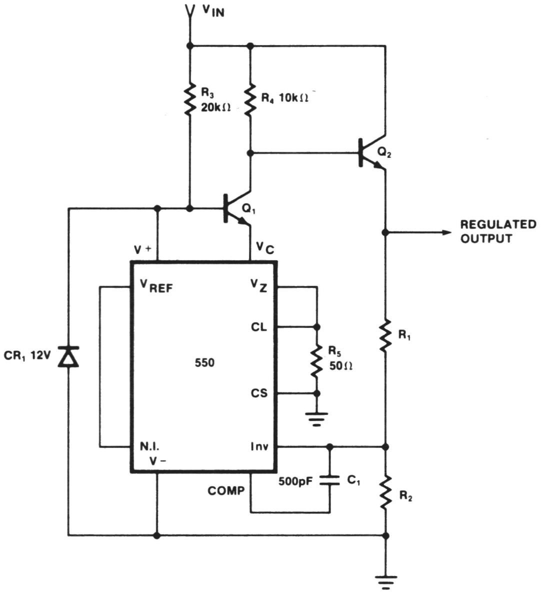
The "Shut-down" gate need only be pulsed to latch the regulator output to zero. R4 may omitted for active pull-up devices. The "Unlatch" gate must have an open collector.

POSITIVE SWITCHING REGULATOR


V IN
3k Ω
Q2
V+
VC
Q1
VREF
VOUT
550
CR1
L1 1.2mH
CL
51 Ω
+5V REGULATED OUTPUT
CS
0.1
6k Ω
C2 100μF
N.I.
INV
1M Ω
V−
COMP
3k Ω
CR2

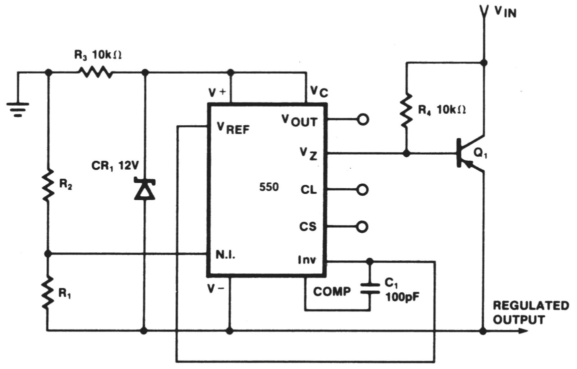
L₁ is 50 turns of #22 wire wound on Ferroxcube. 42/29-377 A400

POSITIVE FLOATING REGULATOR


V IN
R3 20k Ω
R4 10k Ω
Q2
Q1
REGULATED OUTPUT
V+
VC
VREF
VZ
CL
R5 50 Ω
CR1 12V
550
R1
CS
N.I.
V−
Inv
COMP
500pF
C1
R2

TYPICAL APPLICATIONS (Cont'd)

NEGATIVE FLOATING REGULATOR


VIN
R3 10kΩ
V+
VC
VREF
VOUT
VZ
R4 10kΩ
Q1
CR1 12V
R2
550
CL
CS
N.I.
Inv
R1
V−
COMP
C1
100pF
REGULATED
OUTPUT

SWITCHED-MODE POWER SUPPLY CONTROL CIRCUIT NE/SE5560

NE/SE5560-F,N

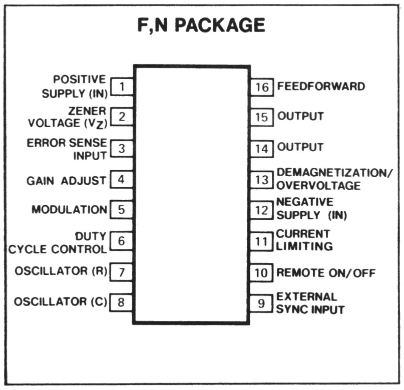
DESCRIPTION

The NE/SE5560 is a control circuit for use in switched mode power supplies. This single monolithic chip incorporates all the control and housekeeping (protection) functions required in switched mode power supplies, including an internal temperature compensated reference source, internal Zener reference, sawtooth generator, pulse width modulator, output stage and various protection circuits.

FEATURES

- **Stabilized power supply**
- **Temperature compensated reference source**
- **Sawtooth generator**
- **Pulse width modulator**
- **Remote on/off switching**
- **Current limiting**
- **Low supply voltage protection**
- **Loop fault protection**
- **Demagnetization/overvoltage protection**
- **Maximum duty cycle adjustment**
- **Feed forward control**
- **External synchronization**

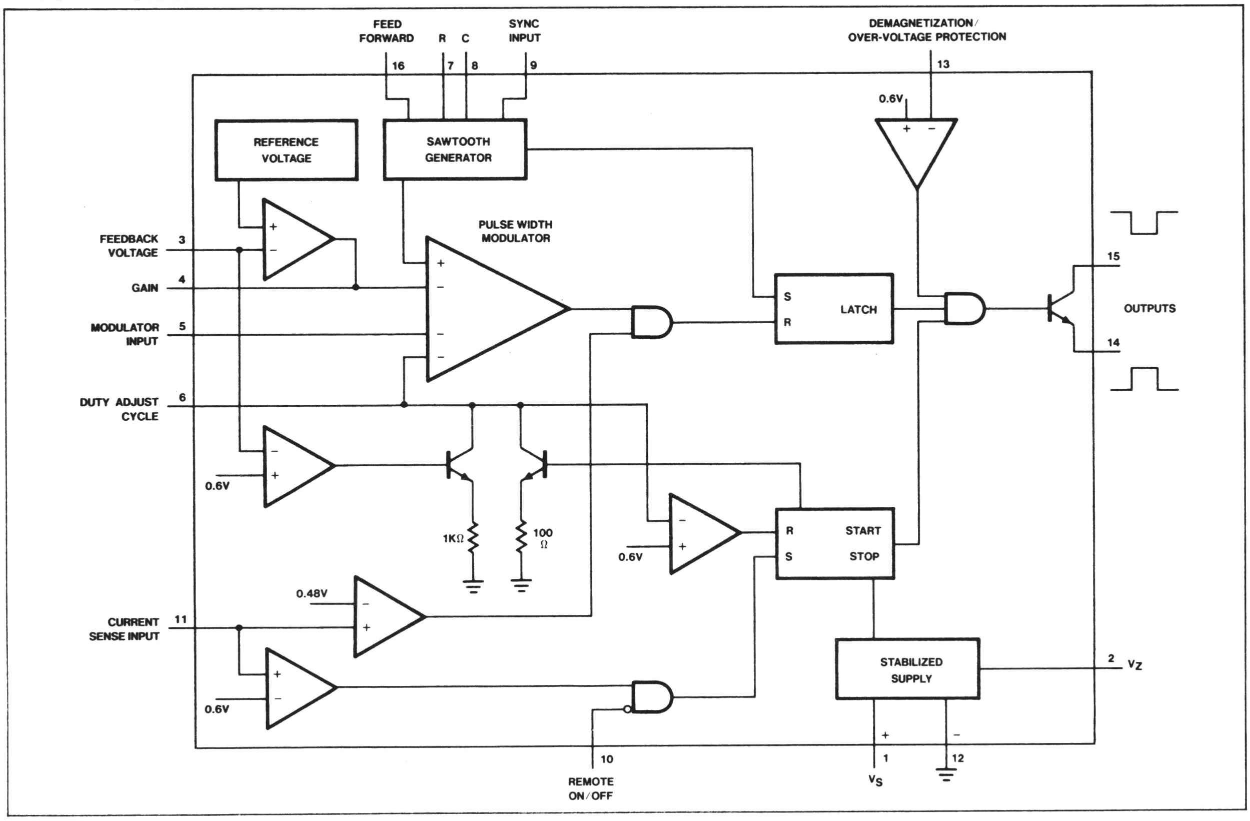
PIN CONFIGURATION


F,N PACKAGE
POSITIVE SUPPLY (IN) 1
ZENER VOLTAGE (VZ) 2
ERROR SENSE INPUT 3
GAIN ADJUST 4
MODULATION 5
DUTY CYCLE CONTROL 6
OSCILLATOR (R) 7
OSCILLATOR (C) 8
16 FEEDFORWARD
15 OUTPUT
14 OUTPUT
13 DEMAGNETIZATION/OVERVOLTAGE
12 NEGATIVE SUPPLY (IN)
11 CURRENT LIMITING
10 REMOTE ON/OFF
9 EXTERNAL SYNC INPUT

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage (Voltage sourced)	+18	V
Supply current (Current sourced)	30	mA
Output current	40	mA
Operating temperature range (ambient)		
SE5560	−55 to +125	°C
NE5560	0 to +70	°C
Storage temperature range	−65 to +150	°C

BLOCK DIAGRAM


FEED FORWARD
R
C
SYNC INPUT
16
7
8
9
DEMAGNETIZATION/ OVER-VOLTAGE PROTECTION
13
0.6V
REFERENCE VOLTAGE
SAWTOOTH GENERATOR
PULSE WIDTH MODULATOR
FEEDBACK VOLTAGE 3
GAIN 4
MODULATOR INPUT 5
DUTY ADJUST CYCLE 6
LATCH
S
R
15
OUTPUTS
14
0.6V
1KΩ
100 Ω
0.6V
R START
S STOP
0.48V
CURRENT SENSE INPUT 11
0.6V
STABILIZED SUPPLY
2 VZ
10
REMOTE ON/OFF
+
−
1
12
VS

DC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 12V unless otherwise specified

PARAMETER	TEST CONDITIONS	SE5560			NE5560			UNIT
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTIONS	Over temp.	3.42		4.04	3.38		4.07	V
Internal reference voltage (V_{ref})	25°C	3.45	3.72	4.0	3.4	3.72	4.05	V
Internal Zener reference (V_Z)	I_L = 7mA	7.8	8.4	9.0	7.8	8.4	9.0	V
Temperature coefficient of V_{ref}				± 100		± 100		ppm/°C
Temperature coefficient of V_Z			± 150			± 150		ppm/°C
OSCILLATOR SECTION								
Frequency range	Over temp.	50		100K	50		100K	Hz
Initial accuracy	R = 5K		5			5		%
Duty cycle range[1]	fo = 20kHz	0		98	0		98	%
MODULATOR								
Modulator input current	Voltage at Pin 5 = 1V over temp.		0.2	20		0.2	20	μA
HOUSEKEEPING FUNCTION								
Pin 6 Duty cycle limit control	(For 50% Maximum duty cycle) 15kHz to 50kHz	38	40	42	37	40	43	% of V_Z
Pin 6 Input current	Over temp.		.2	20		0.2	20	μA
Pin 1 Low supply voltage protection thresholds		V_Z+.2	V_Z+7V	V_Z +1.7V	V_Z+.2	V_Z+.7	V_Z+1.7	V
Pin 3 Feedback loop protection trip on threshold		470	600	720	470	600	720	mV
Pin 3 Pull up current	Over temp.		−15	−35		−15	−35	μA
Pin 13 Demagnetization/over voltage protection trip on threshold		470	600	720	470	600	720	mV
Pin 13 Input current	Over temp.		0.6	10		0.6	10	μA
	25°C			20			20	μA
Pin 16 Feed forward duty cycle[2] control	Voltage at Pin 16 = 2V_Z		0.4			0.4		original duty cycle
Feed forward input current			0.2	5		0.2	5	μA
	Over temp. 25°C			10			10	μA
EXTERNAL SYNCHRONIZATION								
Pin 9 off		0		0.8	0		0.8	V
on		2		V_Z	2		V_Z	V
Sink current	Voltage at Pin 9 = 0_V 25°C		−65	−100		−65	−125	μA
	Over temp.			−125			−125	μA
REMOTE								
Pin 10 off		0		0.8	0		0.8	V
on		2		V_Z	2		V_Z	V
Sink current	25°C		−85	−100		−75	−125	μA
	Over temp.			−125			−125	μA
CURRENT LIMITING								
Pin 11; I_{IN}	Voltage at Pin 11 = 250mV, 25°C		−2	−10		−2	−10	μA
	Over temp.			−20			−20	
Single pulse inhibit delay	Inhibit delay time for 20% overdrive at 40mA I_{OUT}		0.7	0.8		0.7	0.8	μs
Trip Levels:								
Shut down/slow start		.500	.600	.700	.500	.600	.700	V
Current limit		.400	.48	.56	.400	.480	.560	V

NOTES

1. See graph
2. See graph

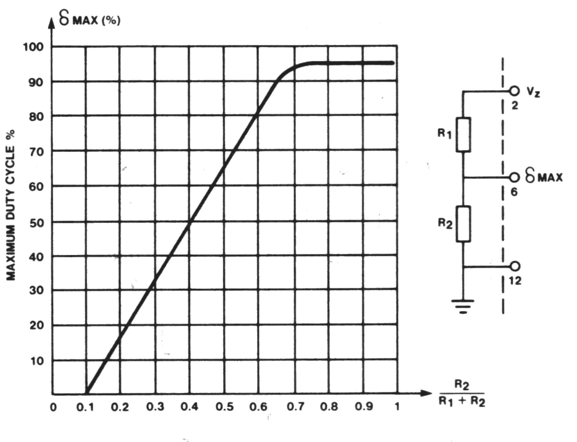
DC ELECTRICAL CHARACTERISTICS (Con't) $T_A = 25°C$, $V_{CC} = 12V$ unless otherwise specified

PARAMETER	TEST CONDITIONS	SE5560			NE5560			UNIT
		Min	Typ	Max	Min	Typ	Max	
ERROR AMPLIFIER								
Open loop gain			60			60		dB
Feedback resistor		10K			10K			Ω
Small signal bandwith			3			3		MHz
Output voltage swing (positive)		6.2			6.2			V
Output voltage swing (negative)				0.7			0.6	V
OUTPUT STAGE								
Output Current (Pin 15)		40			40			mA
Max emitter voltage (Pin 14)		5	6		5	6		V
V_{CE}(SAT) I_C = 40mA				0.5			0.5	V
SUPPLY VOLTAGE/CURRENT								
I_{CC}	$I_Z = 0$, Voltage fed, $V_{CC} = 12V$, 25°C			10			10	mA
	Over temp.			15			15	mA
V_{CC}	I_{CC} = 10mA, Current fed	20		23	19		24	V
V_{CC}	I_{CC} = 30mA, Current fed	20		30	20		30	V

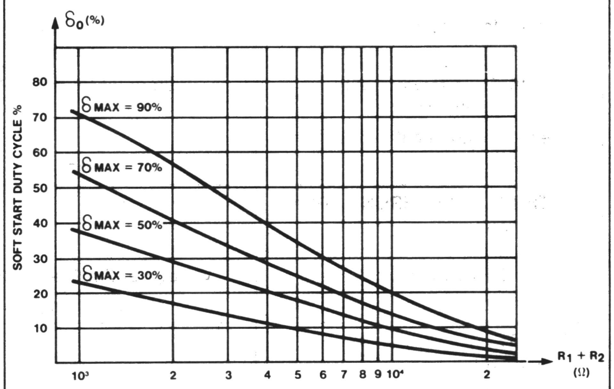
NOTES
1. See graph
2. See graph

TYPICAL PERFORMANCE CHARACTERISTICS

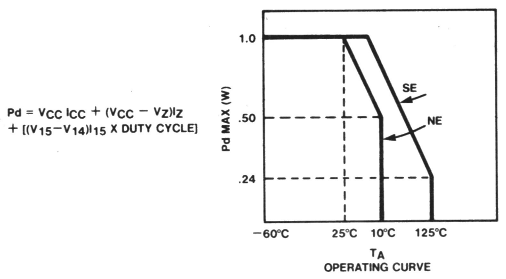
GRAPH FOR DETERMINING δ MAX



SOFT-START MIN. DUTY CYCLE VS $R_1 + R_2$

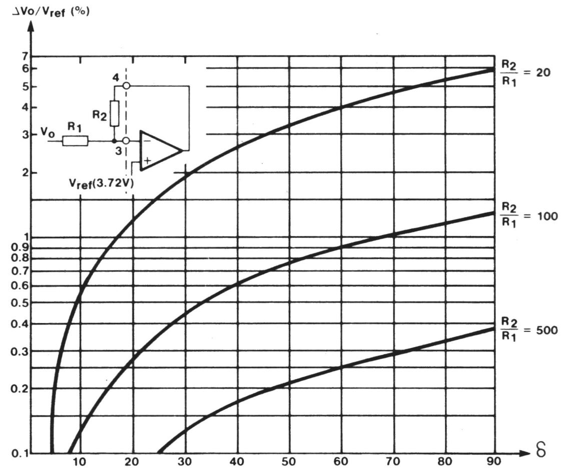


POWER DERATING CURVE



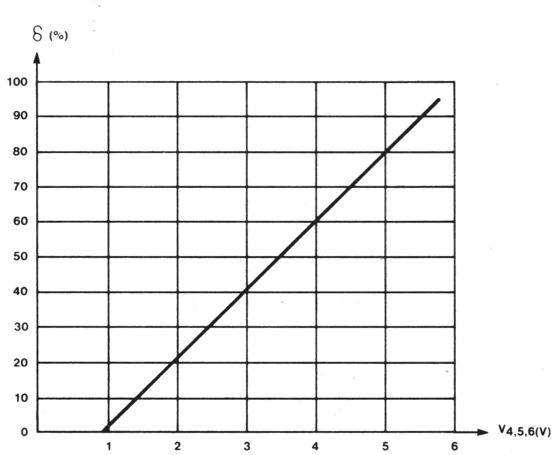
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

REGULATION VS ERROR AMP CLOSED LOOP GAIN

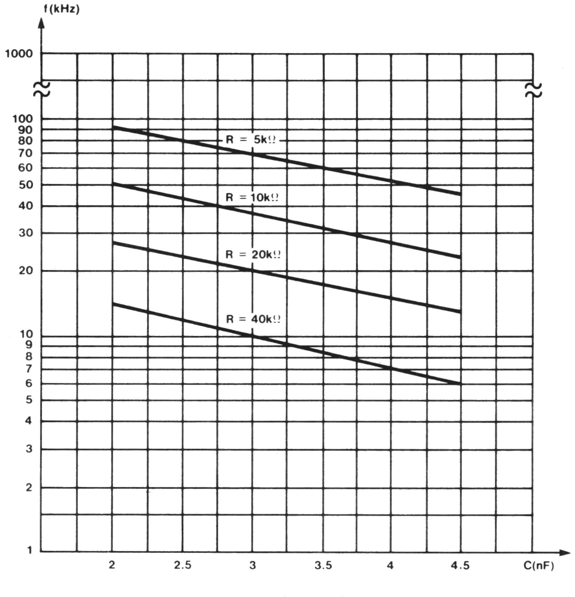


TRANSFER CURVE OF PULSE WIDTH MODULATOR

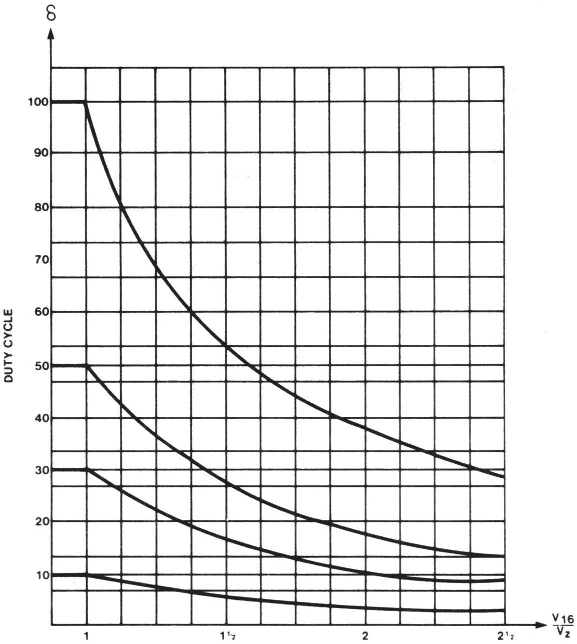
DUTY CYCLE VS INPUT VOLTAGE



TYPICAL FREQUENCY PLOT VS R_T AND C_T



DUTY CYCLE SENSITIVITY TO FEED FORWARD VOLTAGE (PIN 16)



DESCRIPTION

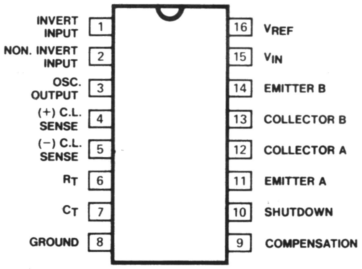
This monolithic integrated circuit contains all the control circuitry for a regulating power supply inverter or switching regulator. Included in a 16-pin dual-in-line package is the voltage reference, error-amplifier, oscillator, pulse width modulator, pulse steering flip-flop, dual alternating output switches and current limiting and shut-down circuitry. This device can be used for switching regulators of either polarity, transformer coupled DC to DC converters, transformerless voltage doublers and polarity converters, as well as other power control applications. The SG1524 is specified for operation over the full military temperature range of −55°C to +125°C, while the SG2524 and SG3524 are designed for commercial applications of 0°C to +70°C.

FEATURES

- **Complete PWM power control circuitry**
- **Single ended or push-pull outputs**
- **Line and load regulation of 0.2%**
- **1% maximum temperature variation**
- **Total supply current is less than 10mA**
- **Operation beyond 100kHz**

PIN CONFIGURATION

CONNECTION DIAGRAM
F,N PACKAGE


INVERT INPUT 1
NON. INVERT INPUT 2
OSC. OUTPUT 3
(+) C.L. SENSE 4
(−) C.L. SENSE 5
RT 6
CT 7
GROUND 8
16 VREF
15 VIN
14 EMITTER B
13 COLLECTOR B
12 COLLECTOR A
11 EMITTER A
10 SHUTDOWN
9 COMPENSATION

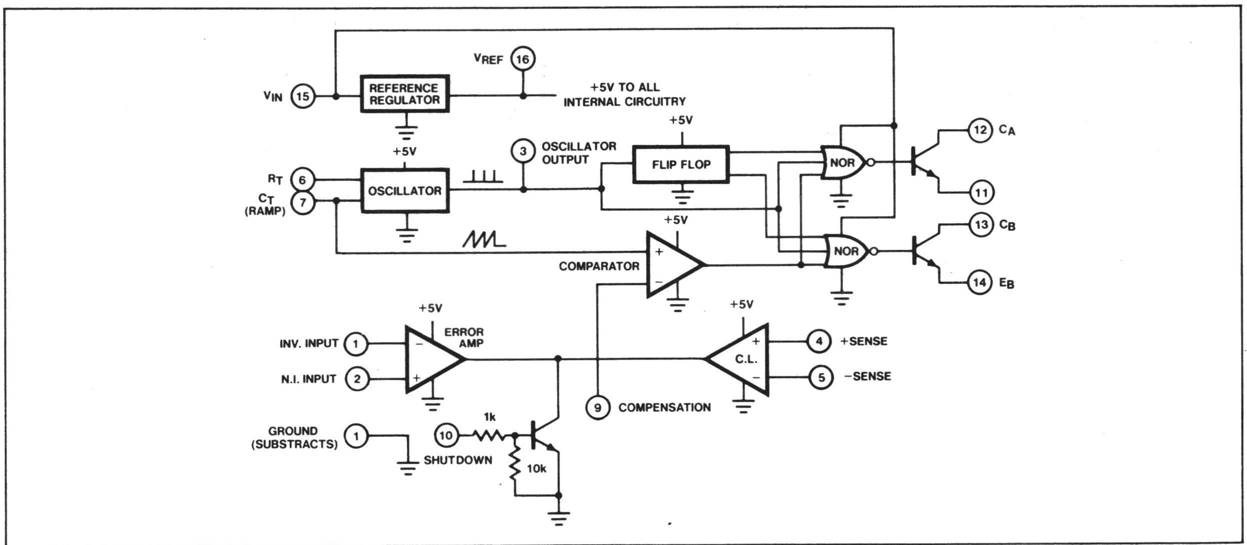
TOP VIEW

ORDER PART NO.
SG1524F, SG2524F
SG2524N, SG3524F
SG3524N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Input voltage	40	V
Output current (each output)	100	mA
Reference output current	50	mA
Oscillator charging current	5	mA
Power dissipation		
Package limitation	1000	mW
Derate above 25°C	8	mW/°C
Operating temperature range		
SG1524	−55 to +125	°C
SG2524/SG3524	0 to +70	°C
Storage temperature range	−65 to +150	°C

BLOCK DIAGRAM


VREF 16
VIN 15
REFERENCE REGULATOR
+5V TO ALL INTERNAL CIRCUITRY
+5V
3 OSCILLATOR OUTPUT
FLIP FLOP
RT 6
CT (RAMP) 7
OSCILLATOR
NOR
12 CA
11
13 CB
14 EB
COMPARATOR
ERROR AMP
INV. INPUT 1
N.I. INPUT 2
C.L.
4 +SENSE
5 −SENSE
9 COMPENSATION
GROUND (SUBSTRACTS) 1
10 SHUTDOWN
1k
10k

DC ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for $T_A = -55°C$ to $+125°C$ for the SG1524 and 0°C to +70°C for the SG2524 and SG3524, $V_{IN} = 20V$, and f = 20kHz)

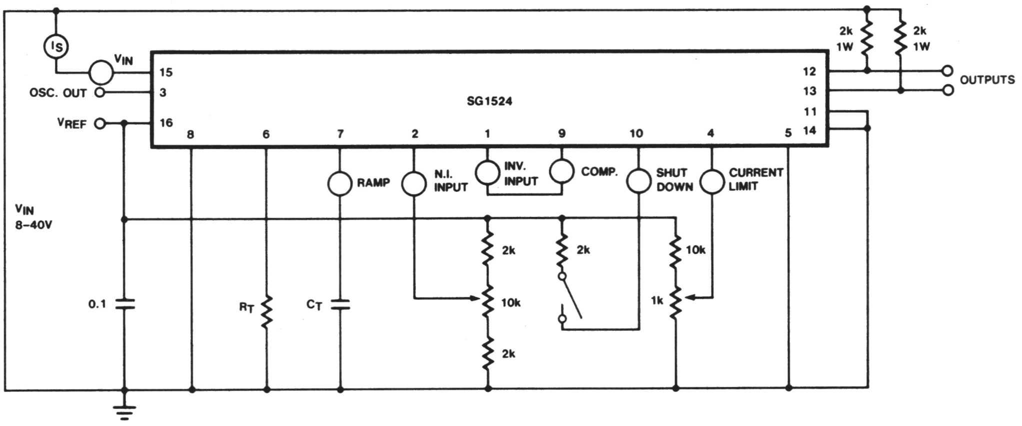
PARAMETER	TEST CONDITIONS	SG1524 SG2524			SG3524			UNIT
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Output voltage		4.8	5.0	5.2	4.6	5.0	5.4	V
Line regulation	V_{IN} = 8 to 40V		10	20		10	30	mV
Load regulation	I_L = 0 to 20mA		20	50		20	50	mV
Ripple rejection	f = 120Hz, $T_A = 25°C$		66			66		dB
Short circuit current limit	$V_{REF} = 0$, $T_A = 25°C$		100			100		mA
Temperature stability	Over operating temperature range		0.3	1		0.3	1	%
Long term stability	$T_A = 25°C$		20			20		mV/kHr
OSCILLATOR SECTION								
Maximum frequency	C_T = .001 mfd, $R_T = 2k\Omega$		300			300		kHz
Initial accuracy	R_T and C_T constant		5			5		%
Voltage stability	V_{IN} = 8 to 40V, $T_A = 25°C$			1			1	%
Temperature stability	Over operating temperature range						2	%
Output amplitude	Pin 3, $T_A = 25°C$		3.5			3.5		V
Output pulse width	C_T = .01 mfd, $T_A = 25°C$		0.5			0.5		μs
ERROR AMPLIFIER SECTION								
Input offset voltage	$V_{CM} = 2.5V$		0.5	5		2	10	mV
Input bias current	$V_{CM} = 2.5V$		2	10		2	10	μA
Open loop voltage gain		72	80		60	80		dB
Common mode voltage	$T_A = 25°C$	1.8		3.4	1.8		3.4	V
Common mode rejection ratio	$T_A = 25°C$		70			70		dB
Small signal bandwidth	A_V = 0dB, $T_A = 25°C$		3			3		MHz
Output voltage	$T_A = 25°C$	0.5		3.8	0.5		3.8	V
COMPARATOR SECTION								
Duty cycle	% each output "ON"	0		45	0		45	%
Input threshold	Zero duty cycle		1			1		V
Input threshold	Maximum duty cycle		3.5			3.5		V
Input bias current			1			1		μA
CURRENT LIMITING SECTION								
Sense voltage	Pin 9 = 2V with error amplifier set for maximum out, $T_A = 25°C$	190	200	210	180	200	220	mV
Sense voltage T.C.			0.2			0.2		mV/°C
Common mode voltage		−1		+1	−1		+1	V
OUTPUT SECTION (each output)								
Collector-emitter voltage		40			40			V
Collector-leakage current	$V_{CE} = 40V$		0.1	50		0.1	50	μA
Saturation voltage	$I_C = 50mA$		1	2		1	2	V
Emitter output voltage	$V_{IN} = 20V$	17	18		17	18		V

DC ELECTRICAL CHARACTERISTICS (Cont'd)

(Unless otherwise stated, these specifications apply for $T_A = -55°C$ to $+125°C$ for the SG1524 and 0°C to +70°C for the SG2524 and SG3524, $V_{IN} = 20V$, and f = 20kHz)

PARAMETER	TEST CONDITIONS	SG1524 SG2524			SG3524			UNIT
		Min	Typ	Max	Min	Typ	Max	
Rise time	R_C = 2K ohm, T_A = 25°C		0.2			0.2		μs
Fall time	R_C = 2K ohm, T_A = 25°C		0.1			0.1		μs
TOTAL STANDBY CURRENT (excluding oscillator charging current, error and current limit dividers, and with outputs open)	V_{IN} = 40V		8	10		8	10	mA

OPEN LOOP TEST CIRCUIT



APPLICATIONS

Voltage Reference

An internal series regulator provides a nominal 5 volt output which is used both to generate a reference voltage and is the regulated source for all the internal timing and controlling circuitry. This regulator may be bypassed for operation from a fixed 5 volt supply by connecting pins 15 and 16 together to the input voltage. In this configuration, the maximum input voltage is 6.0 volts.

This reference regulator may be used as a 5 volt source for other circuitry. It will provide up to 50mA of current itself and can easily be expanded to higher currents with an external PNP as shown in Figure 1.

Oscillator

The oscillator in the SG1524 uses an external resistor (R_T) to establish a constant charging current into an external capacitor (C_T). While this uses more current than a series connected RC, it provides a linear ramp voltage on the capacitor which is also used as a reference for the comparator. The charging current is equal to 3.6V ÷ R_T and should be kept within the range of approximately 30μA to 2mA, i.e., $1.8K < R_T < 100K$.

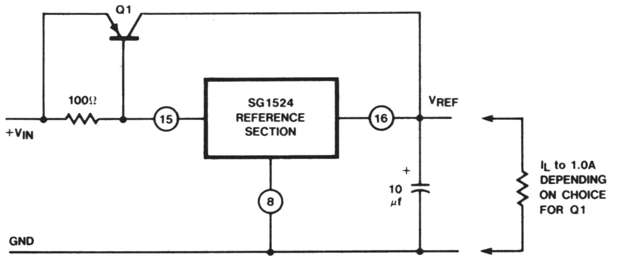
The range of values for C_T also has limits as the discharge time of C_T determines the pulse width of the oscillator output pulse. This pulse is used (among other things) as a blanking pulse to both outputs to insure that there is no possibility of having both outputs on simultaneously during transitions. This output dead time relationship is shown in Figure 2. A pulse width below approximately 0.5 microseconds may allow false triggering of one output by removing the blanking pulse prior to the flip-flops reaching a stable state. If small values of C_T must be used, the pulse width may still be expanded by adding a shunt capacitance (≈100pF) to ground at the oscillator output. (Note: Although the oscillator output is a convenient oscilloscope sync input, the cable and input capacitance may increase the blanking pulse width slightly.) Obviously, the upper limit to the pulse width is determined by the maximum duty cycle acceptable. Practical values of C_T fall between .001 and 0.1 microfarad.

The oscillator period is approximately $t = R_TC_T$ where t is in microseconds when R_T = ohms and C_T = microfarads. The use of Figure 3 will allow selection of R_T and C_T for a wide range of operating frequencies. Note that for series regulator applications, the two outputs can be connected in parallel for an effective 0-90% duty cycle and the frequency of the oscillator is the frequency of the output. For push-pull applications, the outputs are separated and the flip-flop divides the frequency such that each outputs duty cycle is 0-45% and the overall frequency is one-half that of the oscillator.

If it is desired to synchronize the SG1524 to an external clock, a pulse of ≈+3 volts may be applied to the oscillator output terminal with R_TC_T set slightly greater than the clock period. The same considerations of pulse width apply. The impedance to ground at this point is approximately 2K ohms.

If two or more SG1524's must be synchronized together, one must be designated as master with its R_TC_T set for the correct period. The slaves should each have an R_TC_T

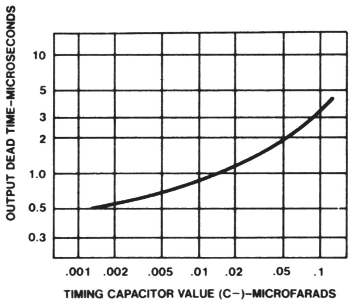
TYPICAL APPLICATION



Expanded Reference Current Capability.

Figure 1

TYPICAL APPLICATION



Output stage dead time as a function of the timing capacitor value.

Figure 2

set for approximately 10% longer period than the master with the added requirement that C_T (slave) = one-half C_T (master). Then connecting Pin 3 on all units together will insure that the master output pulse—which occurs first and has a wider pulse width—will reset the slave units.

Error Amplifier

This circuit is a simple differential-input, transconductance amplifier. The output is the compensation terminal, pin 9, which is a high impedance node ($R_L \approx 5M\Omega$). The gain is

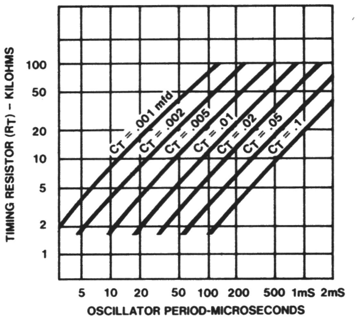
$$A_V = gmR_L = \frac{8\, I_C\, R_L}{2kT} \approx .002\, R_L$$

and can easily be reduced from a nominal of 10,000 by an external shunt resistance from pin 9 to ground, as shown in Figure 4.

In addition to DC gain control, the compensation terminal is also the place for AC phase compensation. The frequency response curves of Figure 4 show the uncompensated amplifier with a single pole at approximately 200Hz and a unity gain cross-over at 5MHz.

Typically, most output filter designs will introduce one or more additional poles at a significantly lower frequency. Therefore, the best stabilizing network is a series R-C combination between pin 9 and ground which introduces a zero to cancel one of the output filter poles. A good starting point is 50kΩ plus .001 microfarad.

TYPICAL APPLICATION



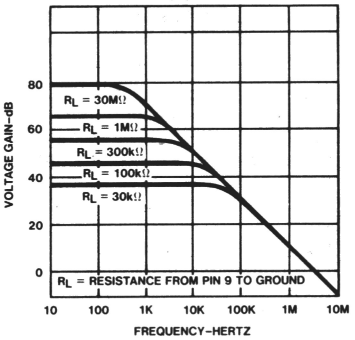
Oscillator period as a function of R_T and C_T.

Figure 3

One final point on the compensation terminal is that this is also a convenient place to insert any programming signal which is to override the error amplifier. Internal shutdown and current limit circuits are connected here, but any other circuit which can sink 200μA can pull this point to ground thus shutting off both outputs.

While feedback is normally applied around the entire regulator, the error amplifier can be used with conventional operational amplifier feedback and is stable in either the inverting or non-inverting mode. Regardless of the connections, however, input common-mode limits must be observed or output signal inversions may result. For conventional regulator applications, the 5 volt reference voltage must be divided down as shown in Figure 5. The error amplifier may also be used in fixed duty cycle applications by using the unity gain configuration shown in the open loop test circuit.

TYPICAL APPLICATION



Amplifies open-loop gain as a function of frequency and loading on Pin 9.

Figure 4

Current Limiting

The current limiting circuitry of the SG1524 is shown in Figure 6.

By matching the base-emitter voltages of Q1 and Q2, and assuming negligible voltage drop across R_1,

$$\begin{aligned}\text{Threshold} &= V_{BE}(Q1) + I_1R_2 - V_{BE}(Q2)\\ &= I_1R_2 \approx 200\text{mV}\end{aligned}$$

Although this circuit provides a relatively small threshold with a negligible temperature coefficient, there are some limitations to its use, the most important of which is the ±1 volt common mode range which requires sensing in the ground line. Another factor to consider is that the frequency compensation provided by R_1C_1 and Q1 provides a roll-off pole at approximately 300Hz.

Since the gain of this circuit is relatively low, there is a transition region as the current limit amplifier takes over pulse width control from the error amplifier. For testing purposes, threshold is defined as the input voltage to get 25% duty cycle with the error amplifier signaling maximum duty cycle.

In addition to constant current limiting, pins 4 and 5 may also be used in transformer-coupled circuits to sense primary current and shorten an output pulse, should transformer saturation occur. (Refer to Figure 14). Another application is to ground pin 5 and use pin 4 as an additional shutdown terminal: i.e., the output will be off with pin 4 open and on when it is grounded. Finally, foldback current limiting can be provided with the network of Figure 7. This circuit can reduce the short-circuit current (I_{SC}) to approximately one-third the maximum available output current (I_{MAX}).

Output Circuits

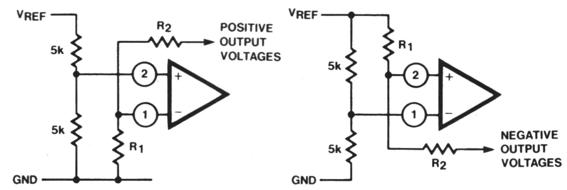
The outputs of the SG1524 are two identical NPN transistors with both collectors and emitters uncommitted. This circuitry is very similar to that used in the SG111 comparator in that each output transistor has antisaturation circuitry for fast response, and current limiting set for a maximum output current of approximately 100mA. The availability of both collectors and emitters allows maximum versatility to enable driving either NPN or PNP external transistors.

In considering the application of the SG1524 to voltage regulator circuitry, there are a multitude of output configurations possible. In general, however, they fall into three basic classifications:

1. Capacitor-diode coupled voltage multipliers
2. Inductor-capacitor single-ended circuits
3. Transformer-coupled circuits

Examples of each category are shown in Figures 8, 9 and 10. In each case, the switches indicated can be either the output transistors in the SG1524 or added external transistors according to the load current requirements.

TYPICAL APPLICATION



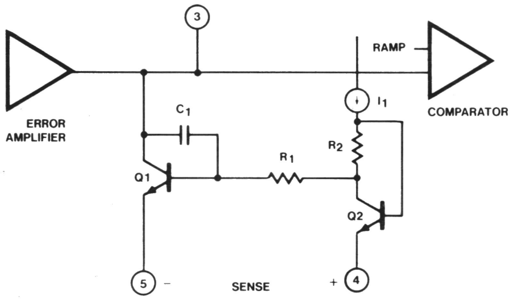
$$V_O = \frac{2.5V\,(R + R_2)}{R_1}$$

$$\frac{R_1\,R_2}{R_2 + R_2} = 2.5k\Omega$$

Error amplifier biasing circuits. Note change in input connections for opposite polarity outputs.

Figure 5

TYPICAL APPLICATION



Current Limiting Circuitry of the SG1524.

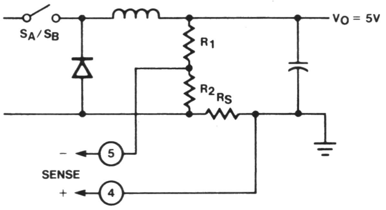
Figure 6

TYPICAL APPLICATION

$$I_{MAX} = \frac{1}{R_S}\left(V_{TH} + \frac{V_O\,R_2}{R_1 + R_2}\right)$$

$$I_{SC} = \frac{V_{TH}}{R_S} \quad \text{WHERE}$$

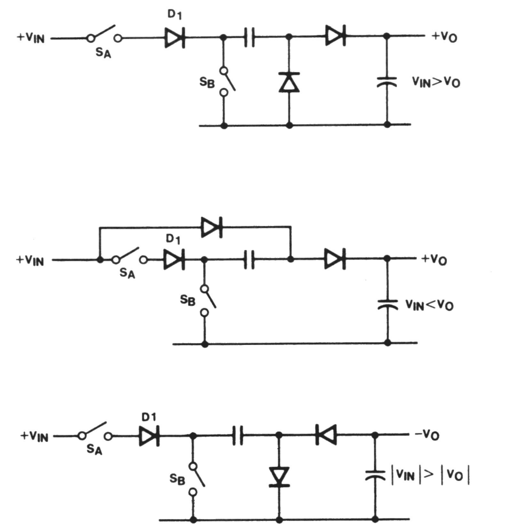
$$V_{TH} = 200\text{ mV}$$



Foldback current limiting can be used to reduce power dissipation under shorted output conditions.

Figure 7

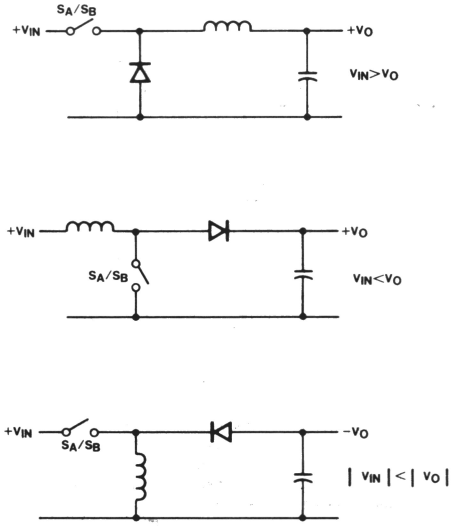
TYPICAL APPLICATION (Cont'd)


+VIN
SA
D1
SB
+VO
VIN>VO
VIN<VO
-VO
|VIN|>|VO|

Capacitor-diode coupled voltage multiplier output stages. (Note: Diode D1 is necessary to prevent reverse emitter-base breakdown to transistor switch S_A).

Figure 8

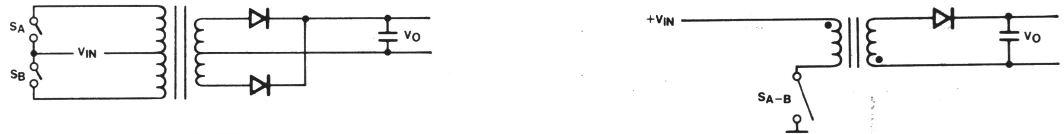
TYPICAL APPLICATION


SA/SB
+VIN
+VO
VIN>VO
VIN<VO
-VO
| VIN |<| VO |

Single-ended inductor circuits where the two outputs of the SG1524 are connected in parallel.

Figure 9

TYPICAL APPLICATION


SA
SB
VIN
VO
+VIN
SA-B

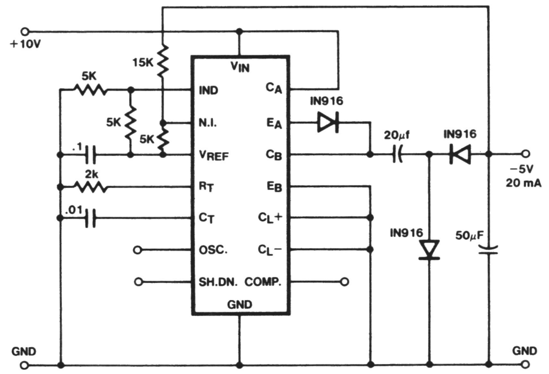
PUSH PULL

FLYBACK

Transformer-coupled outputs need not relate to the input in either amplitude or polarity.

Figure 10

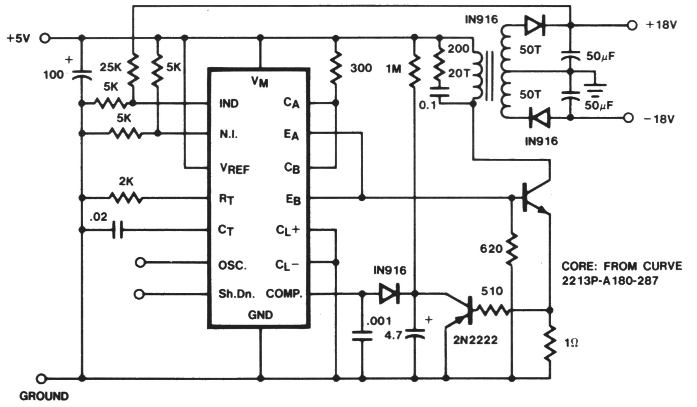
TYPICAL APPLICATION


+10V
15K
5K
5K
5K
.1
2k
.01
VIN
IND
N.I.
VREF
RT
CT
OSC.
SH.DN.
COMP.
GND
CA
EA
CB
EB
CL+
CL-
IN916
20μf
IN916
-5V
20 mA
IN916
50μF
GND
GND

The capacitor-diode output circuit is used here as a polarity converter to generate a −5 volt supply from +15 volts. This circuit is useful for an output current of up to 20mA with no additional boost transistors required. Since the output transistors are current limited, no additional protection is necessary. Also, the lack of an inductor allows the circuit to be stabilized with only the output capacitor.

Figure 11

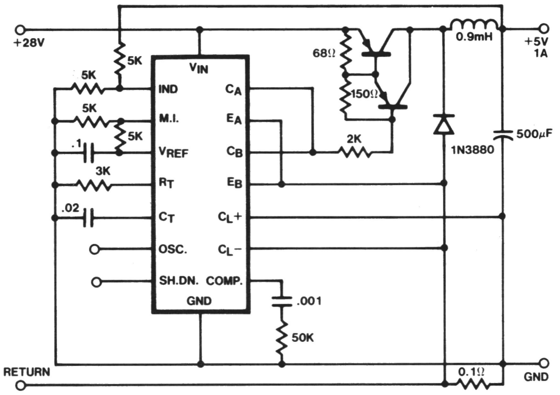
TYPICAL APPLICATION


+5V
+
100
25K
5K
5K
5K
2K
.02
V_M
IND
N.I.
V_{REF}
R_T
C_T
OSC.
Sh.Dn.
C_A
E_A
C_B
E_B
C_L+
C_L-
COMP.
GND
300
1M
200
20T
0.1
IN916
50T
50T
50μF
50μF
+18V
−18V
IN916
620
CORE: FROM CURVE
2213P-A180-287
IN916
510
.001
4.7
+
2N2222
1Ω
GROUND

Another low-current supply is the flyback converter used here to generate ±15 volts at 20mA from a +5 volt regulated line. The reference generator in the SG1524 is unused with the input voltage providing the reference. Current limiting in a flyback converter is difficult and is accomplished here by sensing current in the primary line and resetting a soft-start circuit.

Figure 12

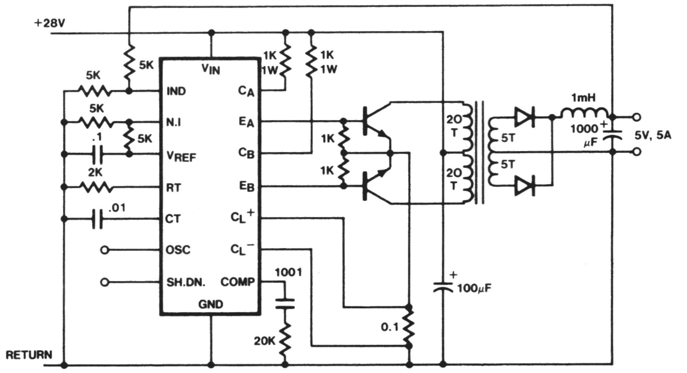
TYPICAL APPLICATION


+28V
5K
5K
5K
5K
.1
3K
.02
V_{IN}
IND
M.I.
V_{REF}
R_T
C_T
OSC.
SH.DN.
C_A
E_A
C_B
E_B
C_L+
C_L-
COMP.
GND
68Ω
150Ω
2K
0.9mH
+5V
1A
1N3880
500μF
.001
50K
RETURN
0.1Ω
GND

In this conventional single-ended regulator circuit, the two outputs of the SG1524 are connected in parallel for effective .0-90% duty-cycle modulation. The use of an output inductor requires an R-C phase compensation network for loop stability.

Figure 13

TYPICAL APPLICATION


+28V
5K
5K
5K
.1
5K
2K
.01
RETURN
VIN
IND
N.I
VREF
RT
CT
OSC
SH.DN.
GND
CA
EA
CB
EB
CL+
CL−
COMP
1K
1W
1K
1W
1K
1K
1001
20K
0.1
100μF
20
T
20
T
5T
5T
1mH
1000
μF
5V, 5A

Push-pull outputs are used in this transformer-coupled DC-DC regulating converter. Note that the oscillator must be set at twice the desired output frequency as the SG1524's internal flip-flop divides the frequency by 2 as it switches the P.W.M. signal from one output to the other. Current limiting is done here in the primary so that the pulse width will be reduced should transformer saturation occur.

Figure 14

SECTION 4
TIMERS

Section 4—TIMERS

NE/SE555 Timer 123
SE555C Timer 123
NE/SE556 Dual Timer 126
NE/SE556-1 Dual Timer 129
SE556-1C Dual Timer 129
NE/SE558 Quad Timer 132

NOTE

*Any product listed in this section but not incorporated within the text may be obtained by writing Information Services at Signetics, 811 E. Arques, M/S 027, Sunnyvale, California 94086, or by calling (408) 746-1682.

TIMER

NE/SE555/SE555C

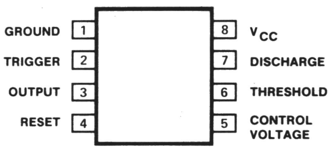
SE555F,H,N,N-14 • SE555C,F,H,N,N-14 • NE555F,H,N,N-14

FEATURES

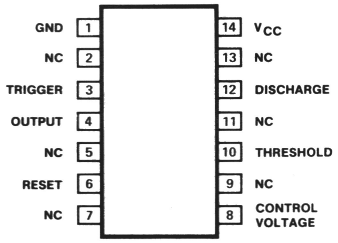
- Turn off time less than 2μs
- Maximum operating frequency greater than 500kHz
- Timing from microseconds to hours
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per °C
- SE555 Mil std 883A,B,C available M38510 (JAN) approved, M38510 processing available.

PIN CONFIGURATIONS

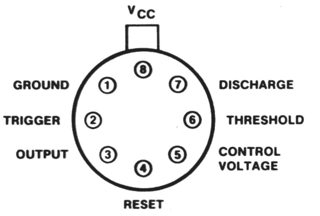
N PACKAGE


GROUND 1
TRIGGER 2
OUTPUT 3
RESET 4
8 V_{CC}
7 DISCHARGE
6 THRESHOLD
5 CONTROL VOLTAGE

F,N-14 PACKAGE


GND 1
NC 2
TRIGGER 3
OUTPUT 4
NC 5
RESET 6
NC 7
14 V_{CC}
13 NC
12 DISCHARGE
11 NC
10 THRESHOLD
9 NC
8 CONTROL VOLTAGE

H PACKAGE


V_{CC}
GROUND ①
TRIGGER ②
OUTPUT ③
④ RESET
⑤ CONTROL VOLTAGE
⑥ THRESHOLD
⑦ DISCHARGE
⑧

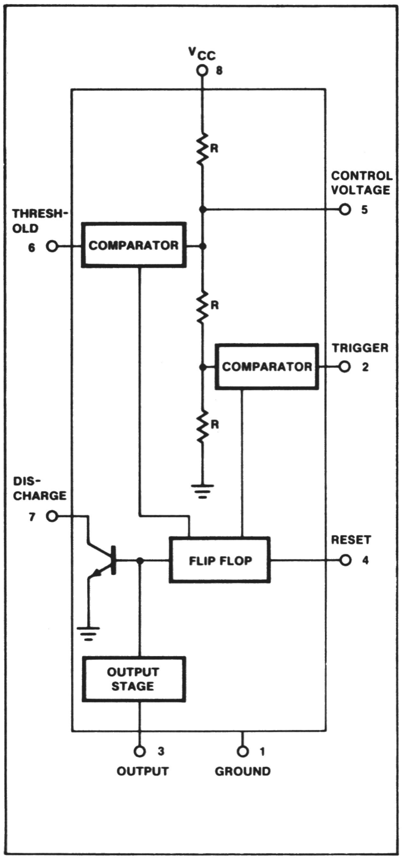
APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Missing pulse detector

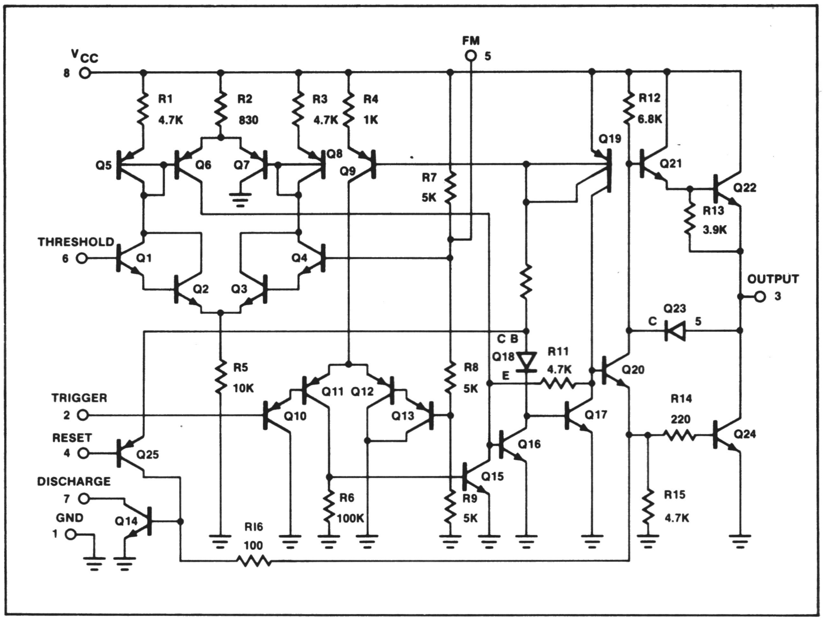
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
SE555	+18	V
NE555, SE555C,	+16	V
Power dissipation	600	mW
Operating temperature range		
NE555	0 to +70	°C
SE555, SE555C	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Load temperature (soldering, 60sec)	300	°C

BLOCK DIAGRAM


V_{CC}
8
R
CONTROL VOLTAGE
5
THRESH-OLD
6
COMPARATOR
R
COMPARATOR
TRIGGER
2
R
DIS-CHARGE
7
FLIP FLOP
RESET
4
OUTPUT STAGE
3
OUTPUT
1
GROUND

EQUIVALENT SCHEMATIC


V_{CC}
8
FM
5
R1 4.7K
R2 830
R3 4.7K
R4 1K
R12 6.8K
Q5
Q6
Q7
Q8
Q9
Q19
Q21
Q22
R7 5K
R13 3.9K
THRESHOLD
6
Q1
Q2
Q3
Q4
OUTPUT
3
Q23
C
5
C B
Q18
E
R11 4.7K
Q20
R5 10K
Q11 Q12
R8 5K
TRIGGER
2
Q10
Q13
Q17
R14 220
Q24
RESET
4
Q25
Q16
DISCHARGE
7
Q15
R6 100K
R9 5K
R15 4.7K
GND
1
Q14
R16 100

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +5V to +15 unless otherwise specified.

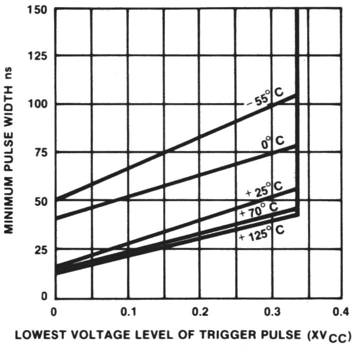
PARAMETER	TEST CONDITIONS	SE555			NE555/SE555C			UNIT
		Min	Typ	Max	Min	Typ	Max	
Supply voltage		4.5		18	4.5		16	V
Supply current (low state)[1]	V_{CC} = 5V $R_L = \infty$		3	5		3	6	mA
	V_{CC} = 15V $R_L = \infty$		10	12		10	15	mA
Timing error (monostable)	R_A = 2KΩ to 100KΩ							
Initial accuracy[2]	C = 0.1μF		0.5	2.0		1.0	3.0	%
Drift with temperature			30	100		50		ppm/°C
Drift with supply voltage			0.05	0.2		0.1	0.5	%/V
Timing error (astable)	R_A, R_B = 1kΩ to 100kΩ							
Initial accuracy[2]	C = 0.1μF		1.5			2.25		%
Drift with temperature	V_{CC} = 15V		90			150		ppm/°C
Drift with supply voltage			0.15			0.3		%/V
Control voltage level	V_{CC} = 15V	9.6	10.0	10.4	9.0	10.0	11.0	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4.0	V
Threshold voltage	V_{CC} = 15V	9.4	10.0	10.6	8.8	10.0	11.2	V
	V_{CC} = 5V	2.7	3.33	4.0	2.4	3.33	4.2	V
Threshold current[3]			0.1	0.25		0.1	0.25	μA
Trigger voltage	V_{CC} = 15V	4.8	5.0	5.2	4.5	5.0	5.6	V
	V_{CC} = 5V	1.45	1.67	1.9	1.1	1.67	2.2	V
Trigger current	V_{TRIG} = 0V		0.5	0.9		0.5	2.0	μA
Reset voltage[4]		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset current			0.1	0.4		0.1	0.4	mA
Reset current	V_{RESET} = 0V		0.4	1.0		0.4	1.5	mA
Output voltage (low)	V_{CC} = 15V							
	I_{SINK} = 10mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100mA		2.0	2.2		2.0	2.5	V
	I_{SINK} = 200mA		2.5			2.5		V
	V_{CC} = 5V							
	I_{SINK} = 8mA		0.1	0.25		0.3	0.4	V
	I_{SINK} = 5mA		0.05	0.2		0.25	0.35	V
Output voltage (high)	V_{CC} = 15V							
	I_{SOURCE} = 200mA		12.5			12.5		V
	I_{SOURCE} = 100mA	13.0	13.3		12.75	13.3		V
	V_{CC} = 5V							
	I_{SOURCE} = 100mA	3.0	3.3		2.75	3.3		V
Turn off time[5]	V_{RESET} = V_{CC}		0.5	2.0		0.5		μs
Rise time of output			100	200		100	300	ns
Fall time of output			100	200		100	300	ns
Discharge leakage current			20	100		20	100	na

NOTES

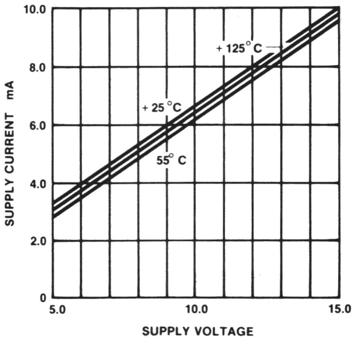
1. Supply current when output high typically 1mA less.
2. Tested at V_{CC} = 5V and V_{CC} = 15V.
3. This will determine the maximum value of $R_A + R_B$, for 15V operation, the max total R = 10 megohm, and for 5V operation, the max total R = 3.4 megohm.
4. Specified with trigger input high.
5. Time measured from a positive going input pulse from 0 to 0.8xV_{CC} into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

TYPICAL PERFORMANCE CHARACTERISTICS

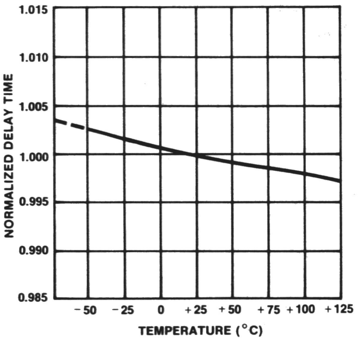
MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



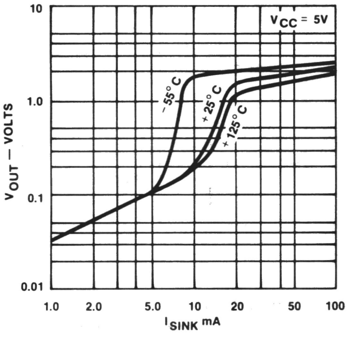
SUPPLY CURRENT vs SUPPLY VOLTAGE



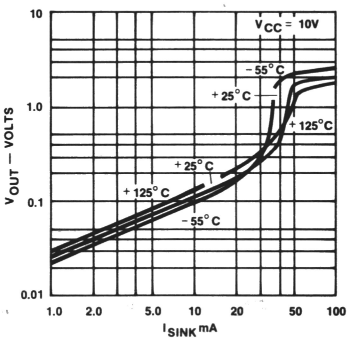
DELAY TIME vs TEMPERATURE



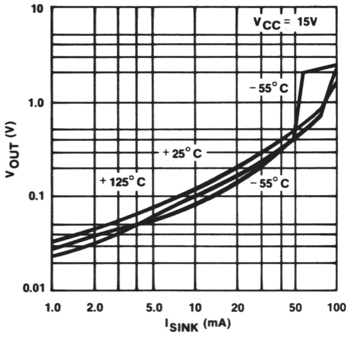
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



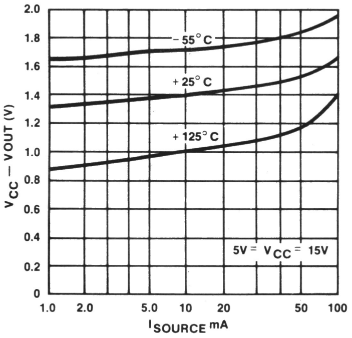
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



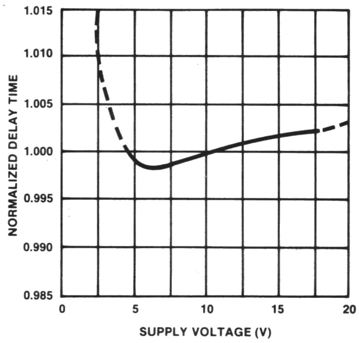
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



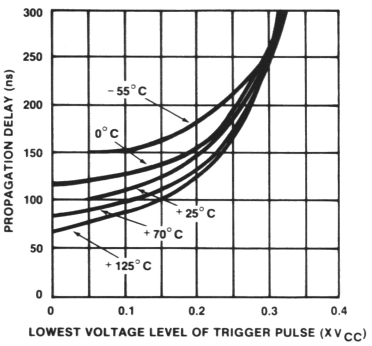
HIGH OUTPUT VOLTAGE DROP vs OUTPUT SOURCE CURRENT



DELAY TIME vs SUPPLY VOLTAGE



PROPAGATION DELAY vs VOLTAGE LEVEL OF TRIGGER PULSE



DUAL TIMER NE/SE556

SE556N,F • NE556F,N • SE556C,F,N

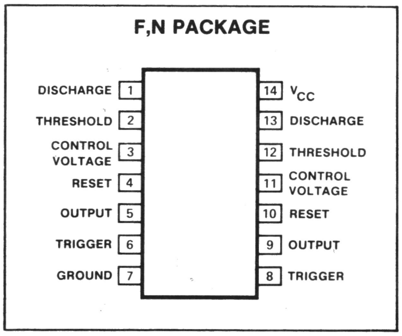
FEATURES

- Timing from microseconds to hours
- Replaces two 555 timers
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per °C
- SE566 MIL STD 883A, B, C available, N38510 (JAN planned, 38510 processing available).

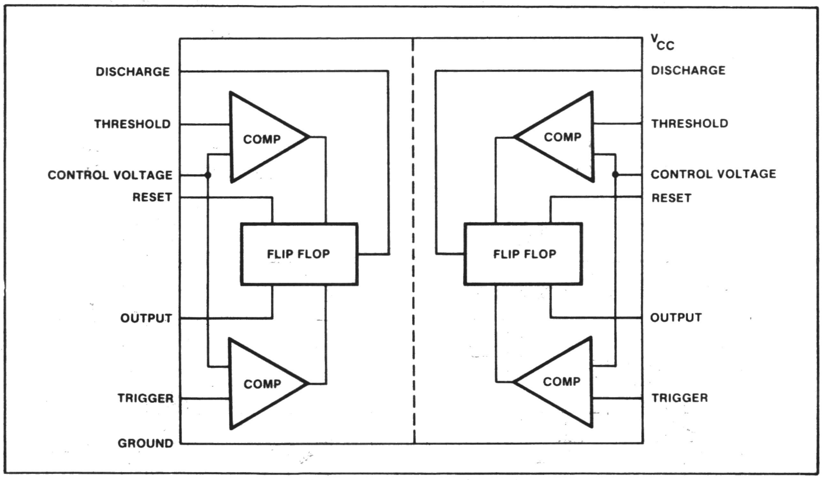
APPLICATIONS

- Precision timing
- Sequential timing
- Pulse shaping
- Pulse generator
- Missing pulse detector
- Tone burst generator
- Pulse width modulation
- Time delay generator
- Frequency division
- Industrial controls
- Pulse position modulation
- Appliance timing
- Traffic light control
- Touch tone encoder

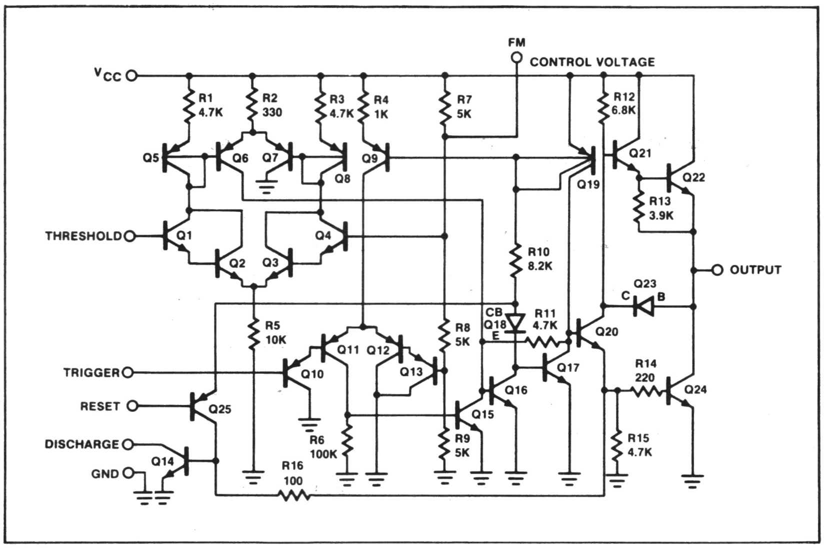
PIN CONFIGURATION


F,N PACKAGE
DISCHARGE 1
THRESHOLD 2
CONTROL VOLTAGE 3
RESET 4
OUTPUT 5
TRIGGER 6
GROUND 7
14 V_{CC}
13 DISCHARGE
12 THRESHOLD
11 CONTROL VOLTAGE
10 RESET
9 OUTPUT
8 TRIGGER

BLOCK DIAGRAM


V_{CC}
DISCHARGE
THRESHOLD
CONTROL VOLTAGE
RESET
OUTPUT
TRIGGER
GROUND
COMP
FLIP FLOP
COMP
DISCHARGE
THRESHOLD
CONTROL VOLTAGE
RESET
OUTPUT
TRIGGER
COMP
FLIP FLOP
COMP

EQUIVALENT SCHEMATIC (Shown for one circuit only)


FM
CONTROL VOLTAGE
V_{CC}
R1 4.7K
R2 330
R3 4.7K
R4 1K
R7 5K
R12 6.8K
Q5
Q6
Q7
Q8
Q9
Q19
Q21
Q22
R13 3.9K
THRESHOLD
Q1
Q2
Q3
Q4
R10 8.2K
OUTPUT
Q23
C
B
R5 10K
CB
Q18
E
R11 4.7K
Q20
R8 5K
Q11
Q12
Q13
Q17
R14 220
TRIGGER
Q10
Q16
Q24
RESET
Q25
Q15
DISCHARGE
R6 100K
R9 5K
R15 4.7K
Q14
GND
R16 100

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
SE556	+18	V
NE556, SE556C,	+16	V
Power dissipation	600	mW
Operating temperature range		
NE556	0 to +70	°C
SE556, SE556C	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (Soldering, 60 sec)	+300	°C

ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = +5V$ to $+15V$ unless otherwise specified.

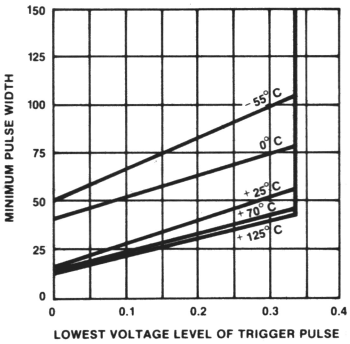
PARAMETER	TEST CONDITIONS	SE556			NE556/SE556C			UNITS
		Min	Typ	Max	Min	Typ	Max	
Supply voltage		4.5		18	4.5		16	V
Supply current (low state)[1]	$V_{CC} = 5V$ $R_L = \infty$		6	10		6	12	mA
	$V_{CC} = 15V$ $R_L = \infty$		20	24		20	30	mA
Timing error (monostable)	$R_A = 2k\Omega$ to $100k\Omega$							
Initial accuracy[2]	$C = 0.1\mu F$		0.5	1.5		0.75	3.0	%
Drift with temperature			30	100		50		ppm/°C
Drift with supply voltage			0.05	0.2		0.1	0.5	%/V
Timing error (astable)	R_A, $R_B = 1k\Omega$ to $100k\Omega$							
Initial accuracy[2]	$C = 0.1\mu F$		1.5			2.25		%
Drift with temperature	$V_{CC} = 15V$		90			150		ppm/°C
Drift with supply voltage			0.15			0.3		%/V
Control voltage level	$V_{CC} = 15V$	9.6	10.0	10.4	9.0	10.0	11.0	V
	$V_{CC} = 5V$	2.9	3.33	3.8	2.6	3.33	4.0	V
Threshold voltage	$V_{CC} = 15V$	9.4	10.0	10.6	8.8	10.0	11.2	V
	$V_{CC} = 5V$	2.7	3.33	4.0	2.4	3.33	4.2	V
Threshold current[3]			30	250		30	250	nA
Trigger voltage	$V_{CC} = 15V$	4.8	5.0	5.2	4.5	5.0	5.6	V
	$V_{CC} = 5V$	1.45	1.67	1.9	1.1	1.67	2.2	V
Trigger current	$V_{TRIG} = 0V$		0.5	0.9		0.5	2.0	μA
Reset voltage[5]		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset current			0.1	0.4		0.1	0.6	mA
Reset current	$V_{RESET} = 0V$		0.4	1.0		0.4	1.5	mA
Output voltage (low)	$V_{CC} = 15V$							
	$I_{SINK} = 10mA$		0.1	0.15		0.1	0.25	V
	$I_{SINK} = 50mA$		0.4	0.5		0.4	0.75	V
	$I_{SINK} = 100mA$		2.0	2.25		2.0	3.2	V
	$I_{SINK} = 200mA$		2.5			2.5		V
	$V_{CC} = 5V$							
	$I_{SINK} = 8mA$		0.1	0.2		0.25	0.3	V
	$I_{SINK} = 5mA$		0.05	0.15		0.15	0.25	V
Output voltage (high)	$V_{CC} = 15V$							
	$I_{SOURCE} = 200mA$		12.5			12.5		V
	$I_{SOURCE} = 100mA$	13.0	13.3		12.75	13.3		V
	$V_{CC} = 5V$							
	$I_{SOURCE} = 100mA$	3.0	3.3		2.75	3.3		V
Rise time of output			100	200		100	300	ns
Fall time of output			100	200		100	300	ns
Discharge leakage current			20	100		20	100	nA
Matching characteristics[4]								
Initial accuracy[2]			0.5	1.0		1.0	2.0	%
Drift with temperature			10			10		ppm/°C
Drift with supply voltage			0.1	0.2		0.2	0.5	%/V

NOTES

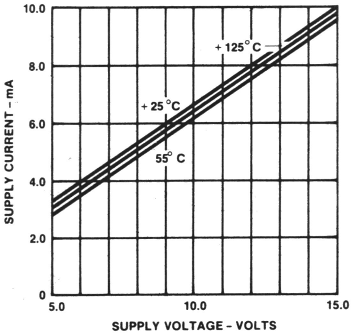
1. Supply current when output is high is typically 1.0mA less.
2. Tested at V_{CC} = 5V and V_{CC} = 15V.
3. This will determine the maximum value of $R_A + R_B$. For 15V operation, the maximum total R = 10 meg-ohms, and for 5V operation, the max. total R = 3.4 meg-ohms.
4. Matching chafactristics refer to the difference between performance characteristics for each timer section in the monostable mode.
5. Specified with trigger input high.

TYPICAL PERFORMANCE CHARACTERISTICS

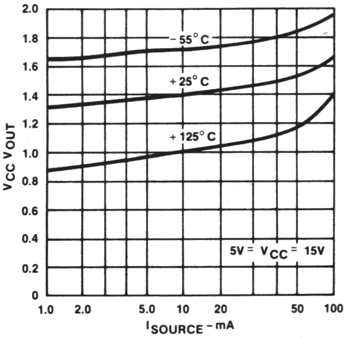
MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



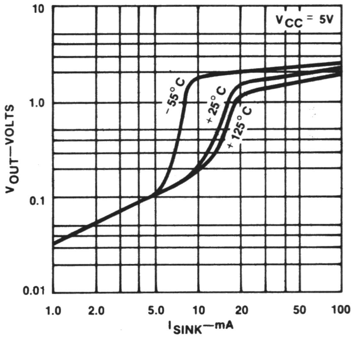
SUPPLY CURRENT vs SUPPLY VOLTAGE



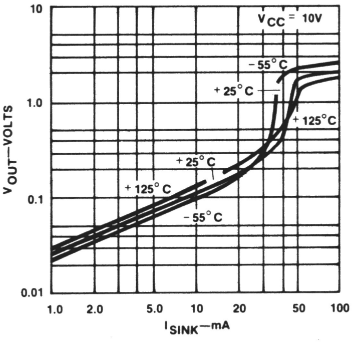
HIGH OUTPUT VOLTAGE DROP vs OUTPUT SOURCE CURRENT



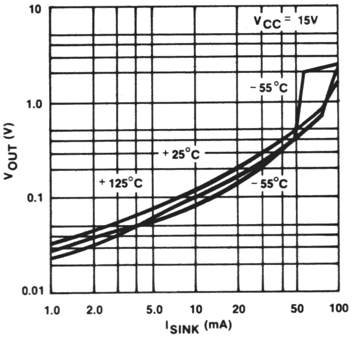
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



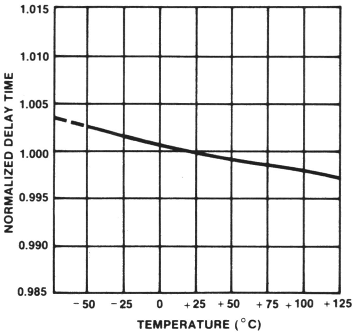
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



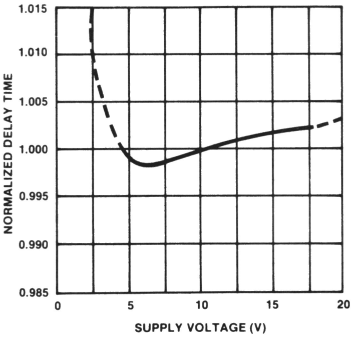
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



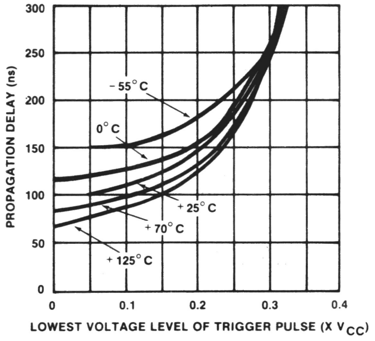
DELAY TIME vs TEMPERATURE



DELAY TIME vs SUPPLY VOLTAGE



PROPAGATION DELAY vs VOLTAGE LEVEL OF TRIGGER PULSE



DUAL TIMER

NE/SE556-1, SE556-1C

SE556-1N,F • NE556-1N,F • SE556-1CN,F

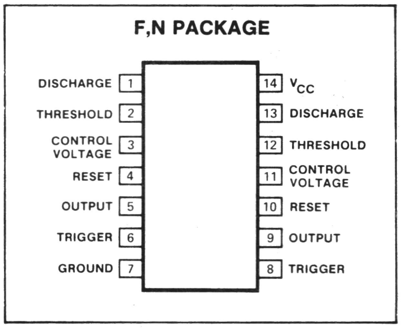
FEATURES

- Turn off time less than 2μS
- Maximum operating frequency greater than 500kHz
- Timing from microseconds to hours
- Replaces two 555 timers
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per °C

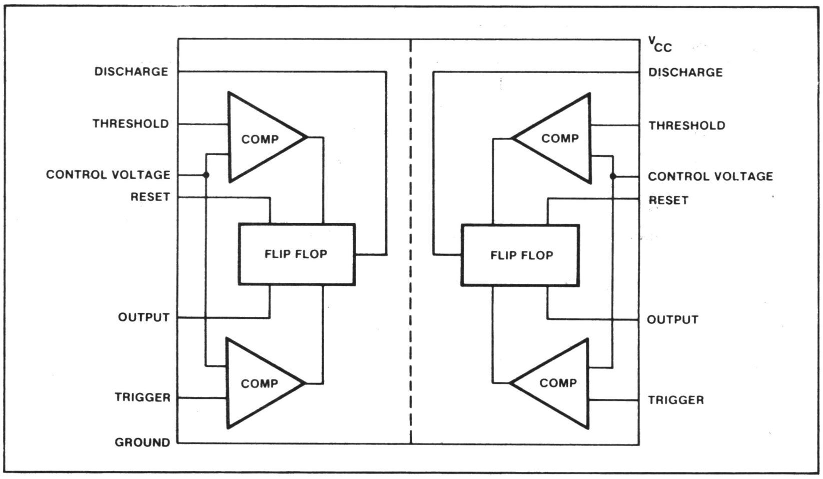
APPLICATIONS

- Precision timing
- Sequential timing
- Pulse shaping
- Pulse generator
- Missing pulse detector
- Tone burst generator
- Pulse width modulation
- Time delay generator
- Frequency division
- Industrial controls
- Pulse position modulation
- Appliance timing
- Traffic light control
- Touch tone encoder

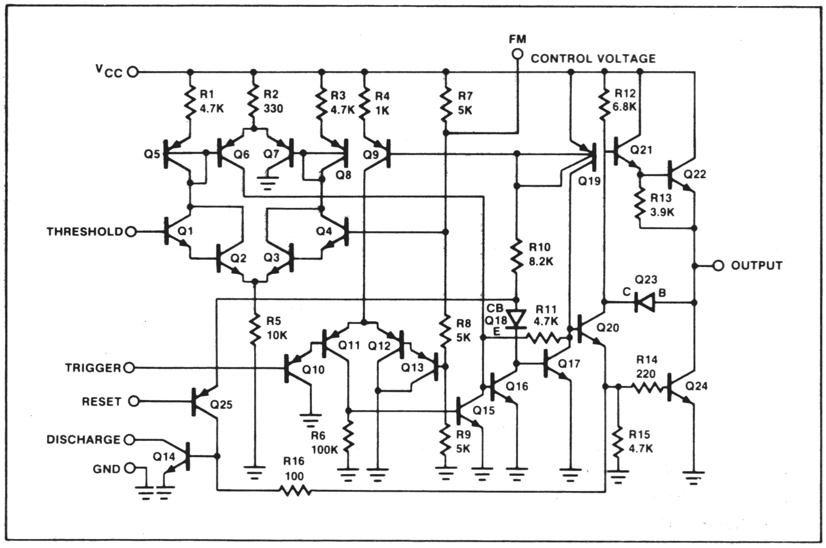
PIN CONFIGURATION


F,N PACKAGE
DISCHARGE 1
THRESHOLD 2
CONTROL VOLTAGE 3
RESET 4
OUTPUT 5
TRIGGER 6
GROUND 7
14 V$_{CC}$
13 DISCHARGE
12 THRESHOLD
11 CONTROL VOLTAGE
10 RESET
9 OUTPUT
8 TRIGGER

BLOCK DIAGRAM


DISCHARGE
THRESHOLD
CONTROL VOLTAGE
RESET
OUTPUT
TRIGGER
GROUND
COMP
FLIP FLOP
COMP
V$_{CC}$
DISCHARGE
THRESHOLD
CONTROL VOLTAGE
RESET
OUTPUT
TRIGGER
COMP
FLIP FLOP
COMP

EQUIVALENT SCHEMATIC (Shown for one circuit only)


V$_{CC}$
FM
CONTROL VOLTAGE
R1 4.7K
R2 330
R3 4.7K
R4 1K
R7 5K
R12 6.8K
Q5
Q6
Q7
Q8
Q9
Q19
Q21
Q22
R13 3.9K
THRESHOLD
Q1
Q2
Q3
Q4
R10 8.2K
OUTPUT
Q23
C
B
CB
Q18
E
R11 4.7K
Q20
R5 10K
R8 5K
Q11
Q12
Q13
Q10
Q17
Q16
Q15
R14 220
Q24
TRIGGER
RESET
Q25
DISCHARGE
Q14
GND
R6 100K
R9 5K
R15 4.7K
R16 100

SE556-1N,F • NE556-1N,F • SE556-1CN,F

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
SE556-1	+18	V
NE556-1, SE556-1C	+16	V
Power dissipation	1.20	W
Operating temperature range		
NE556-1	0 to +70	°C
SE556-1, SE556-1C	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60 sec)	+300	°C

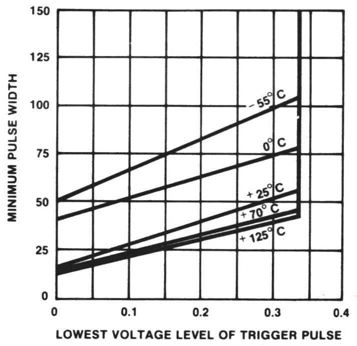
ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +5V to +15V unless otherwise specified.

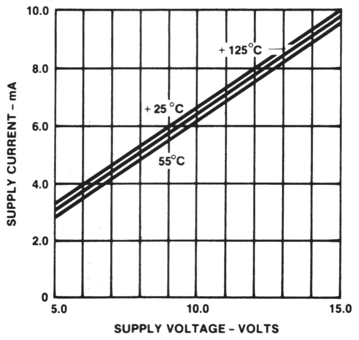
PARAMETER	TEST CONDITIONS	SE556-1			NE556-1/SE556-1C			UNITS
		Min	Typ	Max	Min	Typ	Max	
Supply voltage		4.5		18	4.5		16	V
Supply current (low state)[1]	V_{CC} = 5V R_L = ∞		6	10		6	12	mA
	V_{CC} = 15V R_L = ∞		20	24		20	30	mA
Timing error (monostable)	R_A = 2kΩ to 100kΩ							
Initial accuracy[2]	C = 0.1µF		0.5	1.5		0.75	3.0	%
Drift with temperature			30	100		50		ppm/°C
Drift with supply voltage			0.05	0.2		0.1	0.5	%/V
Timing error (astable)	R_A, R_B = 1kΩ to 100kΩ							
Initial accuracy[2]	C = 0.1µF		1.5			2.25		%
Drift with temperature	V_{CC} = 15V		90			150		ppm/°C
Drift with supply voltage			0.15			0.3		%/V
Control voltage level	V_{CC} = 15V	9.6	10.0	10.4	9.0	10.0	11.0	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4.0	V
Threshold voltage	V_{CC} = 15V	9.4	10.0	10.6	8.8	10.0	11.2	V
	V_{CC} = 5V	2.7	3.33	4.0	2.4	3.33	4.2	V
Threshold current[3]			30	250		30	250	nA
Trigger voltage	V_{CC} = 15V	4.8	5.0	5.2	4.5	5.0	5.6	V
	V_{CC} = 5V	1.45	1.67	1.9	1.1	1.67	2.2	V
Trigger current	V_{TRIG} = 0V		0.5	0.9		0.5	2.0	µA
Reset voltage[5]		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset current			0.1	0.4		0.1	0.6	mA
Reset current	V_{RESET} = 0V		0.4	1.0		0.4	1.5	mA
Output voltage (low)	V_{CC} = 15V							
	I_{SINK} = 10mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100mA		0.8	1.2		2.0	2.5	V
	I_{SINK} = 200mA		2.5			2.5		V
	V_{CC} = 5V							
	I_{SINK} = 8mA		0.1	0.2		0.25	0.3	V
	I_{SINK} = 5mA		0.05	0.15		0.15	0.25	V
Output voltage (high)	V_{CC} = 15V							
	I_{SOURCE} = 200mA		12.5			12.5		V
	I_{SOURCE} = 100mA	13.0	13.3		12.75	13.3		V
	V_{CC} = 5V							
	I_{SOURCE} = 100mA	3.0	3.3		2.75	3.3		V
Turn off time[6]	V_{RESET} = V_{CC}		0.5	2.0		0.5		µs
Rise time of output			100	200		100	300	ns
Fall time of output			100	200		100	300	ns
Discharge leakage current			20	100		20	100	nA
Matching characteristics[4]								
Initial accuracy[2]			0.5	1.0		1.0	2.0	%
Drift with temperature			±10			±10		ppm/°C
Drift with supply voltage			0.1	0.2		0.2	0.5	%/V

TYPICAL CHARACTERISTICS

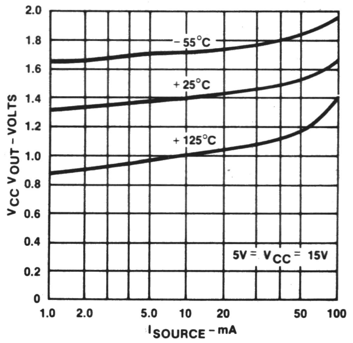
MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



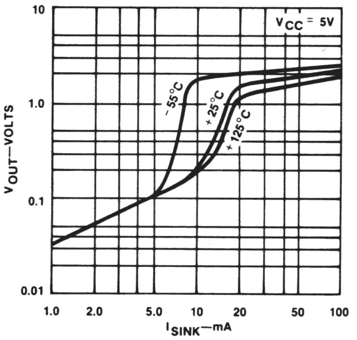
SUPPLY CURRENT vs SUPPLY VOLTAGE



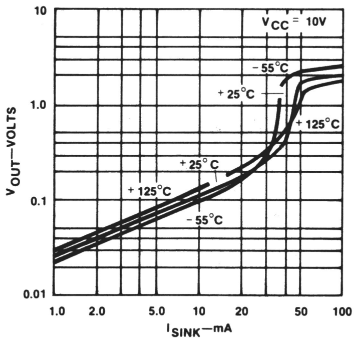
HIGH OUTPUT VOLTAGE DROP vs OUTPUT SOURCE CURRENT



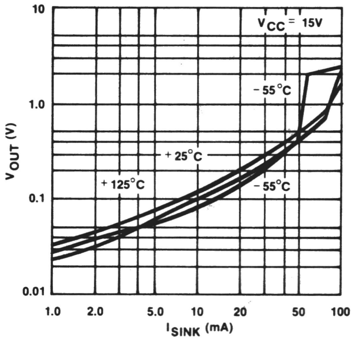
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



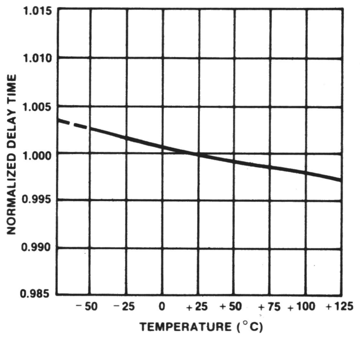
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



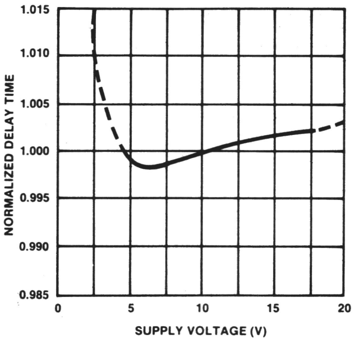
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



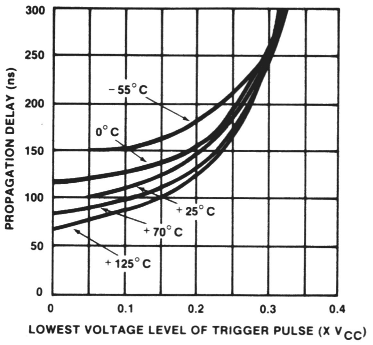
DELAY TIME vs TEMPERATURE



DELAY TIME vs SUPPLY VOLTAGE



PROPAGATION DELAY vs VOLTAGE LEVEL OF TRIGGER PULSE



NOTES

1. Supply current when output is high is typically 1.0mA less.
2. Tested at V_{CC} = 5V and V_{CC} = 15V.
3. This will determine the maximum value of $R_A + R_B$. For 15V operation, the maximum total R = 10 megohms, and for 5V operation, the max. total R = 3.4 megohms.
4. Matching characteristics refer to the difference between performance characteristics for each timer section in the monostable mode.
5. Specified with trigger input high.
6. Time measured from a positive going input pulse from 0 to 0.8 V_{CC} into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

DESCRIPTION

The SA/SE/NE558 Quad Timers are monolithic timing devices which can be used to produce four entirely independent timing functions. The 558 output sinks current. These highly stable, general purpose controllers can be used in a monostable mode to produce accurate time delays, from microseconds to hours. In the time delay mode of operation, the time is precisely controlled by one external resistor and one capacitor. A stable operation can be achieved by using two of the four timer sections.

The four timing sections in the 558 are edge triggered; therefore, when connected in tandem for sequential timing applications, no coupling capacitors are required. Output current capability of 100mA is provided in both devices.

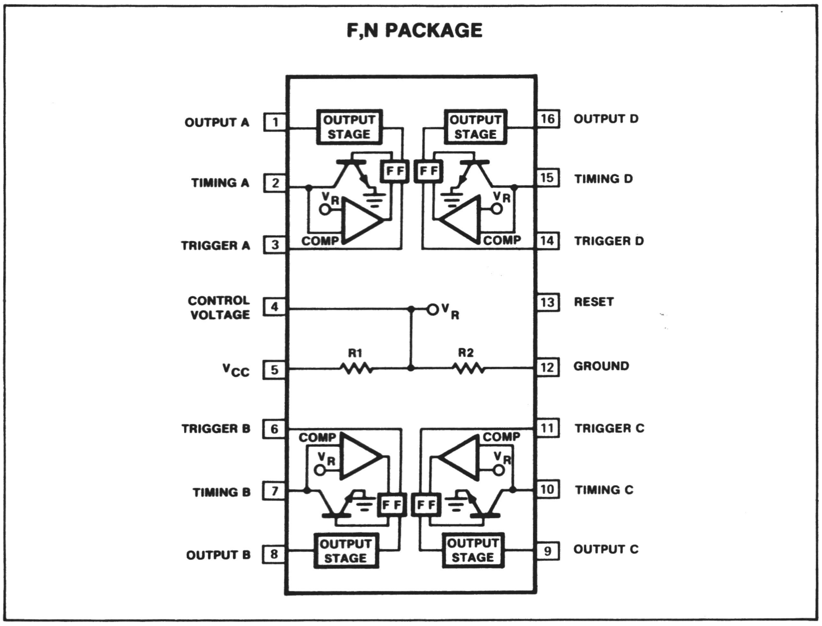
FEATURES

- **100mA output current per section**
- **Edge triggered (no coupling capacitor)**
- **Output independent of trigger conditions**
- **Wide supply voltage range 4.5V to 18V**
- **Timer intervals from microseconds to hours**
- **Time period equals RC**
- **Military qualifications pending**

APPLICATIONS

- **Sequential timing**
- **Time delay generation**
- **Precision timing**
- **Industrial controls**
- **Quad one-shot**

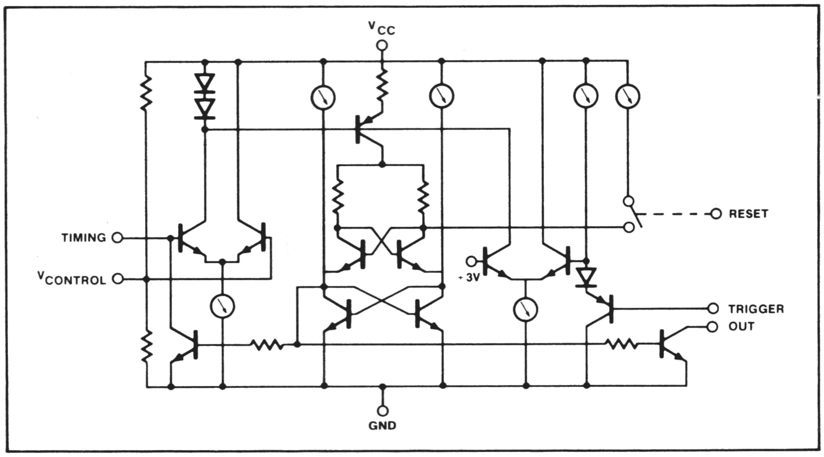
PIN CONFIGURATION


F,N PACKAGE
OUTPUT A 1
TIMING A 2
TRIGGER A 3
CONTROL VOLTAGE 4
VCC 5
TRIGGER B 6
TIMING B 7
OUTPUT B 8
OUTPUT C 9
TIMING C 10
TRIGGER C 11
GROUND 12
RESET 13
TRIGGER D 14
TIMING D 15
OUTPUT D 16
OUTPUT STAGE
FF
COMP
VR
R1
R2

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
SE558, SE559	+18	V
NE558, NE559	+16	V
Power dissipation	1.25	W
Operating temperature range		
NE558, NE559	0 to +70	°C
SE558	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	+300	°C

558 EQUIVALENT CIRCUIT


VCC
TIMING
VCONTROL
+3V
RESET
TRIGGER
OUT
GND

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = +5V$ to $+15V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE558			NE558			UNIT
		Min	Typ	Max	Min	Typ	Max	
Supply voltage		4.5		18	4.5		16	V
Supply current (558)	V_{CC} = Reset = 15V		21	32		27	36	mA
(559)	V_{CC} = Reset = 15V		9	16		12	18	mA
Timing accuracy (T = RC)	R = 2kΩ to 100kΩ C = 1μF							
Initial accuracy			1.0	3		2		%
Drift with temperature			150			150		ppm/°C
Drift with supply voltage			0.1			0.1		%/V
Trigger voltage[1]	V_{CC} = 15V	0.8	1.5	2.4	0.8	1.5	2.4	V
Trigger current	Trigger = 0V		5	30		5	100	μA
Reset voltage[2]		0.8	1.5	2.4	0.8	1.5	2.4	V
Reset current	Reset		50	300		50		μA
Threshold voltage			0.63			0.63		xV_{CC}
Threshold leakage			15			15		nA
Output voltage (558)[3]	I_L = 10mA		0.1	0.2		0.1	0.4	V
	I_L = 100mA		0.7	1.5		1.0	2.0	V
Output voltage (559)[4]	I_L = 10mA	13	13.6		12.5	13.3		V
	I_L = 100mA	12.5	13.3		12.0	13.0		V
Output leakage			10			10		nA
Propagation delay (558)			1.0			1.0		μs
(559)			0.4			0.4		μs
Risetime of output	I_L = 100mA		100			100		ns
Falltime of output	I_L = 100mA		100			100		ns

NOTES

1. The trigger functions only on the falling edge of the trigger pulse only after previously being high. After reset the trigger must be brought high and then low to implement triggering.
2. For reset below 0.8 volts, outputs set low and trigger inhibited. For reset above 2.4 volts, trigger enabled.
3. The 558 output structure is open collector which requires a pull up resistor to V_{CC} to sink current. The output is normally low sinking current.
4. The 559 output structure is a darlington emitter follower which requires a pull down resistor to ground to source current. The output is normally low and sources current only when switched high.

SECTION 5
COMPARATORS

Section 5—COMPARATORS

NE/SE521 High Speed Dual Differential Comparator/Sense Amp 139
NE/SE522 High Speed Dual Differential Comparator/Sense Amp 143
NE/SE527 Voltage Comparator 147
NE/SE529 Voltage Comparator 151
LM111 Voltage Comparator . . . . . *
LM211 Voltage Comparator . . . . . *
LM311 Voltage Comparator . . . . . *
LM119 Dual Voltage Comparator . . . . . *
LM219 Dual Voltage Comparator . . . . . *
LM319 Dual Voltage Comparator . . . . . *
LM139 Quad Voltage Comparator . . . . . *
LM239 Quad Voltage Comparator . . . . . *
LM339 Quad Voltage Comparator . . . . . *
MC3302 Quad Voltage Comparator . . . . . *
LM2901 Quad Voltage Comparator . . . . . *
LM193/193A Low Power Dual Voltage Comparator . . . . . *
LM293/293A Low Power Dual Voltage Comparator . . . . . *
LM393/393A Low Power Dual Voltage Comparator . . . . . *
LM2903 Low Power Dual Voltage Comparator . . . . . *

NOTE

*Any product listed in this section but not incorporated within the text may be obtained by writing Information Services at Signetics, 811 E. Arques, M/S 027, Sunnyvale, California 94086, or by calling (408) 746-1682.

NE/SE521-F,N

FEATURES

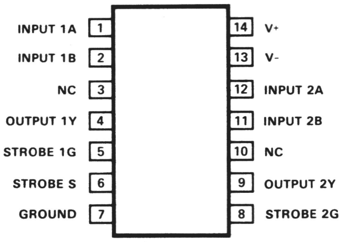
- 12ns maximum guaranteed propagation delay
- $20\mu A$ maximum input bias current
- TTL compatible strobes and outputs
- Large common mode input voltage range
- Operates from standard supply voltages
- Military qualifications pending

APPLICATIONS

- MOS memory sense amp
- A-to-D conversion
- High speed line receiver

PIN CONFIGURATION

F,N PACKAGE

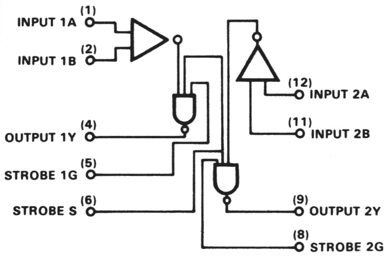

INPUT 1A 1
INPUT 1B 2
NC 3
OUTPUT 1Y 4
STROBE 1G 5
STROBE S 6
GROUND 7
14 V+
13 V-
12 INPUT 2A
11 INPUT 2B
10 NC
9 OUTPUT 2Y
8 STROBE 2G

Order Part No.
NE521 F,N
SE521 F,N

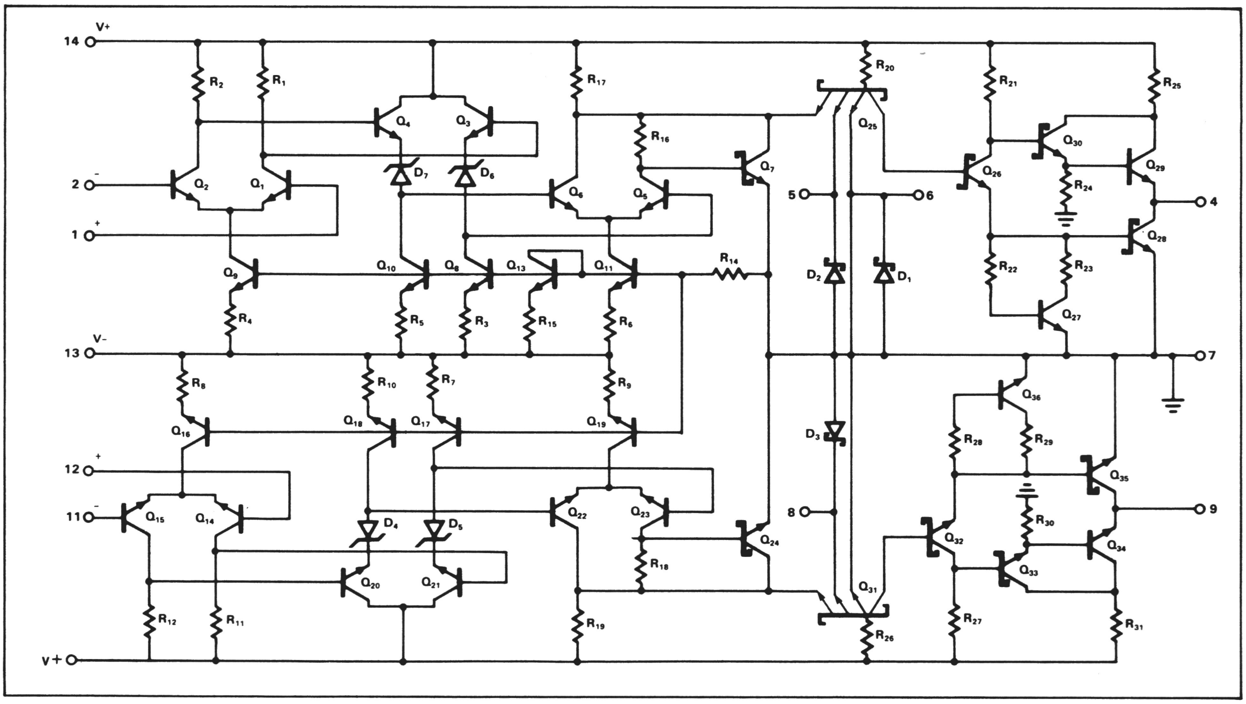
ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
	Supply voltage		V
V+	Positive	+7	
V-	Negative	-7	
V_{IDR}	Differential input voltage	±6	V
V_{IN}	Input voltage		V
	Common mode	±5	
	Strobe/gate	+5.25	
P_D	Power dissipation	600	mW
T_A	Operating temperature range	0 to 70	°C
T_{stg}	Storage temperature range	-65 to +150	°C
	Lead temperature (solder, 60 sec)	+300	°C

BLOCK DIAGRAM


INPUT 1A (1)
INPUT 1B (2)
OUTPUT 1Y (4)
STROBE 1G (5)
STROBE S (6)
(12) INPUT 2A
(11) INPUT 2B
(9) OUTPUT 2Y
(8) STROBE 2G

EQUIVALENT SCHEMATIC


V+
14
2 -
1 +
13
V-
12 +
11 -
v+
5
6
4
7
8
9
R1 R2 R3 R4 R5 R6 R7 R8 R9 R10 R11 R12 R14 R15 R16 R17 R18 R19 R20 R21 R22 R23 R24 R25 R26 R27 R28 R29 R30 R31
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 Q13 Q14 Q15 Q16 Q17 Q18 Q19 Q20 Q21 Q22 Q23 Q24 Q25 Q26 Q27 Q28 Q29 Q30 Q31 Q32 Q33 Q34 Q35 Q36
D1 D2 D3 D4 D5 D6 D7

DC ELECTRICAL CHARACTERISTICS $V+ = +5V$, $V- = -5V$, $T_A = 0$ to 70°C unless otherwise specified

PARAMETER		TEST CONDITIONS	SE LIMITS			UNITS
			Min	Typ	Max	
V_{OS}	Input offset voltage	$V+ = +4.5V$, $V- = -4.75V$				mV
	At 25°C			6	7.5	
	Over temperature range				15	
I_{BIAS}	Input bias current	$V+ = +5.5V$, $V- = -5.5V$				μA
	At 25°C			7.5	20	
	Over temperature range				40	
I_{OS}	Input offset current	$V+ = +5.5V$, $V- = -5.5V$				μA
	At 25°C			1.0	5	
	Over temperature range				12	
V_{CM}	Common mode voltage range	$V+ = +4.5V$, $V- = -4.5V$	±3			V
V_{IL}	Low level input voltage					
	At 25°C				0.8	
	Over temperature				0.7	
	Input current	$V+ = +5.5V$, $V- = -5.5V$				
I_{IH}	High	$V_{IH} = 2.7V$				
		1G or 2G strobe			50	μA
		Common strobe S			100	μA
I_{IL}	Low	$V_{IL} = 0.5V$				
		1G or 2G strobe			-2.0	mA
		Common strobe S			-4.0	mA
	Output voltage	$V_{I(S)} = 2.0V$				V
V_{OH}	High	$V+ = +4.5V$, $V- = -4.5V$, $I_{LOAD} = -1mA$	2.5	3.4		
V_{OL}	Low	$V+ = +4.5V$, $V- = -4.5V$, $I_{LOAD} = -10mA$			0.5	
		$T_A = 25°C$				
	Supply voltage					V
$V+$	Positive		4.5	5.0	5.5	
$V-$	Negative		-4.5	-5.0	-5.5	
	Supply current	$V+ = 5.5V$, $V- = -5.5V$, $T_A = 25°C$				mA
I_{CC+}	Positive			27	50	
I_{CC-}	Negative			-15	-28	
I_{SC}	Short circuit output current		-35		-125	μA

DC ELECTRICAL CHARACTERISTICS (Cont'd) V+ = +5V, V− = −5V, T_A = 0 to 70°C unless otherwise specified

PARAMETER		TEST CONDITIONS	NE LIMITS			UNITS
			Min	Typ	Max	
V_{OS}	Input offset voltage	V+ = +4.75V, V− = −4.75V				mV
	At 25°C			6	7.5	
	Over temperature range				10	
I_{BIAS}	Input bias current	V+ = +5.25V, V− = −5.25V				μA
	At 25°C			7.5	20	
	Over temperature range				40	
I_{OS}	Input offset current	V+ = +5.25V, V− = −5.25V				μA
	At 25°C			1.0	5	
	Over temperature range				12	
V_{CM}	Common mode voltage range	V+ = +4.75V, V− = −4.75V	±3			V
	Input current	V+ = +5.25V, V− = −5.25V				
I_{IH}	High	V_{IH} = 2.7V				
		1G or 2G strobe			50	μA
		Common strobe S			100	μA
I_{IL}	Low	V_{IL} = 0.5V				
		1G or 2G strobe			−2.0	mA
		Common strobe S			−4.0	mA
	Output voltage	$V_{I(S)}$ = 2.0V				V
V_{OH}	High	V+ = +4.75V, V− = −4.75V, I_{LOAD} = −1mA	2.7	3.4		
V_{OL}	Low	V+ = +5.25V, V− = −5.25V, I_{LOAD} = 20mA			0.5	
	Supply voltage					V
V+	Positive		4.75	5.0	5.25	
V−	Negative		−4.75	−5.0	−5.25	
	Supply current	V+ = 5.25V, V− = −5.25V, T_A = 25°C				mA
I_{CC+}	Positive			27	50	
I_{CC-}	Negative			−15	−28	
I_{SC}	Short circuit output current		−40		−100	μA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, R_L = 280Ω C_L = 15pF V+ = +5V V− = −5V

PARAMETER		FROM INPUT	TO OUTPUT	LIMITS			UNIT
				Min	Typ	Max	
Large Signal Switching Speed							
	Propagation delay						ns
$t_{PLH(D)}$	Low to high[1]	Amp	Output		8	12	
$t_{PHL(D)}$	High to low[1]	Amp	Output		6	9	
$t_{PLH(S)}$	Low to high[2]	Strobe	Output		4.5	6	
$t_{PHL(S)}$	High to low[2]	Strobe	Output		3.0	4.5	
	Maximum operating frequency			40	55		MHz

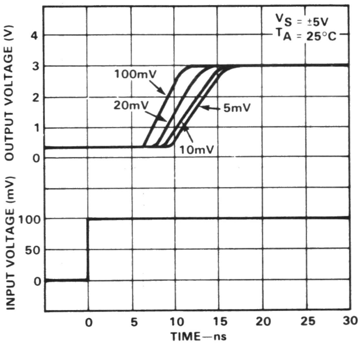
NOTES

1. Response time measured from 0V point of ±100mV p-p 10MHz square wave to the 1.5V point of the output
2. Response time measured from 1.5V point of input to 1.5V point of the output

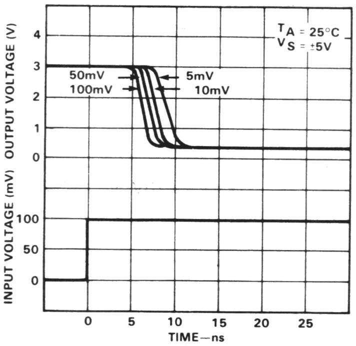
NE / SE521-F,N

TYPICAL PERFORMANCE CHARACTERISTICS

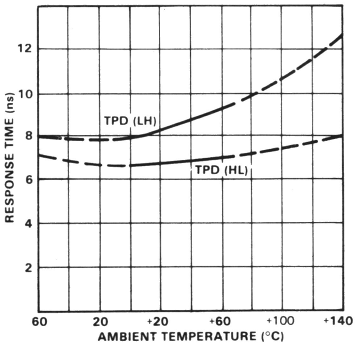
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



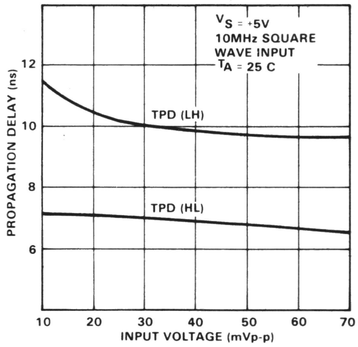
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



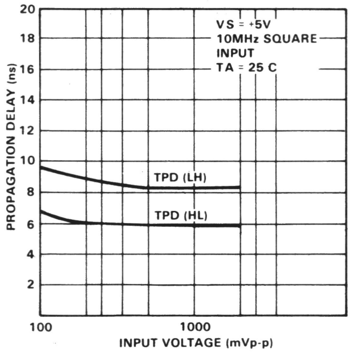
RESPONSE TIME vs TEMPERATURE



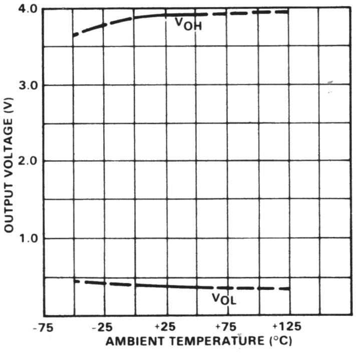
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGE



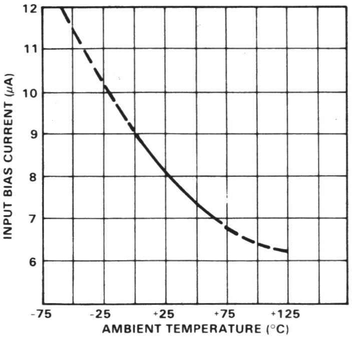
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



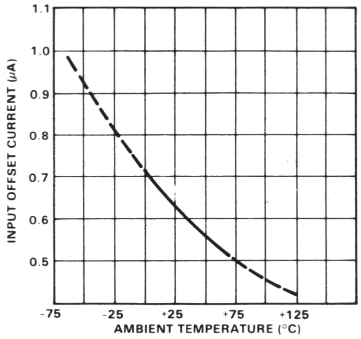
OUTPUT VOLTAGE vs AMBIENT TEMPERATURE



INPUT BIAS CURRENT vs AMBIENT TEMPERATURE



INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE



HIGH SPEED DUAL DIFFERENTIAL COMPARATOR/SENSE AMP NE/SE522

NE522-F,N • SE522-F

FEATURES

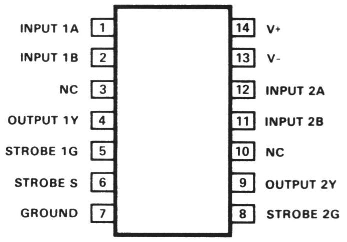
- 15ns maximum guaranteed propagation delay
- 20μA maximum input bias current
- TTL compatible strobes and outputs
- Open collector output for wire-OR'd applications
- Large common mode input voltage range
- Operates from standard supply voltages

APPLICATIONS

- MOS memory sense amp
- A-to-D conversion
- High speed line receiver

PIN CONFIGURATION

F,N PACKAGE


INPUT 1A 1
INPUT 1B 2
NC 3
OUTPUT 1Y 4
STROBE 1G 5
STROBE S 6
GROUND 7
14 V+
13 V-
12 INPUT 2A
11 INPUT 2B
10 NC
9 OUTPUT 2Y
8 STROBE 2G

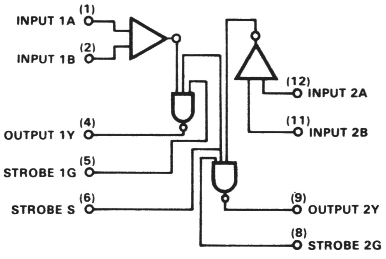
Order Part No.

NE522 F,N
SE522 F

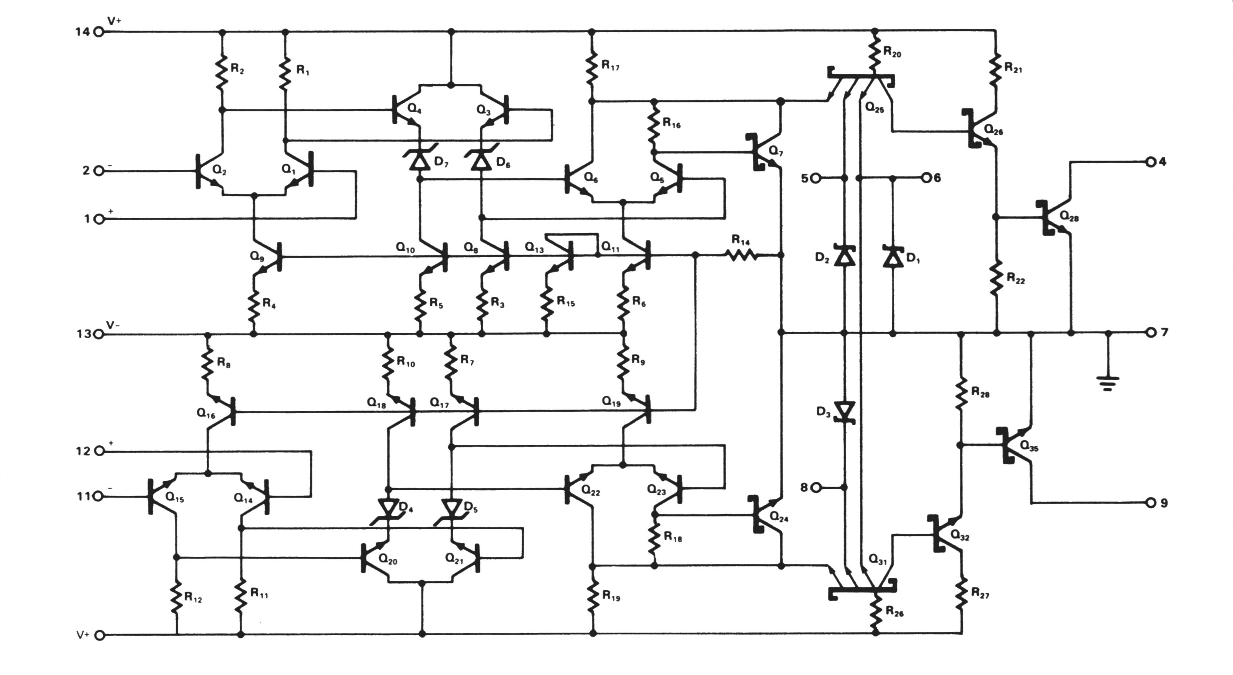
ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
	Supply voltage		V
V+	Positive	+7	
V-	Negative	-7	
V_{IDR}	Differential input voltage	±6	V
V_{IN}	Input voltage		V
	Common mode	±5	
	Strobe/gate	±5.25	
P_D	Power dissipation	600	mW
T_A	Operating temperature range NE	0 to 70	°C
	SE	-55 to +125	
T_{stg}	Storage temperature range	-65 to +150	°C
	Lead temperature (solder, 60 sec)	+300	°C

BLOCK DIAGRAM


INPUT 1A (1)
INPUT 1B (2)
OUTPUT 1Y (4)
STROBE 1G (5)
STROBE S (6)
(12) INPUT 2A
(11) INPUT 2B
(9) OUTPUT 2Y
(8) STROBE 2G

EQUIVALENT SCHEMATIC


14 V+
R2
R1
Q4
Q3
D7
D6
2 -
1 +
Q2
Q1
Q9
Q10
Q8
Q13
Q11
R4
R5
R3
R15
R6
13 V-
R8
R10
R7
R9
Q16
Q18
Q17
Q19
12 +
11 -
Q15
Q14
D4
D5
Q22
Q23
Q20
Q21
R12
R11
R18
R19
V+
R17
R16
Q6
Q5
Q7
R14
R20
Q25
R21
Q26
5
6
D2
D1
4
Q28
R22
7
D3
R28
Q35
9
8
Q24
Q32
Q31
R26
R27

DC ELECTRICAL CHARACTERISTICS ±5V ±10%, T_A = -55 to 125°C unless otherwise specified

PARAMETER		TEST CONDITIONS	SE LIMITS			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage	V+ = +4.5V, V- = -4.5V				mV
	At 25°C			6	7.5	
	Over temperature range				15.	
I_{BIAS}	Input bias current	V+ = +5.5V, V- = -5.5V				μA
	At 25°C			7.5	20.	
	Over temperature range				40.	
I_{OS}	Input offset current	V+ = +5.5V, V- = -5.5V				μA
	At 25°C			1.0	5.	
	Over temperature range				12.	
V_{CM}	Common mode voltage range	V+ = +4.5V, V- = -4.5V	±3			V
	Input current	V+ = +5.5V, V- = -5.5V				
I_{IH}	High	V_{IH} = 2.7V				
		1G or 2G strobe			50	μA
		Common strobe S			100	μA
I_{IL}	Low	V_{IL} = 0.5V				
		1G 2G strobe			-2	mA
		Common strobe S			-4	mA
	Output voltage					V
V_{OL}	Low	V+ = +4.5V, V- = -4.5V				
		I_{OL} = 20mA, T_A = 25°C			.5	
		I_{OL} = 10mA			.5	
	Output current					μA
I_{OH}	High	V_{CC+} = +4.5, V_{CC-} = -4.5V, V_{OH} = 5.5V			250	
	Supply voltage					V
V+	Positive		4.5	5.0	5.5	
V-	Negative		-4.5	-5.0	-5.5	
	Supply current	V+ = 5.5V, V- = -5.5V				mA
I_{CC+}	Positive			27	50	
I_{CC-}	Negative			-15	-28	

DC ELECTRICAL CHARACTERISTICS (Cont'd) ±5V ±5%, T_A = 0 to 70°C unless otherwise specified

PARAMETER		TEST CONDITIONS	NE LIMITS			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage	V+ = +4.75V, V- = -4.75V				mV
	At 25°C			6	7.5	
	Over temperature range				10	
I_{BIAS}	Input bias current	V+ = +5.25V, V- = -5.25V				μA
	At 25°C			7.5	20	
	Over temperature range				40	
I_{OS}	Input offset current	V+ = +5.25V, V- = -5.25V				μA
	At 25°C			1.0	5	
	Over temperature range				12	
V_{CM}	Common mode voltage range	V+ = +4.75V, V- = -4.75V	±3			V
	Input current	V+ = +5.25V, V- = -5.25V				
I_{IH}	High	V_{IH} = 2.7V				
		1G or 2G strobe			50	μA
		Common strobe S			100	μA
I_{IL}	Low	V_{IL} = 0.5V				
		1G 2G strobe			-2.0	mA
		Common strobe S			-4.0	mA
	Output voltage					V
V_{OL}	Low	V+ = +5.25V, V- = -5.25V, $V_{I(S)}$ = 2.0V			0.5	
	Output current					μA
I_{OH}	High	I_{LOAD} = 20mA, V_{CC+} = +4.75, V_{CC-} = -4.75V, V_{OH} = 5.25V			250	
	Supply voltage					V
V+	Positive		4.75	5.0	5.25	
V-	Negative		-4.75	-5.0	-5.25	
	Supply current	V+ = 5.25V, V- = -5.25V, T_A = 25°C				mA
I_{CC+}	Positive			27	50	
I_{CC-}	Negative			-15	-28	

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, R_L = 280Ω, C_L = 15pF

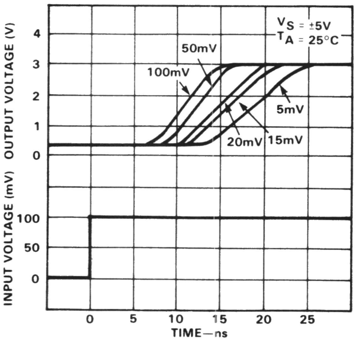
PARAMETER		FROM INPUT	TO OUTPUT	LIMITS			UNIT
				Min	Typ	Max	
	Input resistance				4		kΩ
	Input capacitance				3		pF
Large Signal Switching Speed							
	Propagation delay						ns
$t_{PLH(D)}$	Low to high[1]	Amp	Output		10	15	
$t_{PHL(D)}$	High to low[1]	Amp	Output		8	12	
$t_{PLH(S)}$	Low to high[2]	Strobe	Output		6	10	
$t_{PHL(S)}$	High to low[2]	Strobe	Output		5	8	
	Maximum operating frequency			25	35		MHz
Small Signal Switching Speed							
	Propagation delay						ns
$t_{PLH(D)}$	Low to high[3]	Amp	Output		17	25	
$t_{PHL(D)}$	High to low[3]	Amp	Output		11	17	

NOTES

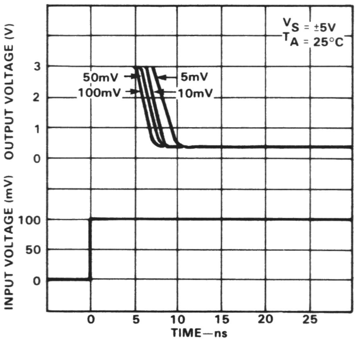
1. Response time measured from 0V point of ±100mV p-p 10MHz square wave to the 1.5V point of the output
2. Response time measured from 1.5V point of input to 1.5V point of the output
3. Response time measured from the start of a 100mV input step with 5mV overdrive to the 1.5V point of the output

TYPICAL PERFORMANCE CHARACTERISTICS

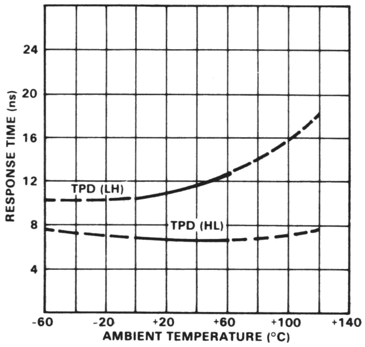
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



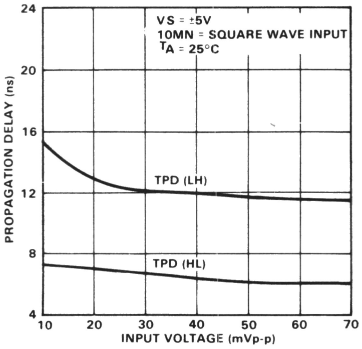
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



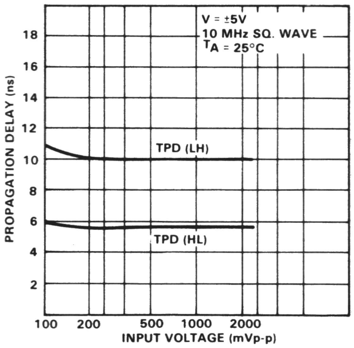
RESPONSE TIME vs TEMPERATURE



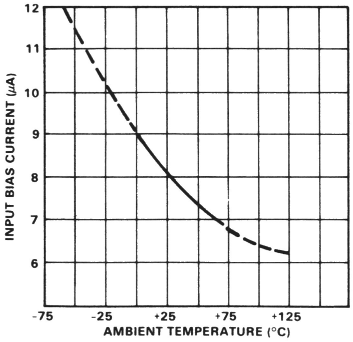
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



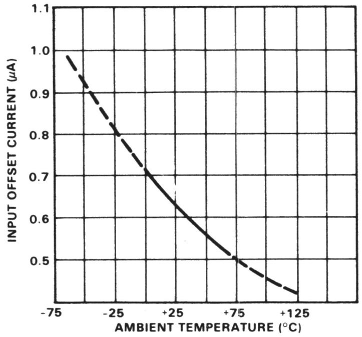
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



INPUT BIAS CURRENT vs AMBIENT TEMPERATURE



INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE



VOLTAGE COMPARATOR NE/SE527

NE527-F,H,N/SE527-F,H,N

DESCRIPTION

The SE/NE527 is a high speed analog voltage comparator which, in the first time mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed T²L gates with a precision linear amplifier on a single monolithic chip. The SE/NE527 is similar in design to the Signetics SE/NE529 voltage comparator except that it incorporates a "Emitter Follower" input stage for extremely low input currents. This opens the door to a whole new range of applications for analog voltage comparators.

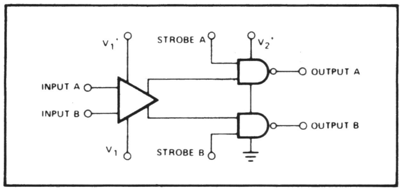
FEATURES

- **15ns propagation delay**
- **Complementary output gates**
- **TTL or ECL compatible outputs**
- **Wide common mode and differential voltage range**
- **Mil std 883A,B,C available**

APPLICATIONS

- **A/D conversion**
- **ECL to TTL interface**
- **TTL to ECL interface**
- **Memory sensing**
- **Optical data coupling**

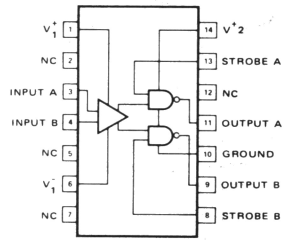
BLOCK DIAGRAM



V_1^+
STROBE A
V_2^+
INPUT A
INPUT B
OUTPUT A
OUTPUT B
V_1^-
STROBE B

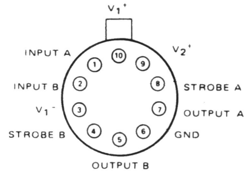
PIN CONFIGURATIONS

F,N PACKAGE



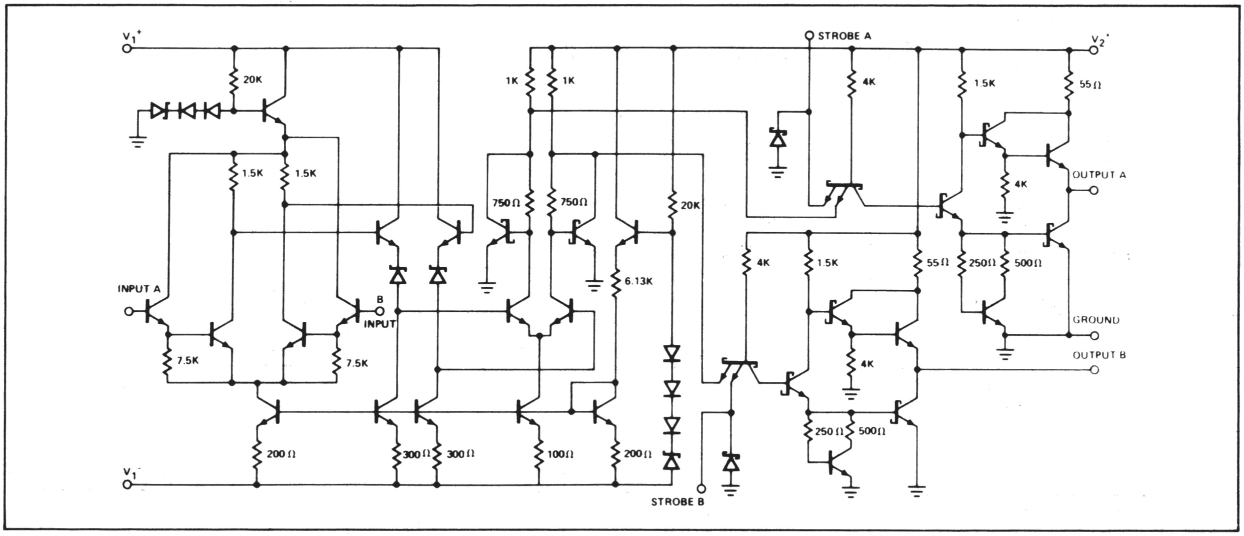
V_1^+ 1
NC 2
INPUT A 3
INPUT B 4
NC 5
V_1^- 6
NC 7
14 V^+_2
13 STROBE A
12 NC
11 OUTPUT A
10 GROUND
9 OUTPUT B
8 STROBE B

H PACKAGE



V_1^+
INPUT A
INPUT B
V_1^-
STROBE B
OUTPUT B
GND
OUTPUT A
STROBE A
V_2^+
1
2
3
4
5
6
7
8
9
10

EQUIVALENT SCHEMATIC



V_1^+
20K
1.5K
1.5K
INPUT A
7.5K
7.5K
B INPUT
200 Ω
300 Ω
300 Ω
100 Ω
200 Ω
V_1^-
1K
1K
750 Ω
750 Ω
20K
6.13K
STROBE A
4K
4K
1.5K
55 Ω
250 Ω
500 Ω
4K
250 Ω
500 Ω
1.5K
55 Ω
V_2^+
OUTPUT A
GROUND
OUTPUT B
STROBE B

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply voltage (V1+)	+15	V
Negative supply voltage (V1-)	-15	V
Gate supply voltage (V2+)	+7	V
Output voltage	+15	V
Differential input voltage	±5	V
Input common mode voltage	±6	V
Power dissipation	600	mW
Operating temperature range		
NE527	0 to +70	°C
SE527	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	+300	°C

DC ELECTRICAL CHARACTERISTICS $V_1^+ = 10V$, $V_1^- = -10V$, $V_2^+ = +5.0V$

PARAMETER	TEST CONDITIONS	SE527			NE527			UNIT
		Min	Typ	Max	Min	Typ	Max	
INPUT CHARACTERISTICS								
Input offset voltage @ 25°C				4			6	mV
Over temperature range				6			10	mV
Input bias current @ 25°C				2			2	μA
Over temperature range				4			4	μA
Input offset current @ 25°C				0.5			0.75	μA
Over temperature range	$V_{IN} = 0V$			1			1	μA
GATE CHARACTERISTICS								
Output voltage								
"1" State	$V_2^+ = 4.75V$, $I_{SOURCE} = -1mA$	2.5	3.3		2.7	3.3		V
"0" State	$V_2^+ = 4.75V$, $I_{SINK} = 10mA$			0.5			0.5	V
Strobe inputs								
"0" Input current	$V_2^+ = 5.25V$, $V_{STROBE} = 0.5V$			-2			-2	mA
"1" Input current @ 25°C	$V_2^+ = 5.25V$, $V_{STROBE} = 2.7V$			50			100	μA
Over temperature range	$V_2^+ = 5.25V$, $V_{STROBE} = 2.7V$			200			200	μA
"0" Input voltage	$V_2^+ = 4.75V$			0.8			0.8	V
"1" Input voltage	$V_2^+ = 4.75V$	2.0			2.0			V
Short circuit								
Output current	$V_2^+ = 5.25V$, $V_{OUT} = 0V$	-18		-70	-18		-70	mA
POWER SUPPLY REQUIREMENTS								
Supply voltage								
V_1^+		5		10	5		10	V
V_1^-		-6		-10	-6		-10	V
V_2^+		4.5	5	5.5	4.75	5	5.25	V
Supply current	$V_1^+ = 10V$, $V_1^- = -10V$ $V_2^+ = 5.25V$							
I_1^+	Over temp.			5			5	mA
I_1^-	Over temp.			10			10	mA
I_2^+	Over temp.			20			20	mA

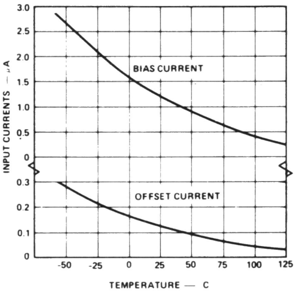
*NOTE

Parameters are guaranteed over the temperature range unless otherwise specified.

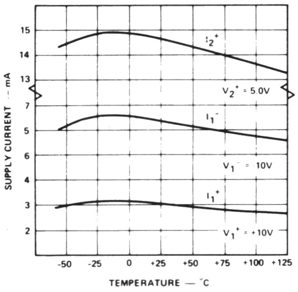
AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Transient response propagation delay time	$V_{IN} = \pm 100mV$ step $T_A = 25°C$				
t_{PLH}			16	26	ns
t_{PHL}			14	24	ns
Delay between output A and B			2	5	ns
Strobe delay time					
t_{on} Turn-on time			6		ns
t_{off} Turn-off time			6		ns

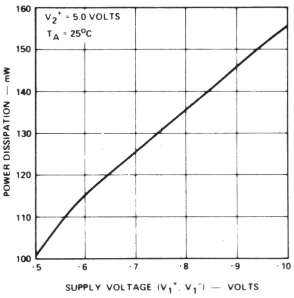
TYPICAL PERFORMANCE CHARACTERISTICS



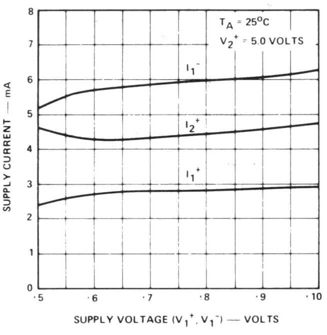
INPUT CURRENTS vs TEMPERATURE



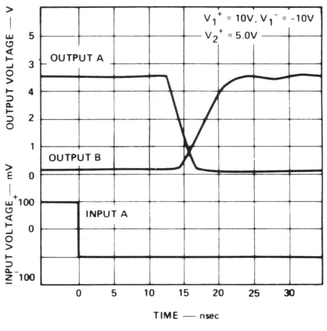
SUPPLY CURRENT vs TEMPERATURE



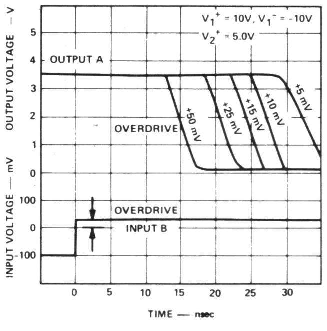
POWER DISSIPATION vs SUPPLY VOLTAGE



SUPPLY CURRENT vs SUPPLY VOLTAGE



OUTPUT PROPAGATION DELAYS



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

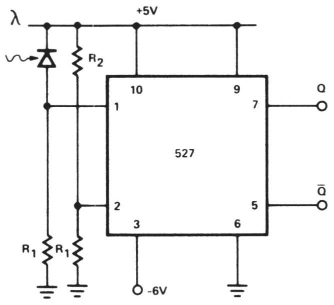
APPLICATIONS

One of the main features of the device is that supply voltages (V1+, V1−) need not be balanced, as indicated in the following diagrams. For proper operation, however, negative supply (V1−) should always be at least six volts more negative than the ground terminal (pin 6). Input Common Mode range should be limited to values of two volts less than the supply voltages (V1+ and V1−) up to a maximum of ±6 volts as supply voltages are increased.

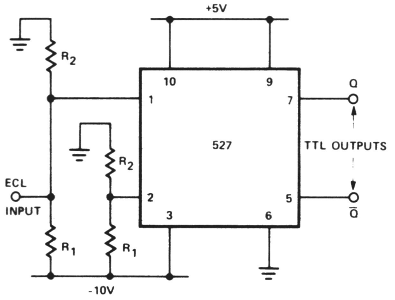
It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

TYPICAL APPLICATIONS

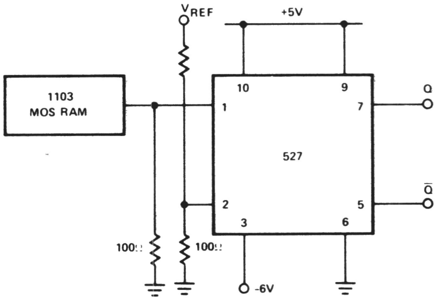
PHOTODIODE DETECTOR


λ
+5V
R2
10
9
1
7
Q
527
Q̄
2
5
3
6
R1
R1
-6V

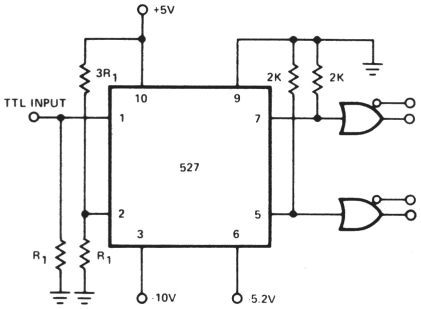
ECL TO TTL INTERFACE


+5V
R2
10
9
1
7
Q
527
R2
TTL OUTPUTS
ECL
INPUT
2
5
3
6
Q̄
R1
R1
-10V

MOS MEMORY SENSE AMP


VREF
+5V
1103
MOS RAM
10
9
1
7
Q
527
Q̄
2
5
3
6
100Ω
100Ω
-6V

TTL TO ECL INTERFACE


+5V
3R1
2K
2K
TTL INPUT
10
9
1
7
527
2
5
3
6
R1
R1
-10V
-5.2V

VOLTAGE COMPARATOR NE/SE529

NE529-F,H,N/SE529-F,H

DESCRIPTION

The SE/NE529 is a high speed analog voltage comparator which, for the first time mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed T²L gates with a precision linear amplifier on a single monolithic chip.

FEATURES

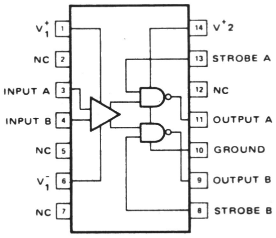
- **10ns propagation delay**
- **Complementary output gates**
- **TTL or ECL compatible outputs**
- **Wide common mode and differential voltage range**

APPLICATIONS

- **A/D conversion**
- **ECL to TTL interface**
- **TTL to ECL interface**
- **Memory sensing**
- **Optical data coupling**
- **Mil std 883A,B,C available**

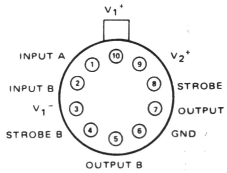
PIN CONFIGURATION

F,N PACKAGE


V_1^+ 1
NC 2
INPUT A 3
INPUT B 4
NC 5
V_1^- 6
NC 7
14 V^+2
13 STROBE A
12 NC
11 OUTPUT A
10 GROUND
9 OUTPUT B
8 STROBE B

ORDER PART NO.
NE/SE529F,NE529N

H PACKAGE

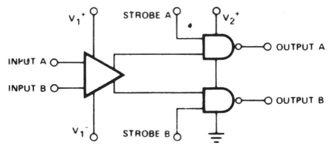

V_1^+
INPUT A
INPUT B
V_1^-
STROBE B
OUTPUT B
GND
OUTPUT A
STROBE A
V_2^+
1
2
3
4
5
6
7
8
9
10

ORDER PART NO.
NE/SE529H

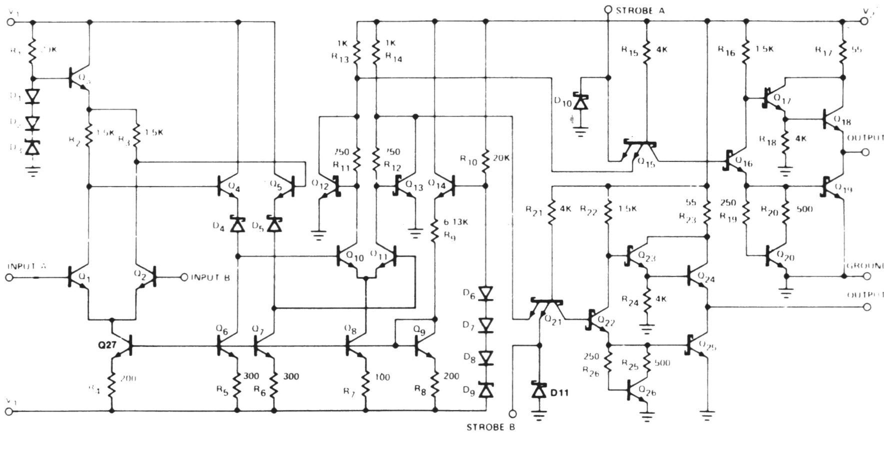
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply voltage (V1+)	+15	V
Negative supply voltage (V1-)	-15	V
Gate supply voltage (V2+)	+7	V
Output voltage	+15	V
Differential input voltage	±5	V
Input common mode voltage	±6	V
Power dissipation	600	mW
Operating temperature range		
NE529	0 to +70	°C
SE529	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60 sec)	+300	°C

BLOCK DIAGRAM


V_1^+
STROBE A
V_2^+
OUTPUT A
INPUT A
INPUT B
OUTPUT B
V_1^-
STROBE B

EQUIVALENT SCHEMATIC


STROBE A
STROBE B
INPUT A
INPUT B
OUTPUT A
OUTPUT B
GROUND
Q27
D11

DC ELECTRICAL CHARACTERISTICS $V_1+ = +10V$, $V_2+ = +5.0V$, $V_1- = -10V$

PARAMETER	TEST CONDITIONS	SE529 Min	SE529 Typ	SE529 Max	NE529 Min	NE529 Typ	NE529 Max	UNIT
INPUT CHARACTERISTICS								
Input offset voltage @25°C				4			6	mV
Over temperature range				6			10	mV
Input bias current @25°C			5	12		5	20	μA
Over temperature range	$V_{IN} = 0V$			36			50	μA
Input offset current @25°C			2	3		2	5	μA
Over temperature range	$V_{IN} = 0V$			9			15	μA
GATE CHARACTERISTICS								
Output voltage								
"1" state	$V_2+ = 4.75V$, $I_{source} = -1mA$	2.5	3.3		2.7	3.3		V
"0" state	$V_2+ = 4.75V$, $I_{sink} = 10mA$			0.5			0.5	V
Strobe inputs								
"0" input current	$V_2+ = 5.25V$, $V_{strobe} = 0.5V$			-2			-2	mA
"1" input current @25°C	$V_2+ = 5.25V$, $V_{strobe} = 2.7V$			50			100	μA
Over temperature range	$V_2+ = 5.25V$, $V_{strobe} = 2.7V$			200			200	μA
"0" input voltage	$V_2+ = 4.75V$			0.8			0.8	V
"1" input voltage	$V_2+ = 4.75V$	2.0			2.0			V
Short circuit								
Output current	$V_2+ = 5.25V$, $V_{OUT} = 0V$	-18		-70	-18		-70	mA
POWER SUPPLY REQUIREMENTS								
Supply voltage								
V_1+		5		10	5		10	V
V_1-		-6		-10	-6		-10	V
V_2+		4.5	5	5.5	4.75	5	5.25	V
Supply current	$V_1+ = 10V$, $V_1- = -10V$ $V_2+ = 5.25V$							
I_1+	Over temp.			5			5	mA
I_1-	Over temp.			10			10	mA
I_2+	Over temp.			20			20	mA

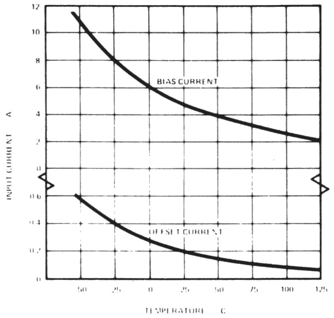
Parameters are guaranteed over the temperature range unless otherwise specified.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$

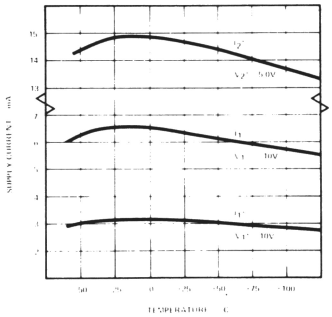
PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
Transient response	$V_{IN} = \pm 100mV$ step				
Propagation delay time					
t_{PLH}			12	22	ns
t_{PHL}			10	20	ns
Delay between output A and B			2	5	ns
Strobe delay time					
t_{ON} turn-on time			6		ns
t_{OFF} turn-off time			6		ns

TYPICAL PERFORMANCE CHARACTERISTICS

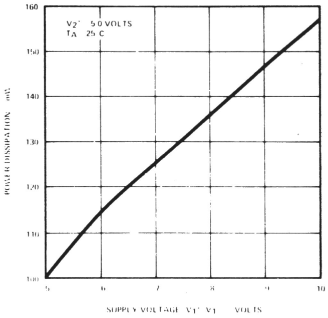
INPUT CURRENTS vs TEMPERATURE



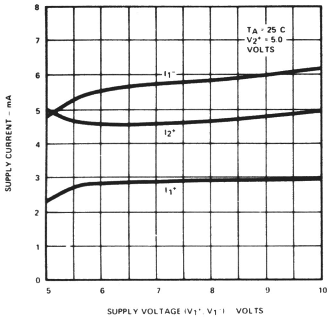
SUPPLY CURRENT vs TEMPERATURE



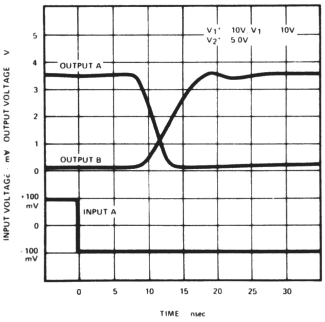
POWER DISSIPATION vs SUPPLY VOLTAGE



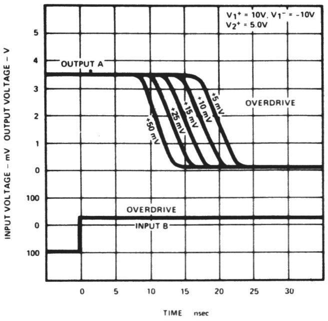
SUPPLY CURRENT vs SUPPLY VOLTAGE



OUTPUT PROPAGATION DELAYS



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



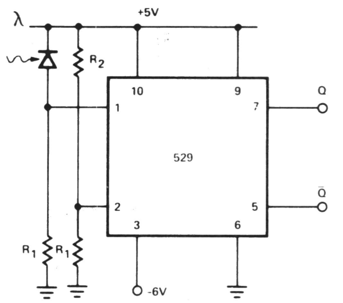
APPLICATIONS

One of the main features of the device is that supply voltages (V1+, V1−) need not be balanced, as indicated in the following diagrams. For proper operation, however, negative supply (V1−) should always be at least five volts more negative than the ground terminal (pin 6). Input Common Mode range should be limited to values of two volts less than the supply voltages (V1+ and V1−) up to a maximum of ±6 volts as supply voltages are increased.

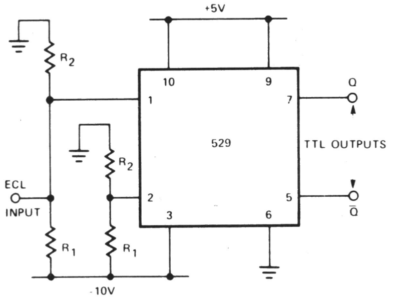
It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

TYPICAL APPLICATIONS

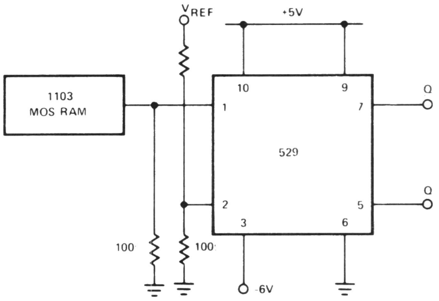
PHOTODIODE DETECTOR


λ
+5V
R2
10
9
1
7
Q
529
Q̄
2
5
3
6
R1
R1
-6V

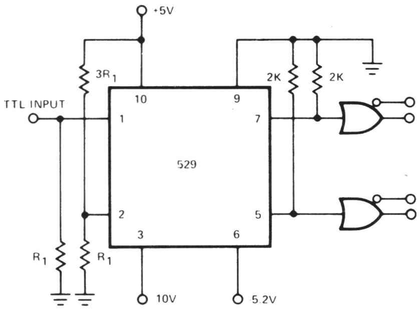
ECL TO TTL INTERFACE


+5V
R2
10
9
Q
1
7
529
TTL OUTPUTS
R2
ECL
INPUT
2
5
Q̄
3
6
R1
R1
-10V

MOS MEMORY SENSE AMP


VREF
+5V
10
9
Q
1103
MOS RAM
1
7
529
Q
2
5
3
6
100
100
-6V

TTL TO ECL INTERFACE


+5V
3R1
2K
2K
TTL INPUT
10
9
1
7
529
2
5
3
6
R1
R1
10V
5.2V

SECTION 6
INTERFACE

Section 6—INTERFACE

NE590 Addressable Peripheral Drivers 159
NE591 Addressable Peripheral Drivers 159
DS3611 High Voltage Peripheral Driver . . . . . *
DS3612 High Voltage Peripheral Driver . . . . . *
DS3613 High Voltage Peripheral Driver . . . . . *
DS3614 High Voltage Peripheral Driver . . . . . *
MC1488 Quad Line Driver 165
MC1489/A Quad Line Receiver 168

NOTE

*Any product listed in this section but not incorporated within the text may be obtained by writing Information Services at Signetics, 811 E. Arques, M/S 027, Sunnyvale, California 94086, or by calling (408) 746-1682.

ADDRESSABLE PERIPHERAL DRIVERS NE590/NE591

PRELIMINARY SPECIFICATION

DESCRIPTION

The NE590/NE591 addressable peripheral drivers are high current latched drivers, similar in function to the 9334 address decoder. The device has 8 darlington power outputs, each capable of 250mA load current. The outputs are turned on or off by respectively loading a logic "1" or logic "0" into the device data input. The required output is defined by a 3 bit address. The device must be enabled by a $\overline{CE}$ input line which also serves the function of further address decoding. A common clear input, $\overline{CLR}$, turns all outputs off when a logic "0" is applied.

The NE590 has 8 open collector darlington outputs which sink current to ground. The device is packaged in a 16 pin molded or cerdip package.

The NE591 has 8 open emitter darlington outputs which source current to an external load from a common collector line, V_S. The V_S line need not necessarily be the same as the 5 volt V_{CC} supply. The device is packaged in an 18 pin molded or cerdip package.

FEATURES

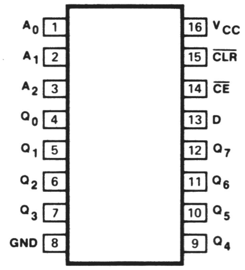
- **8 high current outputs**
- **Low-loading bus compatible inputs**
- **Power-on clear ensures safe operation**
- **NE590 will operate in addressable or demultiplex mode**
- **Allows random (addressed) data entry**
- **Easily expandable**
- **NE590 is pin compatible with 9334.**

APPLICATIONS

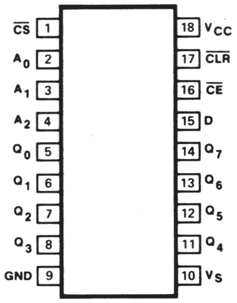
- **Relay driver**
- **Indicator lamp driver**
- **Triac trigger**
- **LED display digit driver**
- **Stepper motor driver**

PIN CONFIGURATIONS

NE590


A0 1
A1 2
A2 3
Q0 4
Q1 5
Q2 6
Q3 7
GND 8
16 VCC
15 CLR
14 CE
13 D
12 Q7
11 Q6
10 Q5
9 Q4

NE591

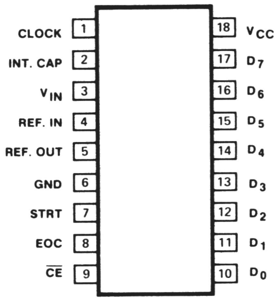

CS 1
A0 2
A1 3
A2 4
Q0 5
Q1 6
Q2 7
Q3 8
GND 9
18 VCC
17 CLR
16 CE
15 D
14 Q7
13 Q6
12 Q5
11 Q4
10 VS

8-BIT ANALOG-TO-DIGITAL CONVERTER NE5030

DESCRIPTION

The NE5030 is an 8-bit A-to-D converter employing the triple-slope technique of conversion. The device includes a voltage reference and clock generator and so constitutes the total conversion system with a minimum of components. Conversion time is approximately 10mS; voltage requirement is a single 5V supply and the data outputs are tri-state bus compatible.

PIN CONFIGURATION


CLOCK 1
INT. CAP 2
VIN 3
REF. IN 4
REF. OUT 5
GND 6
STRT 7
EOC 8
CE 9
18 VCC
17 D7
16 D6
15 D5
14 D4
13 D3
12 D2
11 D1
10 D0

TRUTH TABLE (NE590)

INPUTS						OUTPUTS								MODE
$\overline{CLR}$	$\overline{CE}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
L	H	X	X	X	X	H	H	H	H	H	H	H	H	Clear
L	L	L	L	L	L	H	H	H	H	H	H	H	H	Demultiplex
L	L	H	L	L	L	L	H	H	H	H	H	H	H	
L	L	L	H	L	L	H	H	H	H	H	H	H	H	
L	L	H	H	L	L	H	L	H	H	H	H	H	H	
L	L	L	H	H	H	H	H	H	H	H	H	H	H	
L	L	H	H	H	H	H	H	H	H	H	H	H	L	
H	H	X	X	X	X	Q_{N-1} →								Memory
H	L	L	L	L	L	H	Q_{N-1} →							Addressable Latch
H	L	H	L	L	L	L	Q_{N-1} →							
H	L	L	H	L	L	Q_{N-1}	H	Q_{N-1} →						
H	L	H	H	L	L	Q_{N-1}	L	Q_{N-1}						
H	L	L	H	H	H	Q_{N-1} →							H	
H	L	H	H	H	H	Q_{N-1} →							L	

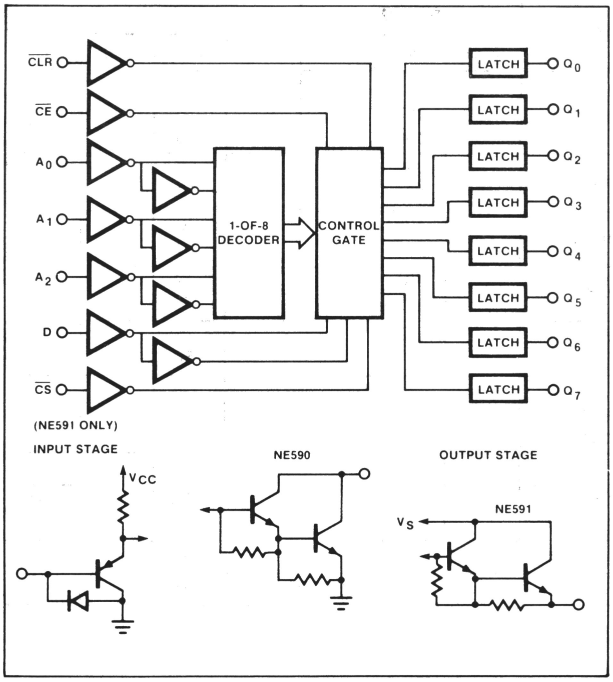
X = Don't care condition
Q_{N-1} = Previous output state
L = Low voltage level/"ON" output state
H = High voltage level/"OFF" output state

TRUTH TABLE (NE591)

INPUTS							OUTPUTS								MODE
$\overline{CLR}$	$\overline{CE}$	$\overline{CS}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
L	X	X	X	X	X	X	L	L	L	L	L	L	L	L	Clear
H	H	H	X	X	X	X	Q_{N-1} →								Memory
H	H	L	X	X	X	X	Q_{N-1} →								
H	L	H	X	X	X	X	Q_{N-1} →								
H	L	L	L	L	L	L	L	Q_{N-1} →							Addressable Latch
H	L	L	H	L	L	L	H	Q_{N-1} →							
H	L	L	L	H	L	L	Q_{N-1}	L	Q_{N-1} →						
H	L	L	H	H	L	L	Q_{N-1}	H	Q_{N-1} →						
H	L	L	L	H	H	H	Q_{N-1} →							L	
H	L	L	H	H	H	H	Q_{N-1} →							H	

X = Don't care
Q_{N-1} = Previous output state
L = Low voltage level/"OFF" output state
H = High voltage level/"ON" output state

BLOCK DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

$T_A = 25°C$ unless otherwise specified.

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7	V
V_{IN}	Input voltage	-0.5 to +15	V
V_{OUT}	Output voltage		V
	NE590	0 to +7	
	NE591	0 to V_{CC}	
V_S	Source bus voltage		V
	NE591 only	-0.5 to +7	
V_S-V_{CC}	Source/supply differential voltage		V
	NE591 only	-5 to +2	
I_{OUT}	Output current		mA
	Each output	300	
	All outputs	1000	
P_D	Power dissipation[1]	1	W
	Temperature range		°C
T_A	Ambient	0 to +70	
T_J	Junction	150	
T_{STG}	Storage	-65 to +150	
T_{sold}	Lead soldering temperature (10sec max)	300	°C

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 4.75$ to 5.25V, $0°C \leq T_A \leq 70°C$ unless otherwise specified.[2,3]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IH}	High		2.0			
V_{IL}	Low				0.8	
	Output voltage					V
V_{OL}	Low (NE590 only)	$I_{OL} = 250mA$, $T_A = 25°C$		1.0	1.3	
		Over temperature			1.5	
V_{OH}	High (NE591 only)	$I_{OH} = -250mA$, $V_{CC} = V_S = 5V$	2.9			
	Input current					µA
I_{IH}	High	$V_{in} = V_{CC}$		0.1	10	
I_{IL}	Low	$V_{in} = 0V$				
	$\overline{CE}$ input			-25	-60	
	All other inputs			-15	-50	
	Supply current[4]	$V_S = V_{CC} = 5V$				mA
I_{CCL}	All outputs low					
	NE590			33	50	
	NE591			15	50	
I_{CCH}	All outputs high					
	NE590			15	50	
	NE591			30	50	

NOTES

1. Derate power dissipation as indicated above threshold ambient temperature:
   NE590N at 95°C/W above 55°C
   NE590F at 100°C/W above 50°C
   NE591N at 90°C/W above 60°C
   NE591F at 93°C/W above 57°C
2. All typical values are at $V_{CC} = 5V$ and $T_A = 25°C$.
3. For the NE591, $V_S = V_{CC}$ in all tests.
4. Supply current for the NE591 is measured with no output load.

SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

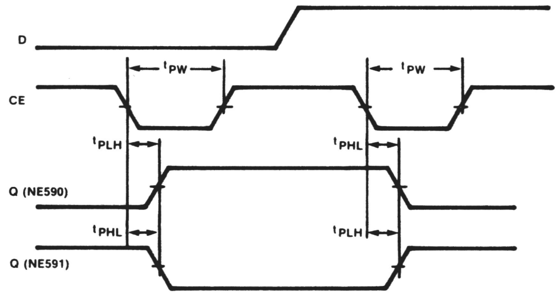
PARAMETER	TO	FROM	NE590			NE591			UNIT
			Min	Typ	Max	Min	Typ	Max	
Propagation delay time									ns
t_{PLH} Low to high[5]	Output	$\overline{CE}$		100			70		
t_{PHL} High to low[5]				130			80		
t_{PLH} Low to high[6]	Output	Data		80			60		
t_{PHL} High to low[6]				100			70		
t_{PLH} Low to high[7]	Output	Address		125			70		
t_{PHL} High to low[7]				115			70		
t_{PLH} Low to high[8]	Output	$\overline{CLR}$		80					
t_{PHL} High to low[8]							60		
t_{PLH} Low to high[5]	Output	$\overline{CS}$					70		
t_{PHL} High to low[5]							80		
SWITCHING SET-UP REQUIREMENTS									
$t_{s(H)}$[9]	Chip enable	High data		120			50		ns
$t_{s(L)}$[9]	Chip enable	Low data		120			70		ns
$t_{s(A)}$[10]	Chip enable	Address		-60			-10		ns
$t_{h(H)}$[9]	Chip enable	High data		-60			-60		ns
$t_{h(L)}$[9]	Chip enable	Low data		-60			-20		ns
$t_{s(CS)}$[9]	Chip enable	Low chip select					70		ns
$t_{pw(E)}$ Chip enable pulse width[5]				150			80		ns

NOTES

5. See Turn-On and Turn-Off Delays, Enable to Output and Enable Pulse Width timing diagram.
6. See Turn-On and Turn-Off Delays, Data to Output timing diagram.
7. See Turn-On and Turn-Off Delays, Address to Output timing diagram.
8. See Turn-Off Delay, Clear to Output timing diagram.
9. See Setup and Hold Time, Data to Enable timing diagram.
10. See Setup Time, Address to Enable timing diagram.

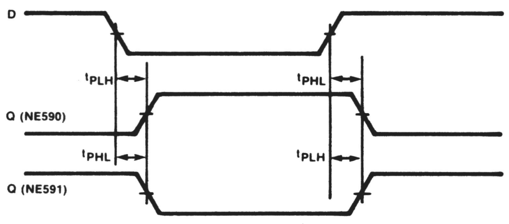
TIMING DIAGRAMS

TURN-ON AND TURN-OFF DELAYS, ENABLE TO OUTPUT AND ENABLE PULSE WIDTH



Other Inputs: $\overline{CLR}$ = H, A = Stable, $\overline{CS}$ = L

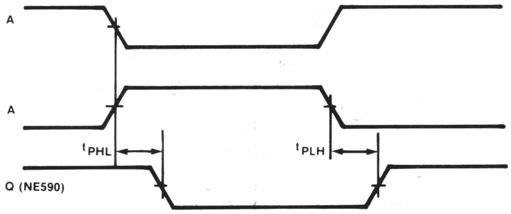
TURN-ON AND TURN-OFF DELAYS, DATA TO OUTPUT



Other Inputs: $\overline{CE}$ = $\overline{CS}$ = L, $\overline{CLR}$ = H, A = Stable

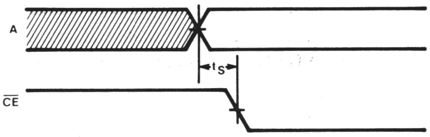
TIMING DIAGRAMS (Cont'd)

TURN-ON AND TURN-OFF DELAYS, ADDRESS TO OUTPUT


A
A
t_{PHL}
t_{PLH}
Q (NE590)

Other Inputs: $\overline{CE}$ = L, $\overline{CLR}$ = L, D = H

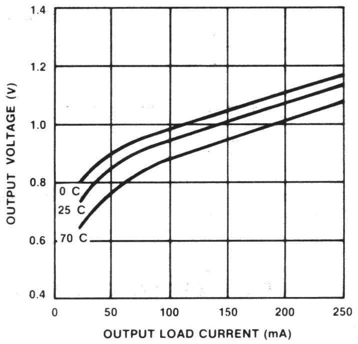
SETUP TIME, ADDRESS TO ENABLE


A
t_S
$\overline{CE}$

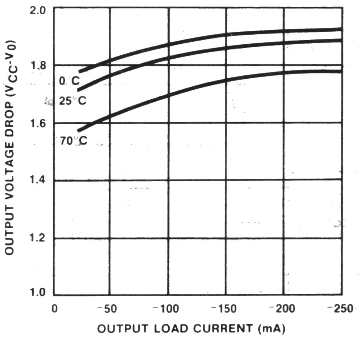
Other Inputs: $\overline{CLR}$ = H, $\overline{CS}$ = L

TYPICAL PERFORMANCE CHARACTERISTICS

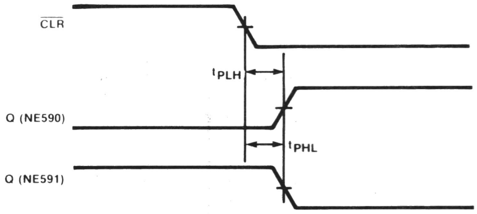
OUTPUT VOLTAGE VS LOAD CURRENT(NE590)



OUTPUT VOLTAGE DROP VS LOAD CURRENT(NE591)

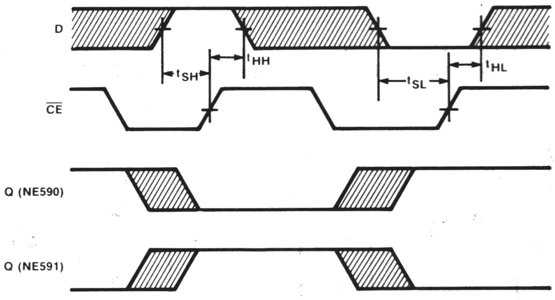


TURN-OFF DELAY, CLEAR TO OUTPUT


$\overline{CLR}$
t_{PLH}
Q (NE590)
t_{PHL}
Q (NE591)

Other Inputs: $\overline{CE}$ = H, $\overline{CS}$ = H

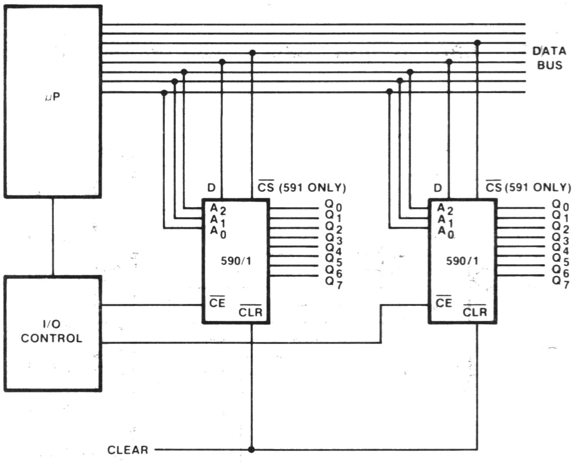
SETUP AND HOLD TIME, DATA TO ENABLE


D
t_{SH}
t_{HH}
t_{SL}
t_{HL}
$\overline{CE}$
Q (NE590)
Q (NE591)

Other Inputs: $\overline{CLR}$ = H, A = Stable, $\overline{CS}$ = L

TYPICAL APPLICATIONS

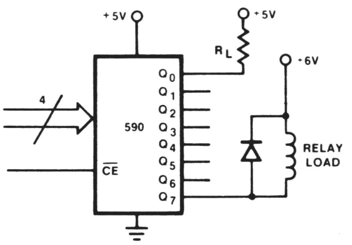
INTERFACING THE 590/591 WITH A MICROPROCESSOR SYSTEM


μP
DATA BUS
I/O CONTROL
D
$\overline{CS}$ (591 ONLY)
A_2
A_1
A_0
590/1
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
$\overline{CE}$
$\overline{CLR}$
D
$\overline{CS}$ (591 ONLY)
A_2
A_1
A_0
590/1
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
$\overline{CE}$
$\overline{CLR}$
CLEAR

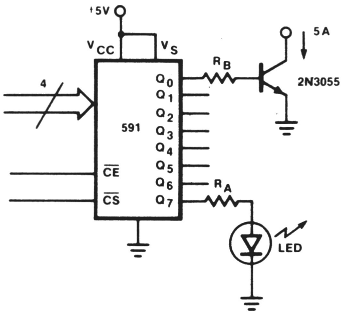
A_0, A_1, A_2, and $\overline{CS}$ may be connected to the address bus if permitted by system design.

TYPICAL APPLICATIONS (Cont'd)

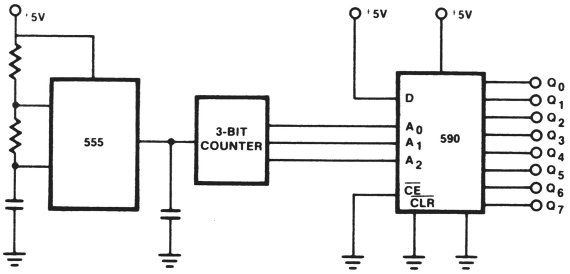
NE590 DRIVING SIMPLE LOADS


+5V
+5V
R_L
+6V
4
590
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
$\overline{CE}$
RELAY LOAD

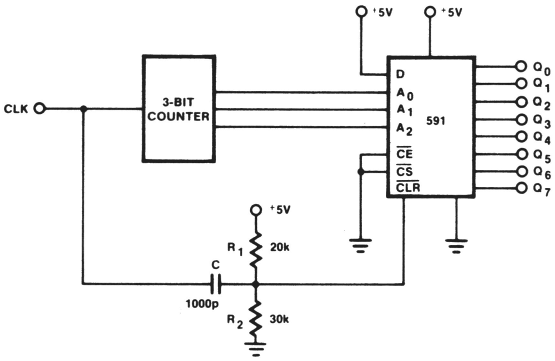
NE591 DRIVING SIMPLE LOADS


+5V
V_{CC}
V_S
R_B
5A
2N3055
4
591
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
$\overline{CE}$
$\overline{CS}$
R_A
LED

NE590 OPERATING IN DEMULTIPLEX MODE

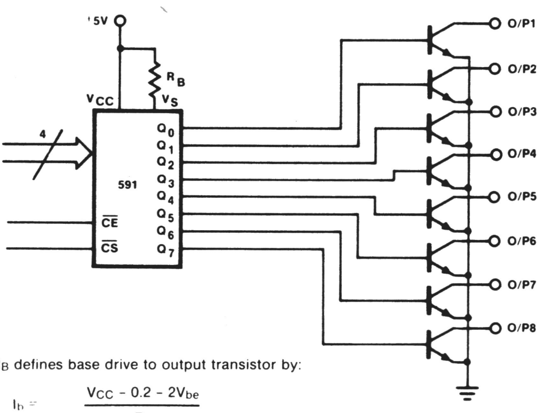

+5V
555
3-BIT COUNTER
+5V
+5V
D
A_0
A_1
A_2
590
$\overline{CE}$
$\overline{CLR}$
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7

NE591 OPERATING IN DEMULTIPLEX MODE


+5V
+5V
CLK
3-BIT COUNTER
D
A_0
A_1
A_2
591
$\overline{CE}$
$\overline{CS}$
$\overline{CLR}$
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
+5V
R_1
20k
C
1000p
R_2
30k

For display applications, interdigit blanking is provided by time constant $\tau = C(R_1/R_2)$. $\approx 10\mu s$ with values shown.

NE591 DRIVING HIGH CURRENT (5A) TRANSISTORS

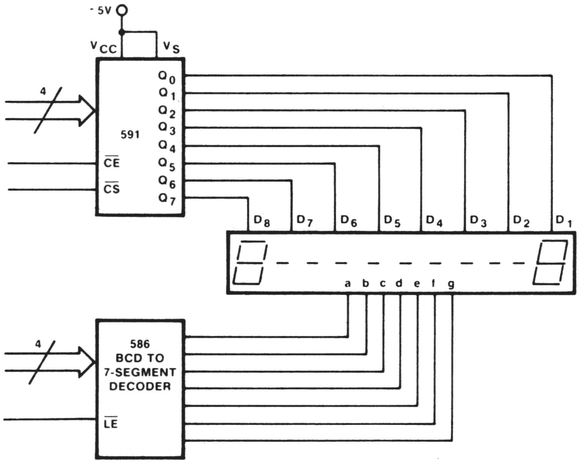

+5V
R_B
V_{CC}
V_S
4
591
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
$\overline{CE}$
$\overline{CS}$
O/P1
O/P2
O/P3
O/P4
O/P5
O/P6
O/P7
O/P8

R_B defines base drive to output transistor by:

$$I_b = \frac{V_{CC} - 0.2 - 2V_{be}}{R_b}$$

provided that only one output is ON at any time.

NE591 AS THE DIGIT DRIVER IN A LED DISPLAY SYSTEM


+5V
V_{CC}
V_S
4
591
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
$\overline{CE}$
$\overline{CS}$
D_8
D_7
D_6
D_5
D_4
D_3
D_2
D_1
a b c d e f g
4
586 BCD TO 7-SEGMENT DECODER
$\overline{LE}$

QUAD LINE DRIVER MC1488

MC1488-F,N

DESCRIPTION

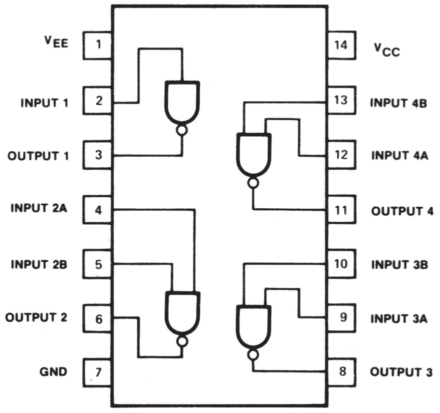
The MC1488 is a quad line driver which converts standard DTL/TTL input logic levels through one stage of inversion to output levels which meet EIA Standard No. RS-232C and CCITT Recommendation V.24.

FEATURES

- **Current limited output: ±10mA Typ**
- **Power-off source impedance: 300Ω Min**
- **Simple slew rate control with external capacitor**
- **Flexible operating supply range**
- **Inputs are DTL/TTL compatible**

PIN CONFIGURATION

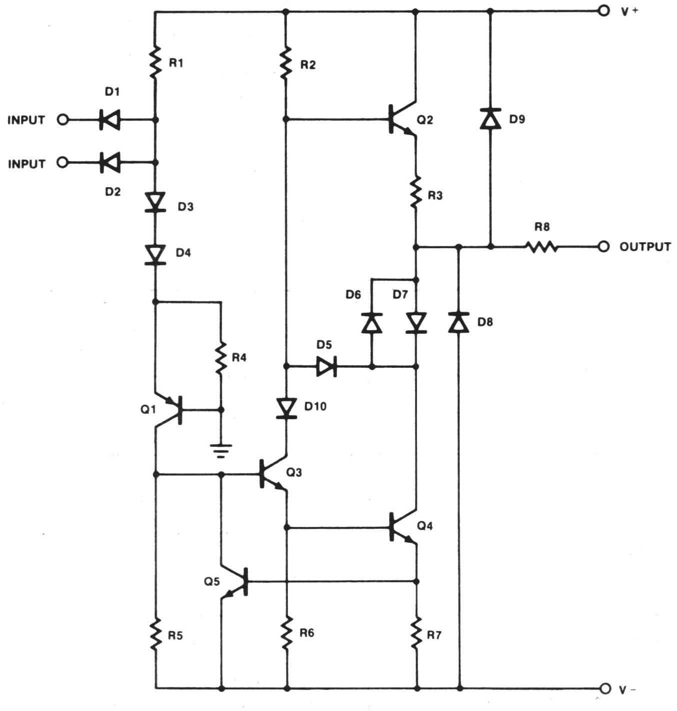
F,N PACKAGE



V_{EE}
1
INPUT 1
2
OUTPUT 1
3
INPUT 2A
4
INPUT 2B
5
OUTPUT 2
6
GND
7
14
V_{CC}
13
INPUT 4B
12
INPUT 4A
11
OUTPUT 4
10
INPUT 3B
9
INPUT 3A
8
OUTPUT 3

ORDER PART NO.
MC1488N/F

CIRCUIT SCHEMATIC



V+
R1
R2
D1
INPUT
INPUT
D2
Q2
D9
D3
R3
D4
R8
OUTPUT
D6
D7
D8
D5
R4
Q1
D10
Q3
Q4
Q5
R5
R6
R7
V−

1/4 CIRCUIT

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage V+	+15	V
V-	-15	V
Input voltage (V_{IN})	$-15 \leq V_{IN} \leq 7.0$	V
Output voltage	±15	V
Power dissipation:		
F package	1000	mW
N package	800	mW
Operating temperature range	0 to +75	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 10sec)	300	°C

DC ELECTRICAL CHARACTERISTICS

$V+ = +9.0V \pm 1\%$, $V- = -9.0V \pm 1\%$, $T_A = 0°C$ to $+75°C$ unless otherwise specified.
All typicals are for $V+ = 9.0V$, $V- = -9.0V$, and $T_A = 25°C$.*

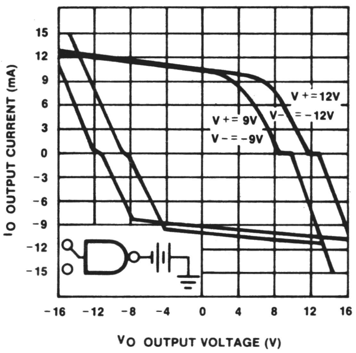
PARAMETER	TEST CONDITIONS		LIMITS			UNIT
			Min	Typ	Max	
Logic "0" input current	$V_{IN} = 0V$			-1.0	-1.6	mA
Logic "1" input current	$V_{IN} = +5.0V$			.005	10.0	µA
High level output voltage	$R_L = 3.0k\Omega$ $V_{IN} = 0.8V$	$V+ = 9.0V$ $V- = -9.0V$	6.0	7.0		V
		$V+ = 13.2V$ $V- = -13.2V$	9.0	10.5		V
Low level output voltage	$R_L = 3.0k\Omega$ $V_{IN} = 1.9V$	$V+ = 9.0V$ $V- = -9.0V$	-6.0	-6.8		V
		$V+ = 13.2V$ $V- = -13.2V$	-9.0	-10.5		V
High level output Short-circuit current	$V_{OUT} = 0V$ $V_{IN} = 0.8V$		-6.0	-10.0	-12.0	mA
Low level output Short-circuit current	$V_{OUT} = 0V$ $V_{IN} = 1.9V$		6.0	10.0	12.0	mA
Output resistance	$V+ = V- = 0V$ $V_{OUT} = \pm 2V$		300			Ω
Positive supply current (output open)	$V_{IN} = 1.9V$	$V+ = 9.0V$, $V- = -9.0V$		15.0	20.0	mA
		$V+ = 12V$, $V- = -12V$		19.0	25.0	mA
		$V+ = 15V$, $V- = -15V$		25.0	34.0	mA
	$V_{IN} = 0.8V$	$V+ = 9.0V$, $V- = -9.0V$		4.5	6.0	mA
		$V+ = 12V$, $V- = -12V$		5.5	7.0	mA
		$V+ = 15V$, $V- = -15V$		8.0	12.0	mA
Negative supply current (output open)	$V_{IN} = 1.9V$	$V+ = 9.0V$, $V- = -9.0V$		-13.0	-17.0	mA
		$V+ = 12V$, $V- = -12V$		-18.0	-23.0	mA
		$V+ = 15V$, $V- = -15V$		-25.0	-34.0	mA
	$V_{IN} = 0.8V$	$V+ = 9.0V$, $V- = -9.0V$		-1	-15	µA
		$V+ = 12V$, $V- = -12V$		-1	-15	µA
		$V+ = 15V$, $V- = -15V$		-.01	-2.5	mA
Power dissipation	$V+ = 9.0V$, $V- = -9.0V$			252	333	mW
	$V+ = 12V$, $V- = -12V$			444	576	mW
Propagation delay to "1" (t_{pd1})	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			275	350	ns
Propagation delay to "0" (t_{pd0})	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			70	175	ns
Rise time (t_r)	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			75	100	ns
Fall time (t_f)	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			40	75	ns

NOTE

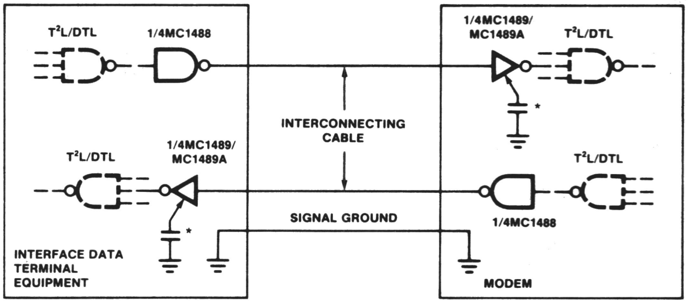
*Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.

TYPICAL PERFORMANCE CHARACTERISTICS

OUTPUT VOLTAGE AND CURRENT-LIMITING CHARACTERISTICS



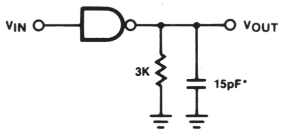
RS232C DATA TRANSMISSION


T²L/DTL
1/4MC1488
T²L/DTL
1/4MC1489/
MC1489A
INTERFACE DATA
TERMINAL
EQUIPMENT
INTERCONNECTING
CABLE
SIGNAL GROUND
1/4MC1489/
MC1489A
T²L/DTL
T²L/DTL
1/4MC1488
MODEM
*
*

NOTE

*Optional for noise filtering

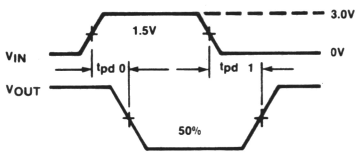
AC LOAD CIRCUIT


VIN
VOUT
3K
15pF*

NOTE

*C_L includes probe and jig capacitance.

SWITCHING WAVEFORMS


3.0V
1.5V
0V
VIN
tpd 0
tpd 1
VOUT
50%

NOTE

t_r and t_f are measured between 10% and 90% of the output waveform

APPLICATIONS

By connecting a capacitor to each driver output the slew rate can be controlled utilizing the output current limiting characteristics of the MC1488. For a set slew rate the appropriate capacitor value may be calculated using the following relationship

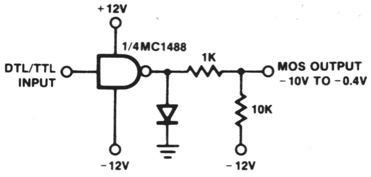
$$C = I_{SC}\,(\Delta T/\Delta V)$$

where C is the required capacitor, I_{SC} is the short circuit current value, and $\Delta V/\Delta T$ is the slew rate.

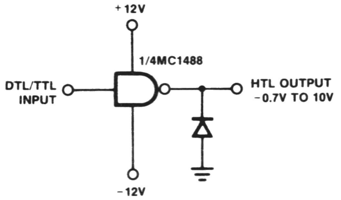
RS232C specifies that the output slew rate must not exceed 30V per microsecond. Using the worst case output short circuit current of 12mA in the above equation, calculations result in a required capacitor of 400pF connected to each output.

TYPICAL APPLICATIONS

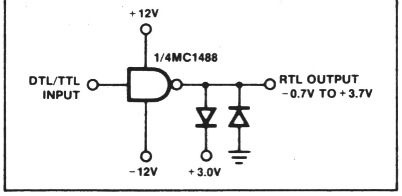
DTL/TTL-TO-MOS TRANSLATOR


+12V
1/4MC1488
1K
DTL/TTL
INPUT
MOS OUTPUT
−10V TO −0.4V
10K
−12V
−12V

DTL/TTL-TO-HTL TRANSLATOR


+12V
1/4MC1488
DTL/TTL
INPUT
HTL OUTPUT
−0.7V TO 10V
−12V

DTL/TTL-TO-RTL TRANSLATOR


+12V
1/4MC1488
DTL/TTL
INPUT
RTL OUTPUT
−0.7V TO +3.7V
−12V
+3.0V

QUAD LINE RECEIVERS MC1489/MC1489A

MC1489/1489-N/F

DESCRIPTION

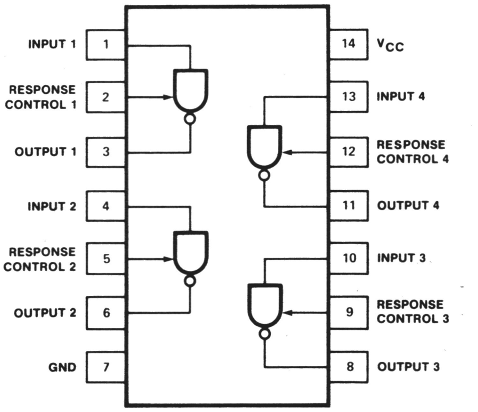
The MC1489/MC1489A are quad line receivers designed to interface data terminal equipment with data communications equipment. They are constructed on a single monolithic silicon chip. These devices satisfy the specifications of EIA standard No. RS232C.

FEATURES

- **Four totally separate receivers per package**
- **Programmable threshold**
- **Built-in input threshold hysteresis**
- **"Fail safe" operating mode**
- **Inputs withstand ±30V**

PIN CONFIGURATION

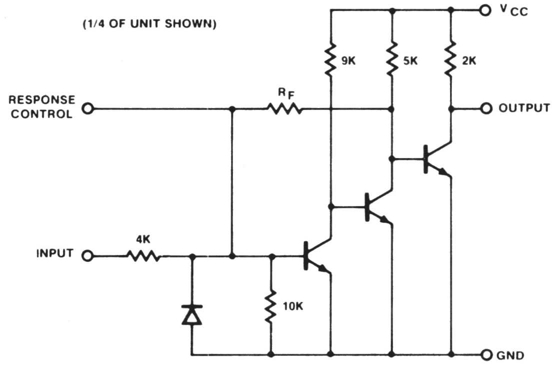
F,N PACKAGE



INPUT 1
1
RESPONSE CONTROL 1
2
OUTPUT 1
3
INPUT 2
4
RESPONSE CONTROL 2
5
OUTPUT 2
6
GND
7
14
V_{CC}
13
INPUT 4
12
RESPONSE CONTROL 4
11
OUTPUT 4
10
INPUT 3
9
RESPONSE CONTROL 3
8
OUTPUT 3

ORDER PART NO.
MC1489F/MC1489AF/MC1489N/MC1489AN

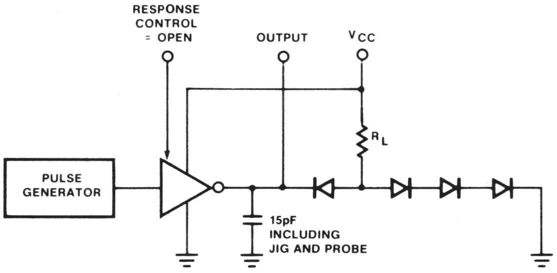
EQUIVALENT SCHEMATIC



(1/4 OF UNIT SHOWN)
V_{CC}
9K
5K
2K
RESPONSE CONTROL
R_F
OUTPUT
INPUT
4K
10K
GND

MC1489: R_F = 10k
MC1489A: R_F = 2k

AC TEST CIRCUIT

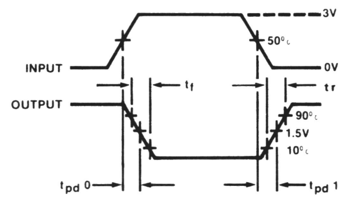


RESPONSE CONTROL = OPEN
OUTPUT
V_{CC}
R_L
PULSE GENERATOR
15pF INCLUDING JIG AND PROBE

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Power supply voltage	10	V
Input voltage range	±30	V
Output load current	20	mA
Power dissipation:		
F package	1	W
N package	800	mW
Operating temperature range	0 to +75	°C
Storage temperature range	-65 to +150	°C

VOLTAGE WAVEFORMS



3V
50%
INPUT
0V
t_f
t_r
OUTPUT
90%
1.5V
10%
t_{pd} 0
t_{pd} 1

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ± 1%, 0°C ≤ T_A ≤ +75°C unless otherwise specified.[1,2]

PARAMETER	TEST CONDITIONS	MC1489			MC1489A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input high threshold voltage	T_A = 25°C, V_{OUT} ≤ 0.45V, I_{OUT} = 10mA	1.0		1.5	1.75		2.25	V
Input low threshold voltage	T_A = 25°C, V_{OUT} ≤ 2.5V, I_{OUT} = -0.5mA	0.75		1.25	0.75		1.25	V
	V_{IN} = +25V V_{IN} = -25V	+3.6 -3.6	+5.6 -5.6	+8.3 -8.3	+3.6 -3.6	+5.6 -5.6	+8.3 -8.3	mA
Input current	V_{IN} = +3V V_{IN} = -3V	+0.43 -0.43	+0.53 -0.53		+0.43 -0.43	+0.53 -0.53		mA
Output high voltage	V_{IN} = 0.75V, I_{OUT} = -0.5mA	2.6	3.8	5.0	2.6	3.8	5.0	V
	Input = Open, I_{OUT} = -0.5mA	2.6	3.8	5.0	2.6	3.8	5.0	V
Output low voltage	V_{IN} = 3.0V, I_{OUT} = 10mA		0.33	0.45		0.33	0.45	V
Output short circuit current	V_{IN} = 0.75V		3.0			3.0		mA
Supply current	V_{IN} = 5.0V		20	26		20	26	mA
Power dissipation	V_{IN} = 5.0V		100	130		100	130	mW

NOTES
1. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
2. These specifications apply for response control pin = open.

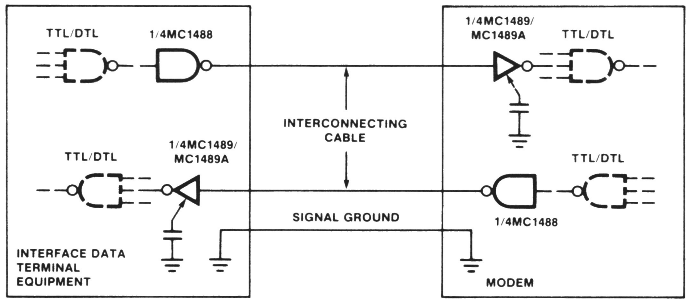
AC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ± 1%, T_A = 25°C unless otherwise specified.[1,2]

PARAMETER	TEST CONDITIONS	MC1489			MC1489A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input to output "high" Propagation delay (t_{pd1})	R_L = 3.9kΩ (AC test circuit)		25	85		25	85	ns
Input to output "low" Propagation delay (t_{pd0})	R_L = 390Ω (AC test circuit)		20	50		20	50	ns
Output rise time	R_L = 3.9kΩ (AC test circuit)		110	175		110	175	ns
Output fall time	R_L = 390Ω (AC test circuit)		9	20		9	20	ns

NOTES
1. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
2. These specifications apply for response control pin = open.

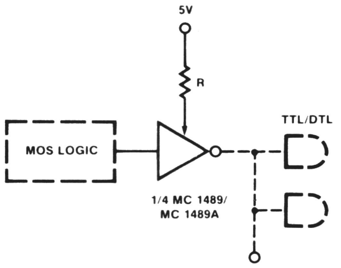
TYPICAL APPLICATIONS

RS232C DATA TRANSMISSION


TTL/DTL
1/4MC1488
1/4MC1489/
MC1489A
TTL/DTL
TTL/DTL
1/4MC1489/
MC1489A
INTERCONNECTING
CABLE
TTL/DTL
SIGNAL GROUND
1/4MC1488
INTERFACE DATA
TERMINAL
EQUIPMENT
MODEM

*Optional for noise filtering

MOS TO TTL/DTL TRANSLATOR


5V
R
MOS LOGIC
TTL/DTL
1/4 MC 1489/
MC 1489A

SECTION 7

TRANSISTOR ARRAYS

Section 7—TRANSISTOR ARRAYS

ULN2003 High Voltage/High Current Darlington Transistor Array 175
ULN2004 High Voltage/High Current Darlington Transistor Array 175
CA3081 Seven Transistor Array 179
CA3082 Seven Transistor Array 179

NOTE

*Any product listed in this section but not incorporated within the text may be obtained by writing Information Services at Signetics, 811 E. Arques, M/S 027, Sunnyvale, California 94086, or by calling (408) 746-1682.

HIGH VOLTAGE/HIGH CURRENT DARLINGTON TRANSISTOR ARRAYS — ULN2003/2004

ULN2003/2004-N

DESCRIPTION

These high-voltage, high-current Darlington transistor arrays are comprised of seven silicon NPN Darlington pairs on a common monolithic substrate. All units feature open collector outputs and integral suppression diodes for inductive loads. Peak inrush currents to 600mA are allowable, making them ideal for driving tungsten filament lamps also.

The Type ULN-2003 has a series base resistor to each Darlington pair, and thus allows operation directly with TTL or CMOS operating at a supply voltage of 5V.

The Type ULN-2004 has an appropriate series input resistor to allow its operation directly from CMOS or PMOS outputs utilizing supply voltages of 6 to 15V. The required input current is below that of the Type ULN-2003 while the required input voltage is less than that required by the Type ULN-2002.

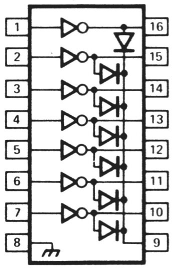
In all cases, the individual Darlington pair collector current rating is 500mA. However, outputs may be paralleled for higher load current capability. All devices are supplied in a 16-pin dual in-line plastic package.

FEATURES

- **Peak inrush current 600mA**
- **Protected internally against inductive loads**
- **Open collector topology**
- **Compatible with most logic technologies**

PIN CONFIGURATION

N PACKAGE

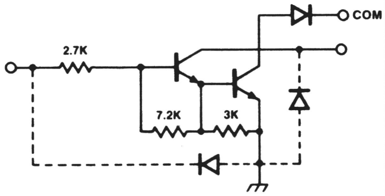


ORDER PART NO.

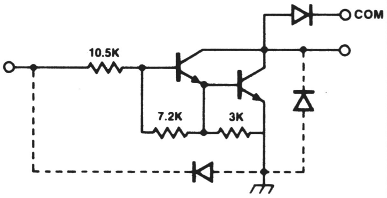
ULN2003N
ULN2004N

EQUIVALENT SCHEMATICS

TYPE ULN2003 (each driver)



TYPE ULN2004 (each driver)



ABSOLUTE MAXIMUM RATINGS

at 25°C Free-Air temperature for any one Darlington pair unless otherwise specified.

	PARAMETER	RATING	UNIT
V_{CE}	Output voltage	50	V
V_{IN}	Input voltage	30	V
V_{EBO}	Emitter base voltage	6	V
I_C	Continuous collector current	500	mA
I_B	Continuous base current	25	mA
P_D	Power dissipation	1.3	W
	Derating factor above 25°C	95	°C/W
T_A	Ambient temperature range (operating)	0 to +85	°C
T_S	Storage temperature range	-65 to +150	°C

*NOTE

Under normal operating conditions, these units will sustain 350mA per output with $V_{CE(SAT)} = 1.6V$ at 70°C with a pulse width of 20 ms and a duty cycle of 30%.

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$ unless otherwise specified.[1,2,3]

PARAMETER		TEST CONDITIONS	Test Fig.	LIMITS			UNIT
				Min	Typ	Max	
I_{CEX}	Output leakage current	$V_{CE} = 50V$, $T_A = 70°C$	1A	—	—	100	μA
	Type ULN-2004	$V_{CE} = 50V$, $T_A = 70°C$, $V_{IN} = 1V$	1B	—	—	500	μA
$V_{CE(SAT)}$	Collector-emitter Saturation voltage	$I_C = 350mA$, $I_B = 500\mu A$	2	—	1.25	1.6	V
		$I_C = 200mA$, $I_B = 350\mu A$	2	—	1.1	1.3	V
		$I_C = 100mA$, $I_B = 250\mu A$	2	—	0.9	1.1	V
$I_{IN(ON)}$	Input current						
	Type ULN-2003	$V_{IN} = 3.85V$	3	—	0.93	1.35	mA
	Type ULN-2004	$V_{IN} = 5V$	3	—	0.35	0.5	mA
		$V_{IN} = 12V$	3	—	1.0	1.45	mA
$I_{IN(OFF)}$	Input current	$I_C = 500\mu A$, $T_A = 70°C$	4	50	65	—	μA
$V_{IN(ON)}$	Input voltage						
	Type ULN-2003	$V_{CE} = 2V$, $I_C = 200mA$	5	—	—	2.4	V
		$V_{CE} = 2V$, $I_C = 250mA$	5	—	—	2.7	V
		$V_{CE} = 2V$, $I_C = 300mA$	5	—	—	3.0	V
	Type ULN-2004	$V_{CE} = 2V$, $I_C = 125mA$	5	—	—	5.0	V
		$V_{CE} = 2V$, $I_C = 200mA$	5	—	—	6.0	V
		$V_{CE} = 2V$, $I_C = 275mA$	5	—	—	7.0	V
		$V_{CE} = 2V$, $I_C = 350mA$	5	—	—	8.0	V
C_{IN}	Input capacitance		—	—	15	30	pF
I_R	Clamp diode leakage current	$V_R = 50V$	6	—	—	50	μA
V_F	Clamp diode forward voltage	$I_F = 350mA$	7	—	1.7	2	V

NOTES

1. All limits stated apply to the complete Darlington series except as specified for a single device type.
2. The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
3. The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$ unless otherwise specified.[1,2,3]

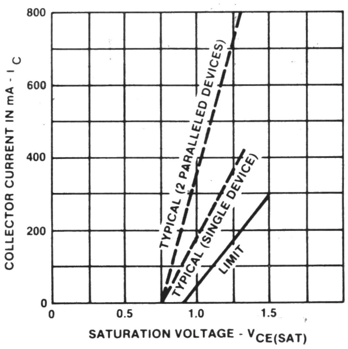
PARAMETER		TEST CONDITIONS	Test Fig.	LIMITS			UNIT
				Min	Typ	Max	
t_{PLH}	Turn-on delay	0.5 E_{IN} to 0.5 E_{OUT}	—	—	1.0	5	μs
t_{PHL}	Turn-off delay	0.5 E_{IN} to 0.5 E_{OUT}	—	—	1.0	5	μs

NOTES

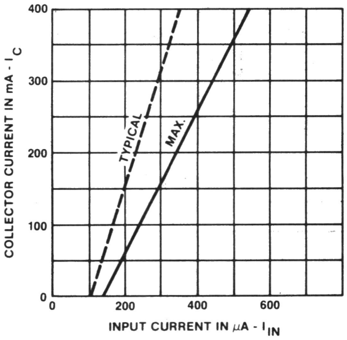
1. All limits stated apply to the complete Darlington series except as specified for a single device type.
2. The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
3. The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

TYPICAL PERFORMANCE CHARACTERISTICS

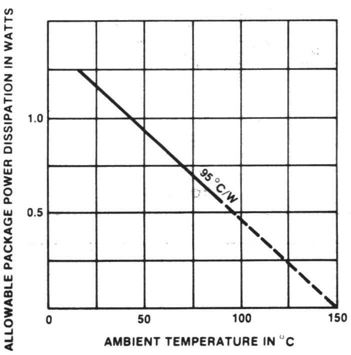
COLLECTOR CURRENT AS A FUNCTION OF SATURATION VOLTAGE



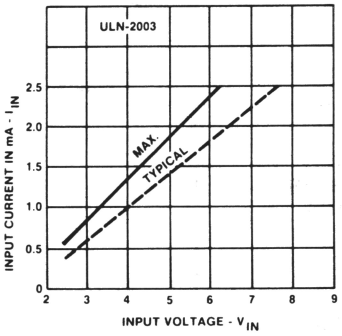
COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT



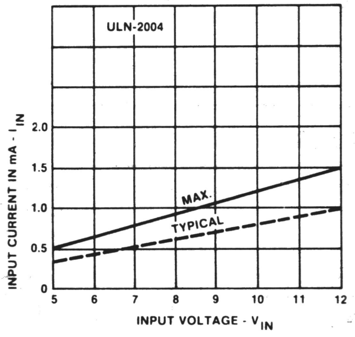
ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE FOR TYPE ULN-2003



INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE FOR TYPE ULN-2004



TEST FIGURES

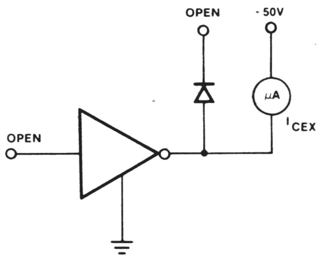

OPEN
- 50V
OPEN
μA
I_{CEX}

Figure 1A

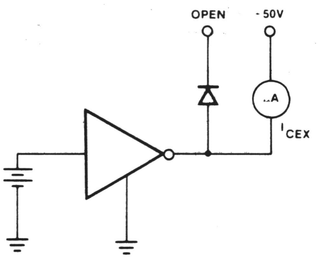

OPEN
- 50V
μA
I_{CEX}

Figure 1B

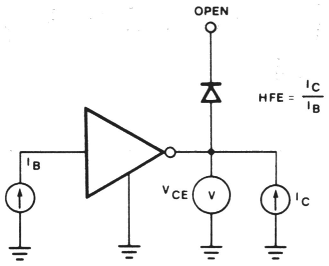

OPEN
$HFE = \frac{I_C}{I_B}$
I_B
V_{CE}
V
I_C

Figure 2

TEST FIGURES (Cont'd)

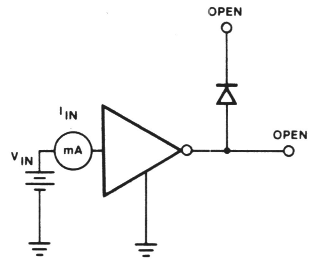

OPEN
I_{IN}
OPEN
V_{IN}
mA

Figure 3

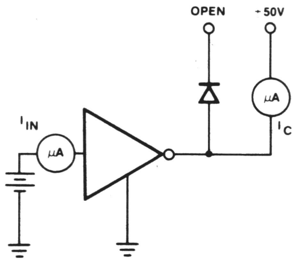

OPEN
+50V
I_{IN}
μA
μA
I_C

Figure 4

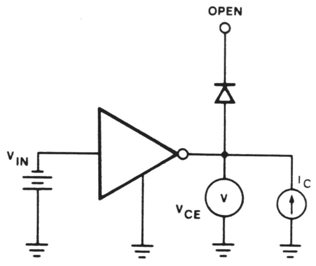

OPEN
V_{IN}
V_{CE}
V
I_C

Figure 5

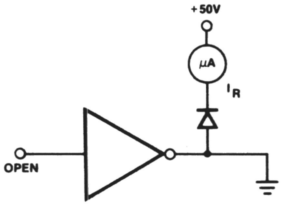

+50V
μA
I_R
OPEN

Figure 6

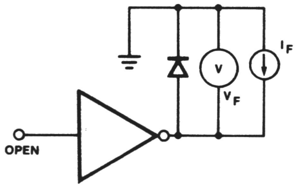
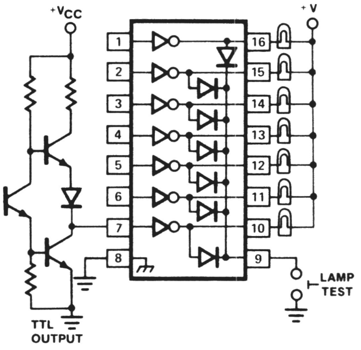


Figure 7

TYPICAL APPLICATIONS

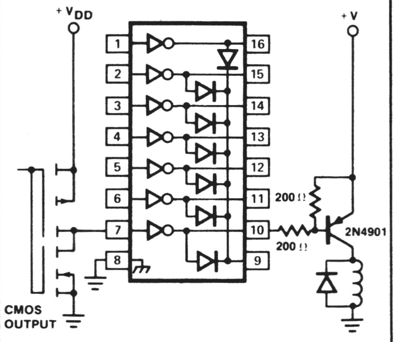
TTL TO LOAD

ULN2003


+VCC
+V
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
LAMP TEST
TTL OUTPUT

BUFFER FOR HIGHER CURRENT LOADS

ULN2004


+VDD
+V
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
200Ω
200Ω
2N4901
CMOS OUTPUT

SEVEN TRANSISTOR ARRAY CA3081/3082

CA3081/3082-N,F

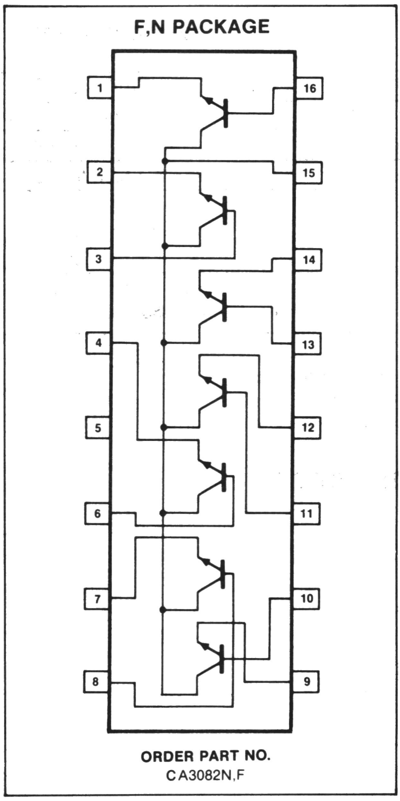
DESCRIPTION

The CA3081 and CA3082 are monolithic integrated circuits each consisting of seven separate npn transistors on a common substrate. The transistors are capable of driving loads up to 100mA. At the same time the transistor geometry used gives maximum current gain at quite low currents, making the devices also suitable for small signal applications. In the CA3081 the transistors are connected in common emitter configuration while in the CA3082 the collectors are common. The transistor arrays are particularly suitable for driving light-emitting diodes and seven-segment displays as well as for general purpose applications.

FEATURES

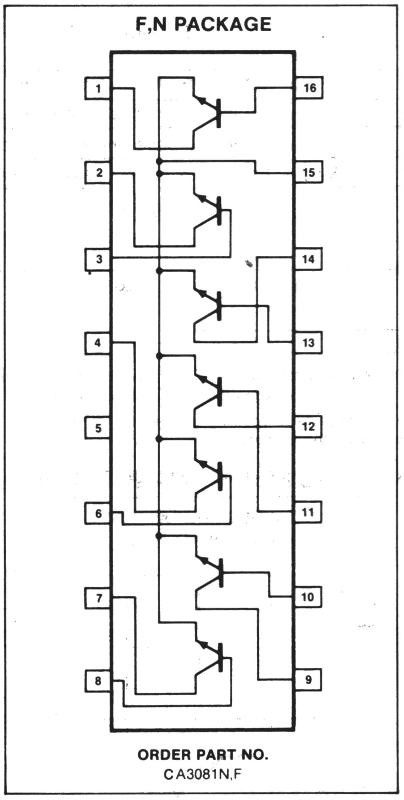
- V_{CBO}=50V
- V_{CEO}=35V
- **Collector current 100mA**
- **Common emitter or common collector configuration**

PIN CONFIGURATIONS



F,N PACKAGE

ORDER PART NO.
CA3082N,F



F,N PACKAGE

ORDER PART NO.
CA3081N,F

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CEO}	Collector-emitter voltage (open base)		V
V_{CBO}	Collector-base voltage (open emitter)	50	V
V_{CSO}	Collector-substrate voltage (open base and emitter)	50	V
V_{EBO}	Emitter-base voltage (open collector)	6	V
I_C	Collector current (dc)	100	mA
I_B	Base current (dc)	20	mA
P	Power dissipation: any one transistor	500	mW
P_{TOT}	total package (see derating curve)	750	mW
T_A	Operating ambient temperature	-40 to +125	°C
T_{stg}	Storage temperature	-50 to +125	°C
T_j	Junction temperature	125	°C
	Lead temperature (10sec)	300	°C

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

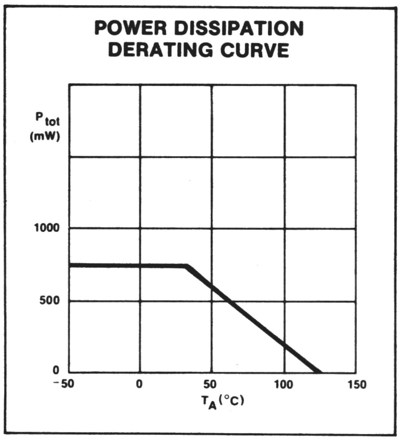
PARAMETER		TEST CONDITIONS	CA3081/3082			UNIT
			Min	Typ	Max	
V_{CEO}	Collector-emitter breakdown voltage	$I_C = 1mA$, $I_B = 0$	35			V
V_{CSO}	Collector-substrate breakdown voltage	$I_C = 1mA$, $I_B = 0$, $I_E = 0$	50			V
V_{CBO}	Collector-base breakdown voltage	$I_C = 10\mu A$, $I_E = 0$	50			V
V_{EBO}	Emitter-base breakdown voltage	$I_E = 10\mu A$, $I_C = 0$	5.5	7.0		V
hfe	DC current gain	$I_E = 10\mu A$, $V_{CE} = 5V$ $I_E = 1mA$, $V_{CE} = 5V$ $I_E = 20mA$, $V_{CE} = 5V$	50 50 30			
V_{SAT}	Saturation voltage	$I_C = 5mA$, $I_B = .5mA$ $I_C = 50mA$, $I_B = 5mA$		0.2 0.4	0.4 0.8	V V

NOTE

As each collector forms a parasitic diode with the substrate, the substrate has to be connected to a voltage which is lower than the lowest collector voltage.

To avoid parasitic coupling between the transistors, the substrate (pin 5) should be connected to signal ground.

TYPICAL PERFORMANCE CHARACTERISTICS



SECTION 8
PHILIPS INDUSTRIAL

Section 8—PHILIPS INDUSTRIAL

SAA1027 Stepper Motor Driver Circuit 185

NOTE

*Any product listed in this section but not incorporated within the text may be obtained by writing Information Services at Signetics, 811 E. Arques, M/S 027, Sunnyvale, California 94086, or by calling (408) 746-1682.

STEPPER MOTOR DRIVER CIRCUIT SAA1027

SAA1027-N

DESCRIPTION

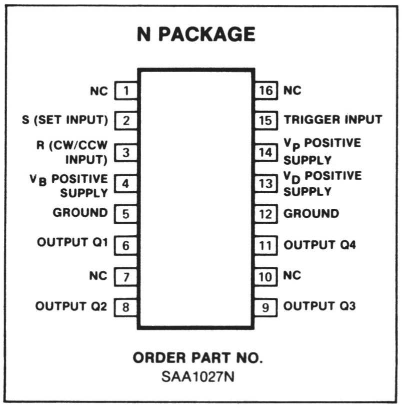
The SAA1027 is intended for driving a four phase two stator stepper motor. The circuit consists of four output stages, a logic part and three input stages. The logic part is driven by three input stages; a trigger input stage, an input stage which can change the switching sequence of the logic part so that the motor can rotate clock wise (CW) or counter clock wise (CCW) and a set input stage to set the four output stages. The three inputs are compatible with high noise immunity logic to ensure proper operation, even in noisy environments. The output can deliver 350mA in each phase. The right switching sequence of the four phases is obtained from the logic part of the circuit. Integrated diodes protect the outputs against transient spikes.

FEATURES

- **CW or CCW rotation**
- **4-phase drive**
- **Few external components**

PIN CONFIGURATION

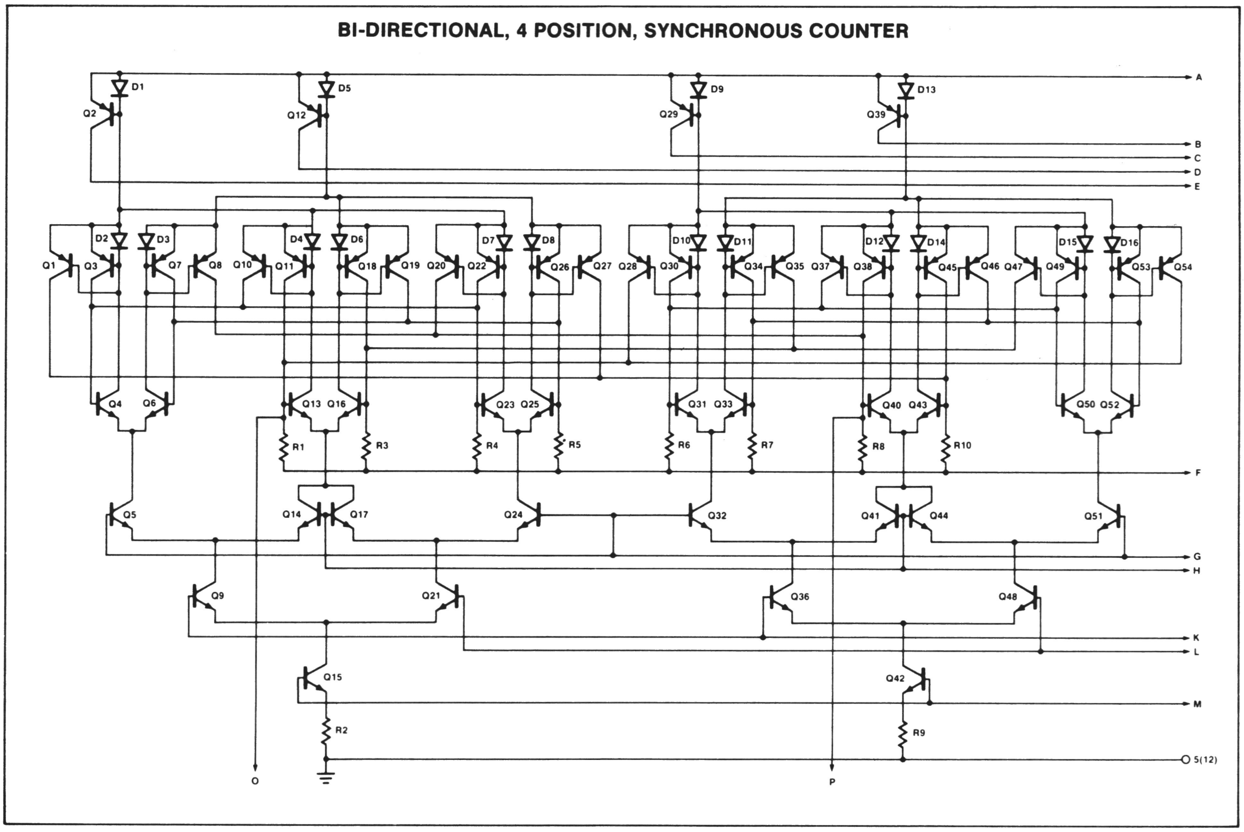
N PACKAGE


NC 1
S (SET INPUT) 2
R (CW/CCW INPUT) 3
V_B POSITIVE SUPPLY 4
GROUND 5
OUTPUT Q1 6
NC 7
OUTPUT Q2 8
16 NC
15 TRIGGER INPUT
14 V_P POSITIVE SUPPLY
13 V_D POSITIVE SUPPLY
12 GROUND
11 OUTPUT Q4
10 NC
9 OUTPUT Q3

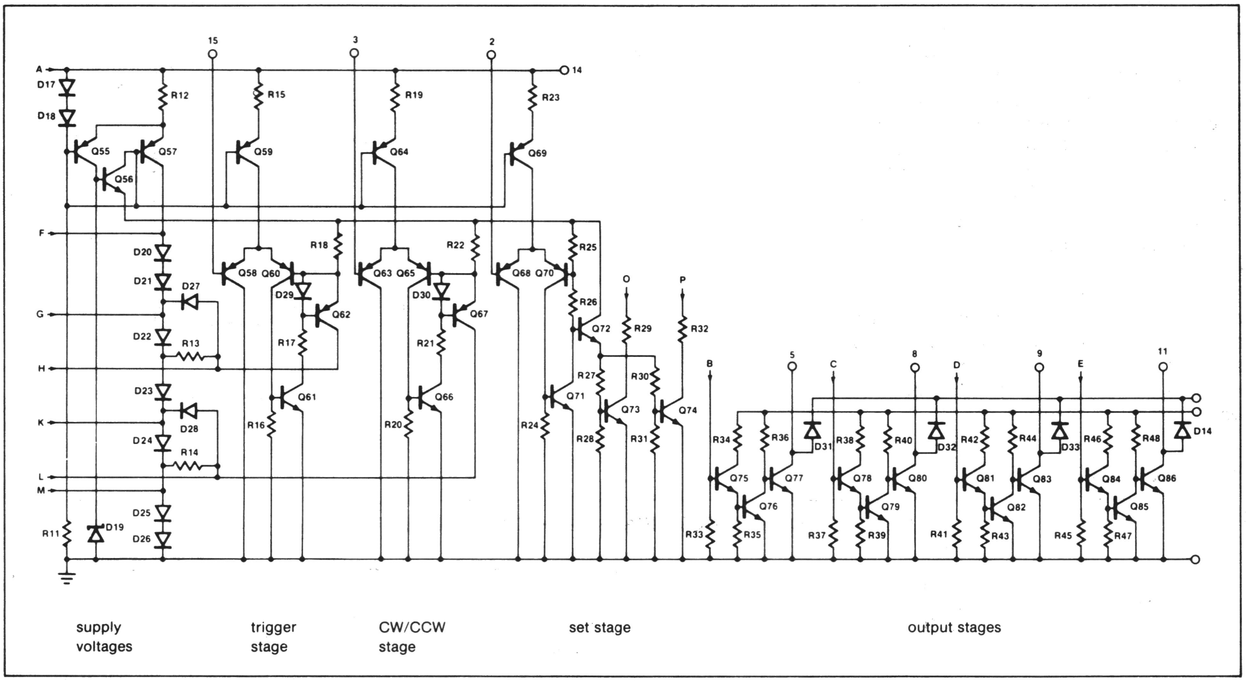
ORDER PART NO.
SAA1027N

EQUIVALENT SCHEMATIC

BI-DIRECTIONAL, 4 POSITION, SYNCHRONOUS COUNTER


A
B
C
D
E
F
G
H
K
L
M
O
P
5(12)
D1
D5
D9
D13
Q2
Q12
Q29
Q39
Q1
Q3
Q7
Q8
Q10
Q11
Q18
Q19
Q20
Q22
Q26
Q27
Q28
Q30
Q34
Q35
Q37
Q38
Q45
Q46
Q47
Q49
Q53
Q54
Q4
Q6
Q13
Q16
Q23
Q25
Q31
Q33
Q40
Q43
Q50
Q52
R1
R3
R4
R5
R6
R7
R8
R10
Q5
Q14
Q17
Q24
Q32
Q41
Q44
Q51
Q9
Q21
Q36
Q48
Q15
Q42
R2
R9

EQUIVALENT SCHEMATIC (Cont'd)


15
3
2
14
A
D17
D18
R12
R15
R19
R23
Q55
Q57
Q56
Q59
Q64
Q69
F
D20
D21
D27
R18
R22
R25
Q58 Q60
Q63 Q65
Q68 Q70
D29
D30
Q62
Q67
G
D22
R13
R17
R21
R26
Q72
O
P
R29
R32
H
D23
Q61
Q66
Q71
R27
R30
Q73
Q74
K
D28
R16
R20
R24
R28
R31
D24
R14
L
M
D25
D26
R11
D19
R33
B
5
C
8
D
9
E
11
R34
R36
D31
R38
R40
D32
R42
R44
D33
R46
R48
D14
Q75
Q77
Q78
Q80
Q81
Q83
Q84
Q86
Q76
Q79
Q82
Q85
R35
R37
R39
R41
R43
R45
R47
supply voltages
trigger stage
CW/CCW stage
set stage
output stages

ABSOLUTE MAXIMUM RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER		RATING	UNIT
	VOLTAGES		
V_P	Supply voltage (pin 4, 13, 14)	20	V
V_I	Input voltage; R (pin 3), S (pin 2), T (pin 15)	20	V
	CURRENT		
I_Q	Output current; Q_1 (pin 6), Q_2 (pin 8), Q_3	500	mA
	POWER DISSIPATION	See figure 1	
	TEMPERATURES		
T_{STG}	Storage temperature	-40 to +125	°C
T_A	Operating ambient temperature	-20 to +70	°C
	THERMAL RESISTANCE		
θ_{ja}	From junction to ambient	70	°C/W

*NOTE

Additional power caused by the self-inductance of the motor-coils will be dissipated in the diodes (D31 to D34).

TRUTH TABLE[1,2]

S = H									
R=H					R = L				
T	Q1	Q2	Q3	Q4	T	Q1	Q2	Q3	Q4
0	L	H	L	H	0	L	H	L	H
1	H	L	L	H	1	L	H	H	L
2	H	L	H	L	2	H	L	H	L
3	L	H	H	L	3	H	L	L	H
4	L	H	L	H	4	L	H	L	H

Trigger Conditions(T)

NOTES

1. Direction conditions (R)
   The direction of rotation can be changed at any moment independent of the state of the T and S inputs.
2. Set conditions (S)
   When T is HIGH and S LOW then the outputs are set: $Q_1 = L$, $Q_2 = H$, $Q_3 = L$, $Q_4 = H$.

DC ELECTRICAL CHARACTERISTICS

$-20°C \le T_A \le 65°$, $V_P = 12V$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SAA1027			UNIT
			Min	Typ	Max	
V_P	Supply voltage (pin 14)		9.5	12	18	V
I_P	Supply current	Pin 4 open, without loads, all inputs high	2.0	4.5	6.5	mA
V_{IH}		R, S, T inputs	7.5			V
I_{IH}		R, S, T inputs		1		μA
V_{IL}		R, S, T inputs			4.5	V
I_{IL}		R, S, T inputs		30		μA
V_Q	Supply voltage	Each output stage	1.5	12	18	V
I_Q	Supply current	Each output stage			350	mA
V_{SAT}	Saturation voltage				1	V
	Bias voltage and current	Reference Figure 2.				
	Bias resistor	Reference Figure 3.				
	Bias resistor power dissipation	Reference Figure 4.				
	Device power dissipation	Reference Figure 5.				

TYPICAL PERFORMANCE CHARACTERISTICS

POWER DISSIPATION DERATING CURVE

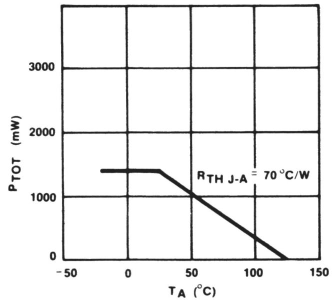


Figure 1

BIAS VOLTAGE AND CURRENT

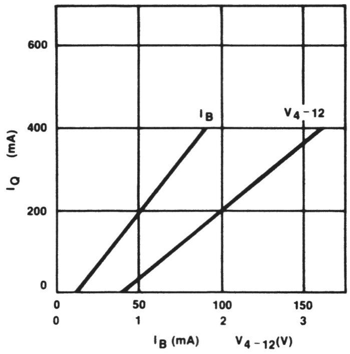


Figure 2

BIAS RESISTOR

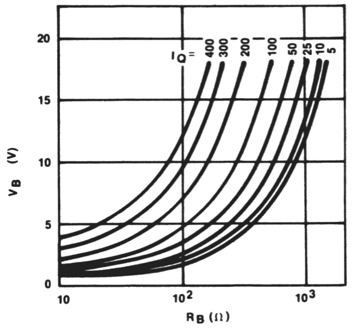


Figure 3

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

BIAS RESISTOR POWER DISSIPATION

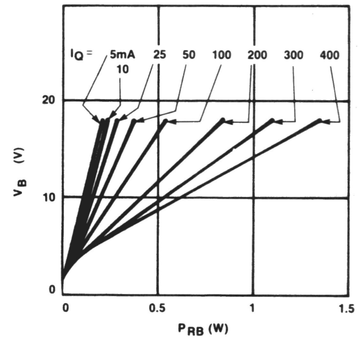


Figure 4

TOTAL DEVICE POWER DISSIPATION

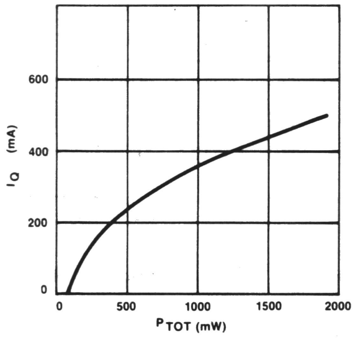


Figure 5

TYPICAL APPLICATIONS

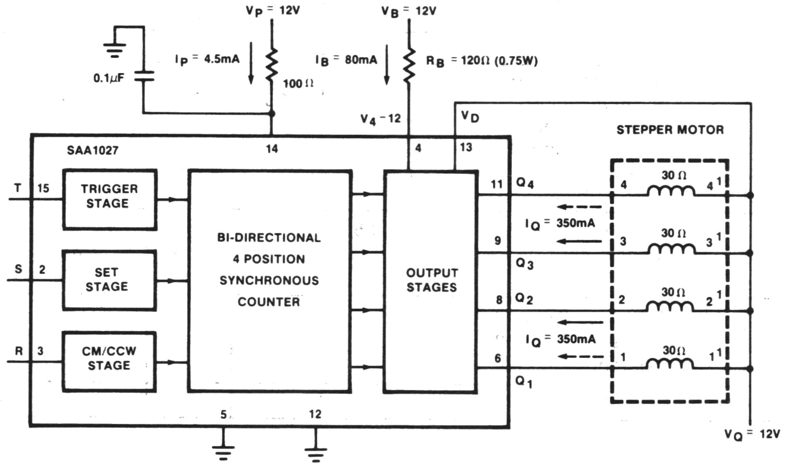

V_P = 12V
V_B = 12V
0.1μF
I_P = 4.5mA
100 Ω
I_B = 80mA
R_B = 120Ω (0.75W)
V_4 - 12
V_D
SAA1027
14
4
13
STEPPER MOTOR
T
15
TRIGGER STAGE
S
2
SET STAGE
R
3
CM/CCW STAGE
BI-DIRECTIONAL 4 POSITION SYNCHRONOUS COUNTER
OUTPUT STAGES
11
Q_4
9
Q_3
8
Q_2
6
Q_1
I_Q = 350mA
I_Q = 350mA
30 Ω
30 Ω
30 Ω
30 Ω
4
4
1
3
3
1
2
2
1
1
1
1
5
12
V_Q = 12V

Figure 6

SECTION 9
DISPLAY DRIVERS

signetics

Section 9—DISPLAY DRIVERS

NE586 LED Decoder/Driver 195
NE587 LED Decoder/Driver 195
SA594 Vacuum Fluorescent Display Driver 204
DS7880 High Voltage 7-Segment Decoder/Driver .... *
DS8880/8880-1 High Voltage 7-Segment Decoder/Driver .... *
NE582 Hex Universal Driver 208

NOTE

*Any product listed in this section but not incorporated within the text may be obtained by writing Information Services at Signetics, 811 E. Arques, M/S 027, Sunnyvale, California 94086, or by calling (408) 746-1682.

DISPLAY DRIVER DEFINITIONS

T_A

Ambient temperature range. Range of the surrounding environment of the operating device.

T_J

Junction Temperature. The maximum temperature of the device. 150°C is standard for silicon devices.

T_{STG}

Storage temperature range. Temperature range that the device can be stored in a non-operating condition.

T_{SOLD}

Soldering Temperature. The temperature which can be applied to the lead frame of the device for short periods of time (normally specified for a duration of 10 sec).

Truth Tables

0 is logic level low
1 is logic level high
X - don't care condition - has no effect under circuit conditions listed.

Absolute Maximum Rating

Operating safe zones exceeding these limits could cause permanent damage to the device and are not meant to imply that devices can operate at these limits.

Power Dissipation

The power that the device can safely handle at 25°C. The dissipation must be derated as indicated for the individual package type.

Package Type Designation

See full package designations in Appendix.

V_{CC} ($-V_{CC}$)

Supply Voltage. The range of power supply voltage over which the device will operate safely.

LED

Light Emitting Diode

$\overline{XX}$

Negate Bar-when it appears over a function indicates that the "true" or valid condition of that function is a logic low level.

i.e. LE - would require a logic high level to cause a latch enable.
$\overline{LE}$ - would require a logic low level to cause a latch enable.

I_{SEG}

Segment Current. The amount of current supplied to each segment in a display. Current ratios are generally compared to segment 'b'.

BCD

Binary Coded Decimal

$\overline{BI}$/RBO

Blanking Input or Ripple Blanking Output.

$\overline{RBI}$

Ripple Blanking Input. The maximum clock frequency: the maximum input frequency at a clock input for the predictable performance. Above this frequency the device may cease to function.

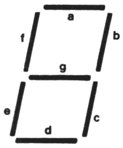
t_{PLH}

Propagation Delay Time. The time between the specified reference points on the input and output waveforms with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL}

Propagation Delay Times. The time between the specified reference points on the input and output waveforms with the output changing from the defined HIGH level to the defined LOW level.

Segment Identification



t_h

Hold Time. The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the current logic level may be released prior to the active transition of the timing pulse and still be recognized.

t_s

Setup Time. The interval immediately preceeding the active transition of the timing pulse (usually the clock pulse) or preceeding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_W

Pulse Width. The time between the specified reference points on the leading and trailing edges of a pulse.

t_{rec}

Recovery Time. The time between the reference point on the trailing edge of an asynchronous input control pulse and the reference point on the activating edge of a synchronous (clock) pulse input such that the device will respond to the synchronous input.

V_S

Source Voltage. A separate V_{CC} line depending on part type.

I_{OH}

Output Current Source the device can supply while maintaining a specified voltage output level.

Typical Value

The typical value of a particular parameter determined by characterization of the device or sampling. Usually indicates that the particular device is not 100% tested for the parameter because it does not vary or can be determined by design and other tested variables. Occasionally typical values are given rather than min-

DISPLAY DRIVER DEFINITIONS (Cont'd)

max values because 100% testing would raise the cost of the product to a prohibitive level. If a typical value must be guaranteed to ensure specific operation, custom testing can often be provided at an additional cost to the user.

I_S

Source Current. Current flowing into the V_S supply terminal of the device with specified operating conditions.

Duty Cycle

Ratio of time on to time off. Generally expressed in percentage.

V_F

Forward voltage drop of a device at a specified current level.

I_B

Input Bias Current Current into an analog circuit input, specified at a particular voltage level.

CLR

Clear. Clear command will preset all internal circuits to a predetermined state.

CE

Chip Enable.

V_{IH}

Input High Voltage. The range of input voltages recognized by the device as a logic high.

V_{IL}

Input Low Voltage. The range of input voltages recognized by the device as a logic low.

V_{OH}

Output High Voltage. The minimum guaranteed High voltage at an output terminal for the specified output current I_{OH} and at the minimum V_{CC} value.

V_{OL}

Output Low Voltage. The maximum guranteed low voltage at an output terminal sinking the specified load current I_{OL}.

V_{BR}

Output Breakdown Voltage. Maximum voltage applied to a disabled (off) output to ensure a leakage current less than the specified value.

V_{IN}

The range of voltage on any input which the device can safely handle or a specified input voltage to the device.

V_{OUT}

The range of voltage on any output which the device can safely handle or a specified output voltage to the device.

$I_{CC}(-I_{CC})$

Supply Current. The current flowing into the $+V_{CC}$ $(-V_{CC})$ supply terminal of the circuit with specified input conditions and open outputs. Input conditions are chosen to guarantee worst case operation unless specified.

I_{IH}

Input High Current. The Current flowing into or out of an input when a specified High level voltage is applied to that input.

I_{IL}

Input Low Current. The current flowing out of an input when a specified Low level voltage is applied to that input.

I_{OL}

Output Low Current. The current flowing into an output when a which is in the Low State.

I_{OS}

Output Short-Circuit Current. The current flowing out of an output which is in the High state when that output is short circuit to the ground.

I_{CEX}

Output Leakage Current. The current flowing out of or into a disabled (off) output with a specified High output voltage applied.

LED DECODER/DRIVER NE586/587

PRELIMINARY SPECIFICATION

F,N

DESCRIPTION

The NE586/587 is a latch/decoder/driver for 7-segment common anode LED displays. The NE586 outputs draw a constant 25mA, which is essentially independent of output voltage, power supply voltage, and temperature. The NE587 has a programmable current output up to 50mA. The data (BCD) inputs and $\overline{LE}$ (latch enable) input are low-loading so that they are compatible with any data bus system. The 7-segment decoding is implemented with a ROM so that alternative fonts can be made available.

FEATURES

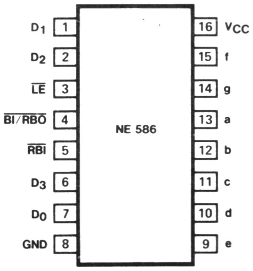
- **Latched BCD inputs**
- **Low loading bus-compatible inputs**
- **Ripple-blanking on leading and/or trailing edge zeros**
- **The NE586 is pin-compatible with 7447, 9374, and 8674**
- **Constant current outputs**

APPLICATIONS

- **Digital panel meters**
- **Measuring instruments**
- **Test equipment**
- **Digital clocks**
- **Digital bus monitoring**

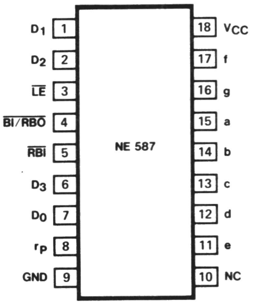
PIN CONFIGURATIONS

F,N PACKAGE



D1 1
D2 2
$\overline{LE}$ 3
$\overline{BI}/\overline{RBO}$ 4
$\overline{RBI}$ 5
D3 6
D0 7
GND 8
NE 586
16 VCC
15 f
14 g
13 a
12 b
11 c
10 d
9 e

F,N PACKAGE



D1 1
D2 2
$\overline{LE}$ 3
$\overline{BI}/\overline{RBO}$ 4
$\overline{RBI}$ 5
D3 6
D0 7
rP 8
GND 9
NE 587
18 VCC
17 f
16 g
15 a
14 b
13 c
12 d
11 e
10 NC

ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise specified

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7	V
V_{IN}	Input voltage (D_0 - D_3, $\overline{LE}$, $\overline{RBI}$)	−0.5 to +15	V
V_{OUT}	Output voltage (a-g, RBO)	−0.5 to +7	V
P_D	Power dissipation (25°C)[1]	1000	mW
T_A	Ambient temperature range	0 to 70	°C
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Soldering temperature (10 sec. max)	300	°C

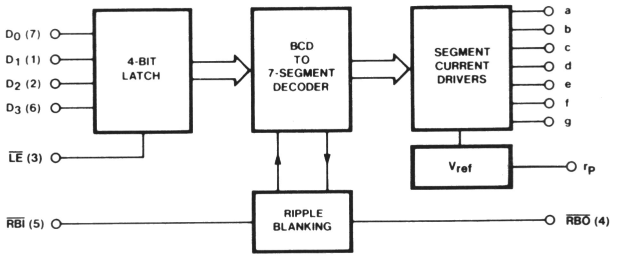
NOTE

Derate power dissipation as indicated

N package - 95°C/watt above 55°C

F package - 100°C/watt above 50°C

BLOCK DIAGRAM



D0 (7)
D1 (1)
D2 (2)
D3 (6)
$\overline{LE}$ (3)
$\overline{RBI}$ (5)
4-BIT LATCH
BCD TO 7-SEGMENT DECODER
SEGMENT CURRENT DRIVERS
Vref
RIPPLE BLANKING
a
b
c
d
e
f
g
rP
$\overline{RBO}$ (4)

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.75 to 5.25V, 0°C $< T_A <$ 70°C.
Typical values are at V_{CC} = 5V, T_A = 25°C, R_P = 1kΩ (± 1%) unless otherwise stated.

PARAMETER		TEST CONDITIONS	NE586/587			UNIT
			Min	Typ	Max	
V_{CC}	Operating supply voltage		4.75	5.00	5.25	V
V_{IH}	Input high voltage	All Inputs except $\overline{\text{BI}}$ + $\overline{\text{RBI}}$ $\overline{\text{BI}}$ $\overline{\text{RBI}}$	2.0 2.0 3.0		15 5.5 15.0	V
V_{IL}	Input low voltage		0		0.8	V
V_{IC}	Input clamp voltage	I_{IN} = −12mA, T_A = 25°C			−1.5	V
I_{IH}	Input high current	Inputs D_0 −D_3, $\overline{\text{LE}}$, $\overline{\text{RBI}}$ V_{IN} = 2.4V V_{IN} = 15V		0.1	20 250	μA μA
I_{IH}	Input high current	Input $\overline{\text{BI}}$ (pin 4) $\overline{\text{RBI}}$ = H V_{IN} = V_{CC} = 5.25V			100	μA
I_{IL}	Input low current	V_{IN} = 0.4V, Inputs D_0 − D_3 $\overline{\text{LE}}$ $\overline{\text{RBI}}$		−5 −200 −140	−50 −400 −300	μA
I_{IL}	Input low current	Input $\overline{\text{BI}}$ (pin 4) V_{CC} = 5.25.V $\overline{\text{RBI}}$ = H, V_{IN} = 0.4V		−0.45	−1.0	mA
V_{OL}	Output low voltage	Output $\overline{\text{RBO}}$ (pin 4) I_{out} = 3.0mA			0.5	V
V_{OH}	Output high voltage	Output $\overline{\text{RBO}}$ (pin 4) I_{OUT} = −50μA $\overline{\text{RBI}}$ = H	3.5	4.25		V
I_{OUT}	Output segment "ON" current (586 only)	Outputs "a" thru "g", T_A = 25°C V_{OUT} = 1.5V over temp	20 17	25 25	30 33	mA
I_{OUT}	Output segment "ON" current (587 only)	Outputs "a" thru "g" V_{OUT} = 1.5V	20	25	30	mA
ΔI_{OUT}	Output current ratio (for 587 all outputs ON)	With reference to "b" segment V_{OUT} = 1.5V	0.90	1.00	1.10	
I_{OFF}	Output segment "OFF" current	Outputs "a" thru "g" V_{OUT} = 5.0V		20	250	μA
I_{CCO}	Supply current	V_{CC} = 5.25V All outputs "ON" V_{OUT} > 1V		28	50	mA
I_{CCI}	Supply current	V_{CC} = 5.25V All outputs blanked		45	60	mA

AC ELECTRICAL CHARACTERISTICS

$V_{CC} = 5V$ $T_A = 25°C$. $R_L = 130\Omega$, $C_L = 30pF$ including probe capacity.

PARAMETER		TEST CONDITIONS	NE586/587			UNIT
			Min	Typ	Max	
t_{HL}	Propagation delay Figure 2	From data to output		85		ns
t_{LH}	Propagation delay Figure 3	From $\overline{LE}$ to output		85		ns
t_W	Latch enable pulse width Figure 4		85			ns
t_S	Latch enable setup time Figure 4	From data to $\overline{LE}$	75			ns
t_H	Latch enable hold time Figure 4	From $\overline{LE}$ to data	0			ns

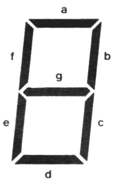
TRUTH TABLE

BINARY INPUT	INPUTS						OUTPUTS								DISPLAY
	$\overline{LE}$	$\overline{RBI}$	D_3	D_2	D_1	D_0	a	b	c	d	e	f	g	$\overline{RBO}$	
—	H	*	X	X	X	X	STABLE								STABLE
0	L	L	L	L	L	L	H	H	H	H	H	H	H	L	BLANK
0	L	H	L	L	L	L	L	L	L	L	L	L	H	H	0
1	L	X	L	L	L	H	H	L	L	H	H	H	H	H	1
2	L	X	L	L	H	L	L	L	H	L	L	H	L	H	2
3	L	X	L	L	H	H	L	L	L	L	H	H	L	H	3
4	L	X	L	H	L	L	H	L	L	H	H	L	L	H	4
5	L	X	L	H	L	H	L	H	L	L	H	L	L	H	5
6	L	X	L	H	H	L	L	H	L	L	L	L	L	H	6
7	L	X	L	H	H	H	L	L	L	H	H	H	H	H	7
8	L	X	H	L	L	L	L	L	L	L	L	L	L	H	7
9	L	X	H	L	L	H	L	L	L	L	H	L	L	H	9
10	L	X	H	L	H	L	H	H	H	H	H	H	L	H	-
11	L	X	H	L	H	H	L	H	H	L	L	L	L	H	E
12	L	X	H	H	L	L	H	L	L	H	L	L	L	H	H
13	L	X	H	H	L	H	H	H	H	L	L	L	H	H	L
14	L	X	H	H	H	L	L	L	H	H	L	L	L	H	P
15	L	X	H	H	H	H	H	H	H	H	H	H	H	H	blank
**BI	X	X	X	X	X	X	H	H	H	H	H	H	H	L**	blank

H = HIGH voltage level, output is "OFF"
L = LOW voltage level, output is "ON"
X = Don't care

* The $\overline{RBI}$ will blank the display only if a binary zero is stored in the latches.
** $\overline{RBO/BI}$ used as an input overrides all other input conditions.

SEGMENT IDENTIFICATION



NE587 PROGRAMMING

NE587 output current can be programmed by using a programming resistor, R_P, connected between r_P (pin 8) and Gnd (pin 9). The voltage at r_P (pin 8) is constant ($\approx$1.25V). A partial schematic of the voltage reference used in the NE586 and NE587 is shown in figure 1. R_P is internal for the NE586. I_P can be calculated as shown.

Output current to program current ratio, I_O/I_P, is 20 in the 15mA to 50mA range. Note that I_P must be derived from a resistor (R_P), and not from a high impedance source such as an I_{OUT} DAC used to control display brightness.

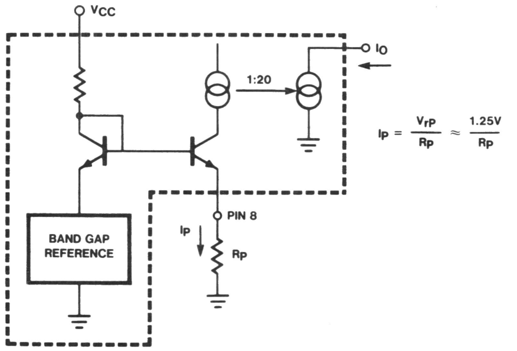


Figure 1

TIMING DIAGRAMS

PROPAGATION DELAY, DATA TO OUTPUT

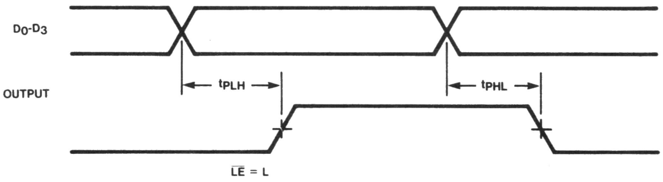


Figure 2

PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

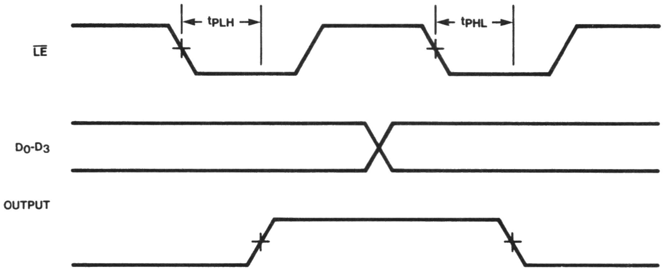


Figure 3

POWER DISSIPATION CONSIDERATIONS

LED displays are power hungry devices, and inevitably somewhat inefficient in their use of the power supply necessary to drive them. Duty cycle control does afford one way of improving display efficiency, provided that the LEDS are not driven too far into saturation, but the improvement is marginal. Operation at higher peak currents has the added advantage of giving much better matching of light output, both from segment-to-segment and digit-to-digit.

An output current of 25mA was chosen for the NE586 so that it would be suitable for multiplexed operation of large size LED digits. When designing a display system, particular care must be taken to minimize power dissipation within the IC display driver. Since the NE586 output is a constant current source, all the remaining supply voltage, which is not dropped across the LED (and the digit driver, if used), will appear across the output of the NE586. Thus, the power dissipation in the NE586 will go up sharply if the display power supply voltage rises. Clearly, then, it is good design practice to keep the display supply voltage as low as possible consistent with proper operation of the supply output current sources. Inserting a resistor or diode in series with the display supply is a good way of reducing the power dissipation within the integrated circuit segment driver, although, of course, total system power remains the same.

Power dissipation within the NE586 may be calculated as follows. Referring to figure 13, the two system power supplies are V_{CC} and V_S. In many cases, these will be the same voltage. Necessary parameters are:

V_{CC},	Supply voltage to driver
V_S,	Supply voltage to display
I_{CC},	Quiescent supply current of driver
I_{SEG},	LED segment current
V_F,	LED segment forward voltage at I_{seg}
K_{DC},	% Duty cycle

V_F, the forward LED drop, depends upon the type of LED material (hence the color) and the forward current. The actual forward voltage drops should be obtained from the LED display manufacturer's literature for the peak segment current selected; however, approximate voltages at nominal rated currents are:

Red	1.6 to 2.0V
Orange	2.0 to 2.5V
Yellow	2.2 to 3.5V
Green	2.5 to 3.5V

TIMING DIAGRAMS (Cont'd)

LATCH ENABLE PULSE WIDTH, SET-UP AND HOLD TIMES

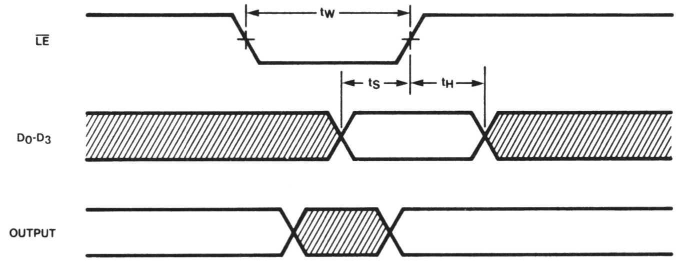


Figure 4

These voltages are all for single diode displays. Some early red displays had 2 series LEDS per segment; hence the forward voltage drop was around 3.5V.

Thus a maximum power dissipation calculation when all segments are on, is:

$P_d = V_{CC} \times I_{CC} + (V_S - V_F) \times 7 \times I_{seg} \times K_{DC}$ mW

Assuming $V_S = V_{CC} = 5.25V$
$V_F = 2.0V$
$K_{DC} = 100\%$
$P_{d\ max} = 5.25 \times 50 + 3.25 \times 7 \times 30$ mW
$= 945$ mW

TYPICAL PERFORMANCE CURVES

OUTPUT CURRENT VS OUTPUT VOLTAGE NE586

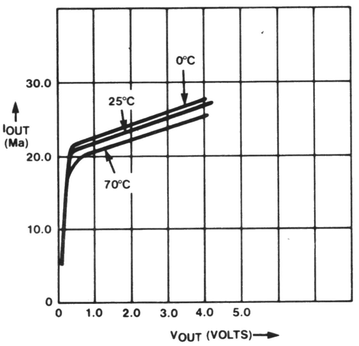


Figure 5

OUTPUT CURRENT VS OUTPUT VOLTAGE NE587 R_P = 1Kohms

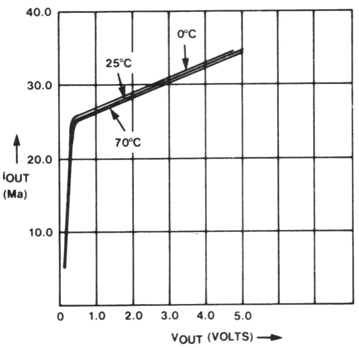


Figure 6

NORMALIZED OUTPUT CURRENT VS TEMPERATURE NE586/587 V_{CC} = 5.0 VOLTS

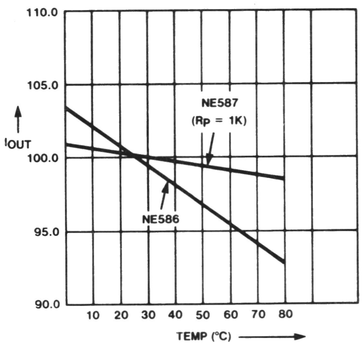


Figure 7

NORMALIZED OUTPUT CURRENT VS SUPPLY VOLTAGE NE586/587 V_O = 1.5V T_A = 25°C

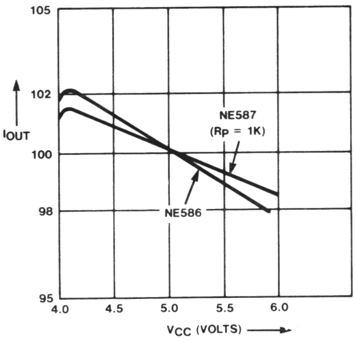


Figure 8

MAXIMUM POWER DISSIPATION VS TEMPERATURE

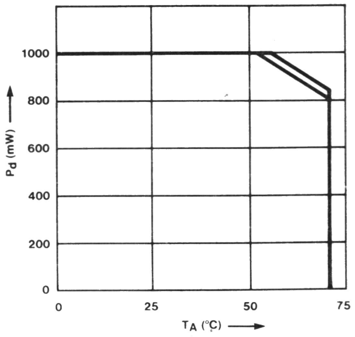


Figure 9

TYPICAL PERFORMANCE CURVES (Cont'd)

SUPPLY CURRENT VS SUPPLY VOLTAGE NE586

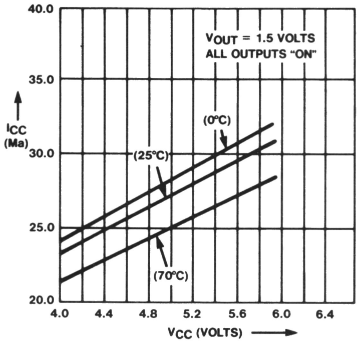


Figure 11

SUPPLY CURRENT VS SUPPLY VOLTAGE NE587

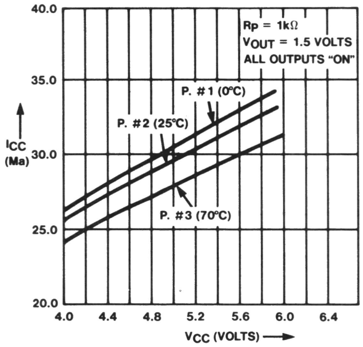
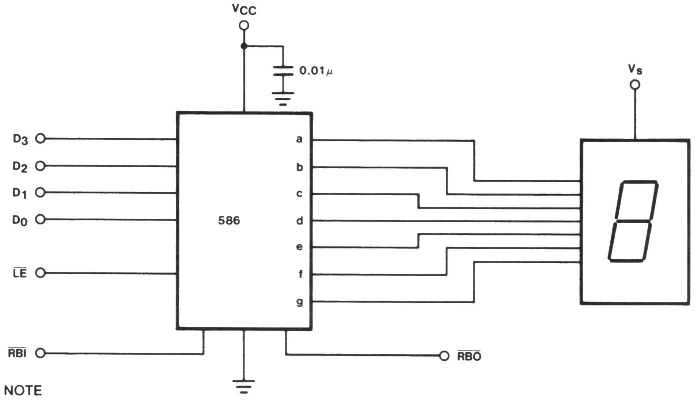


Figure 12

TYPICAL APPLICATIONS

DRIVING A SINGLE DIGIT



NOTE
Decoupling capacitor on V_{CC} should be 0.01 μF ceramic

Figure 13

However, the average power dissipation will be considerably less than this. Assuming 5 segments are on (the average for all output code combinations), then

$$P_{d\ av} = 5.0 \times 30 + 3.00 \times 5 \times 25 \text{ mW} = 525 \text{ mW}$$

Operating temperature range limitations can be deduced from the power dissipation graph in figure 9.

However, a major portion of this power dissipation ($P_{d\ max}$) is because the current source output is operating with 3.25 V across it. In practice, the outputs operate satisfactorily down to 0.5V, and so the extra voltage may be dropped external to the integrated circuit.

Suppose the worst case V_{CC}/V_S supply is 4.75 to 5.25V, and that the maximum V_E for the LED display is 2.25V. Only 2.75V is required to keep the display active, and hence 2.0V may be dropped externally with a resistor from V_{CC} to V_S. The value of this resistor is calculated by:

$$R_S = \frac{2.0}{7 \times I_{seg}} \simeq 10\Omega \text{ (½ W rating)}$$

assuming worst case I_{seg} of 30 mA

Hence now $P_{d\ max} = V_{CC} \times I_{CC} + (V_S - V_V - R_X \times 7 \times I_{seg}) \times 7 \times X I_{seg} \times K_{DC}$
$= 5.25 \times 50 + 1.25 \times 7 \times 30$ mW
$= 525$ mW

and $P_{d\ av} = 5.0 \times 30 + 1.25 \times 5 \times 25$
$= 306$ mW

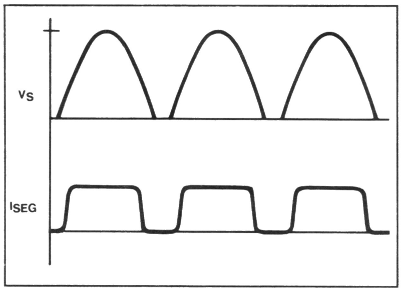
If a diode (or 2) is used to reduce voltage to the display, then the voltage appearing across the display driver will be independent of the number of "ON" segments and will be equal to

$$V_S - V_F - nV_d\,,\ V_D \simeq 0.8V$$

Where n is the number of diodes used, power dissipation can be calculated in a similiar manner.

In a multiplexed display system, the voltage drop across the digit driver must also be considered in computing device power dissipation. It may even be an advantage to use a digit driver which drops an appreciable voltage, rather than the saturating PNP transistors shown in figure 16. For example a darlington PNP or NPN emitter follower may be preferable. Figure 15 shows the NE591 as the digit driver in a multiplexed display system. The NE591 output drops about 1.8V which means that the power dissipation is evenly distributed between the two integrated circuits.

Where V_S and V_{CC} are two different supplies, the V_S supply may be optimized for minimum system power dissipation and/or cost. Clearly, good regulation in the V_S supply is totally unnecessary, and so this supply can be made much cheaper than the regulated 5V supply used in the rest of the system. In fact a simple unsmoothed full-wave rectified sine wave works extremely well if a slight loss in brightness can be tolerated. A transformer voltage of about 3-4.5V rms works well in most LED display systems. Waveforms are shown below:



The duty cycle for this system depends upon V_S, V_F and the output characteristics of the display driver.

With
$V_S = 4.9V$ pk.
$V_F = 2.0V$

The duty cycle is approximately 60%.

TYPICAL PERFORMANCE CURVES (Cont'd)

OUTPUT CURRENT VS PROGRAM RESISTOR

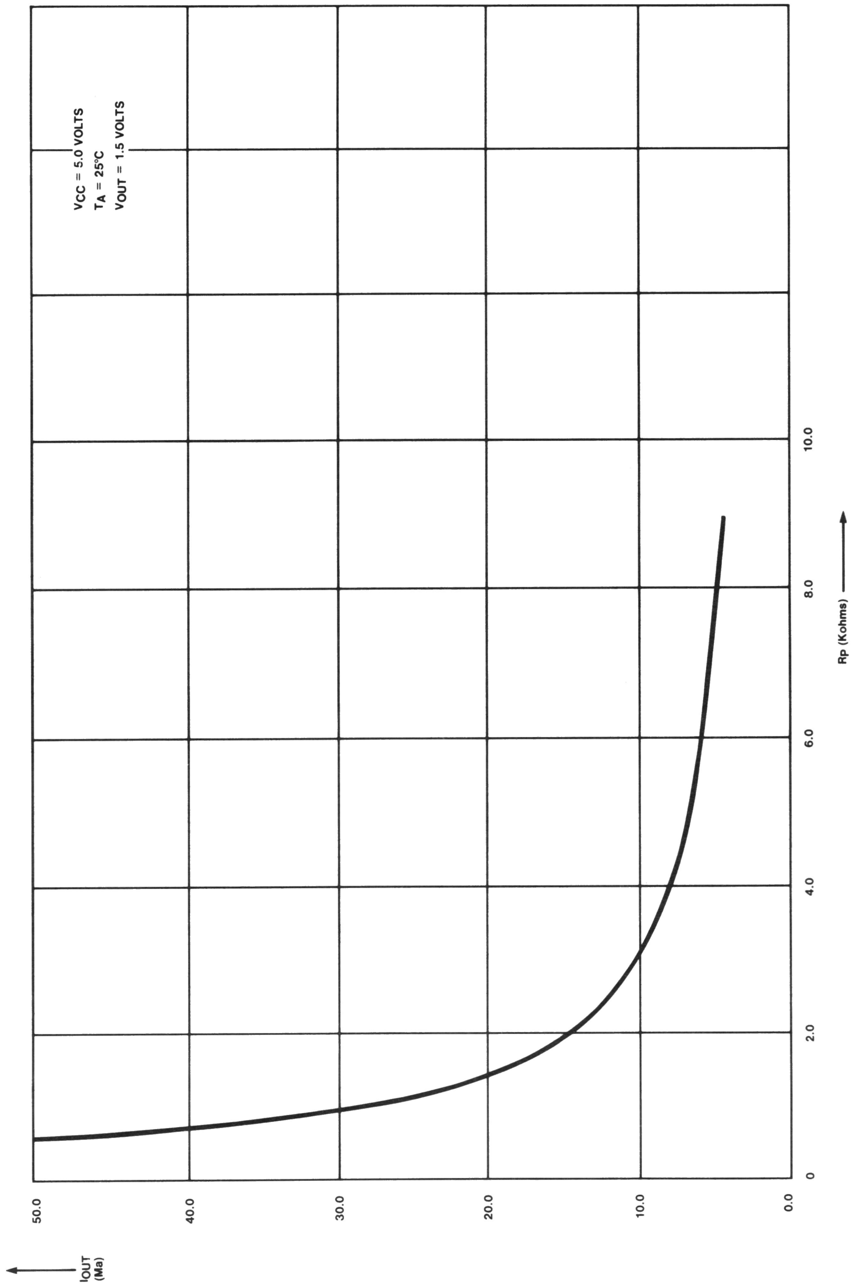


Figure 10

TYPICAL APPLICATIONS (Cont'd)

4-DIGIT DISPLAY WITH BRIGHTNESS CONTROL AND LEADING EDGE RIPPLE BLANKING

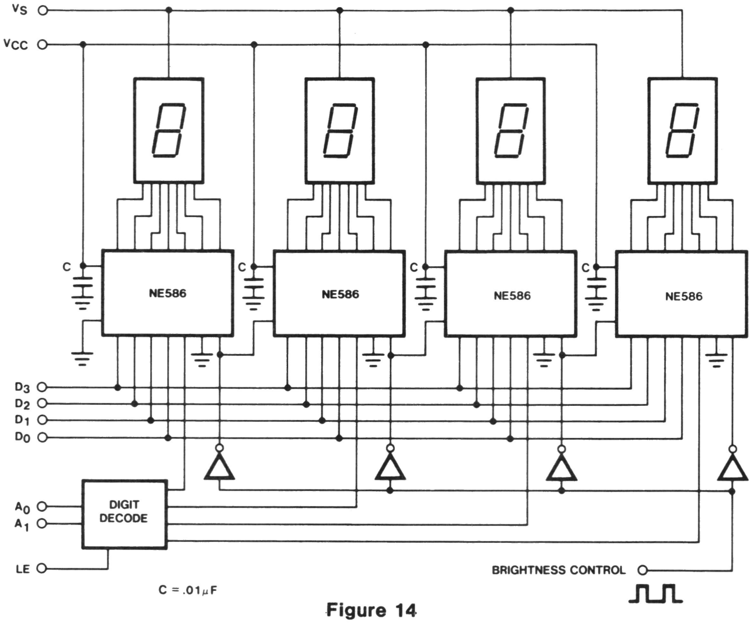

VS
VCC
C
NE586
NE586
NE586
NE586
D3
D2
D1
D0
DIGIT DECODE
A0
A1
LE
BRIGHTNESS CONTROL
C = .01μF

Figure 14

INTERFACING 8-DIGIT LED DISPLAY WITH μP BUS

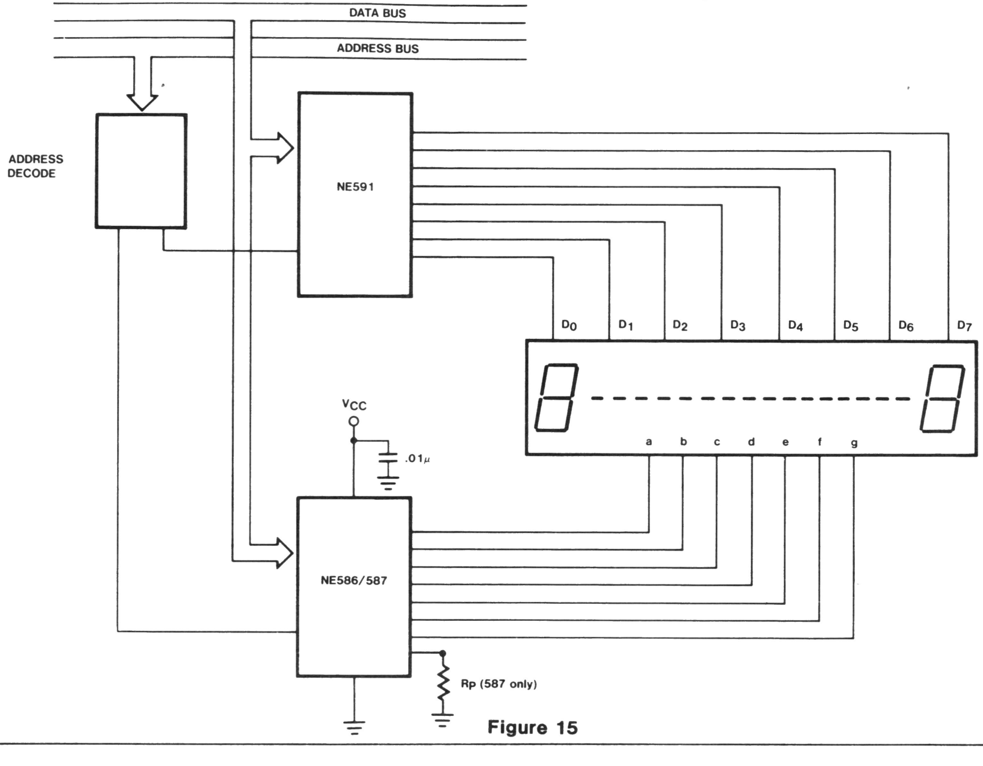

DATA BUS
ADDRESS BUS
ADDRESS DECODE
NE591
D0
D1
D2
D3
D4
D5
D6
D7
a
b
c
d
e
f
g
VCC
.01μ
NE586/587
Rp (587 only)

Figure 15

TYPICAL APPLICATIONS (Cont'd)

4-DIGIT MULTIPLEXED LED DISPLAY

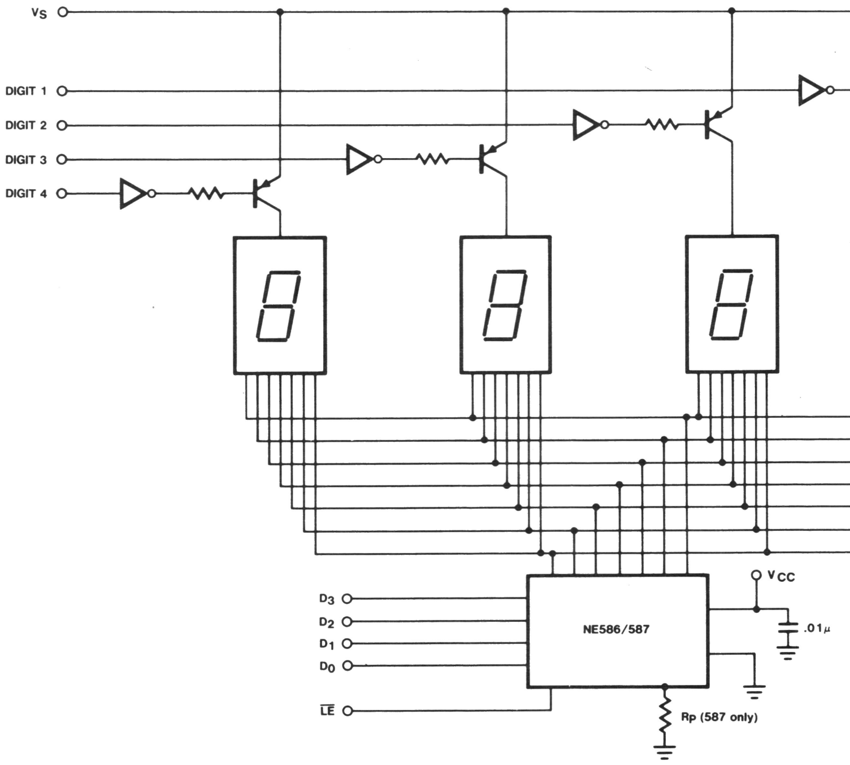

VS
DIGIT 1
DIGIT 2
DIGIT 3
DIGIT 4
NE586/587
VCC
.01μ
D_3
D_2
D_1
D_0
$\overline{LE}$
Rp (587 only)

Figure 16

VACUUM FLUORESCENT DISPLAY DRIVER SA594

PRELIMINARY SPECIFICATION

DESCRIPTION

The SA594 is a display driver interface for vacuum fluorescent displays. The device is comprised of 8 drivers and a bias network and is capable of driving the digits and/or segments of most vacuum fluorescent displays.

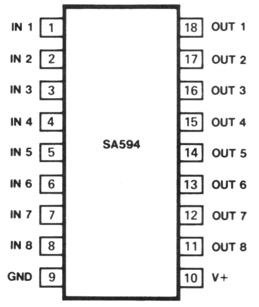
The inputs are designed to be compatible with TTL, DTL, NMOS, PMOS or CMOS output circuitry.

There is an active pull-down circuit on each output so that display ghosting is minimized and no external components are required for most fluorescent display applications.

FEATURES

- **Digit and/or segment drivers**
- **Active output pull-down circuitry**
- **High output breakdown voltage**
- **Low supply voltage**
- **Input compatible with all logic outputs**

PIN CONFIGURATION


IN 1
IN 2
IN 3
IN 4
IN 5
IN 6
IN 7
IN 8
GND
SA594
OUT 1
OUT 2
OUT 3
OUT 4
OUT 5
OUT 6
OUT 7
OUT 8
V+
1
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
10

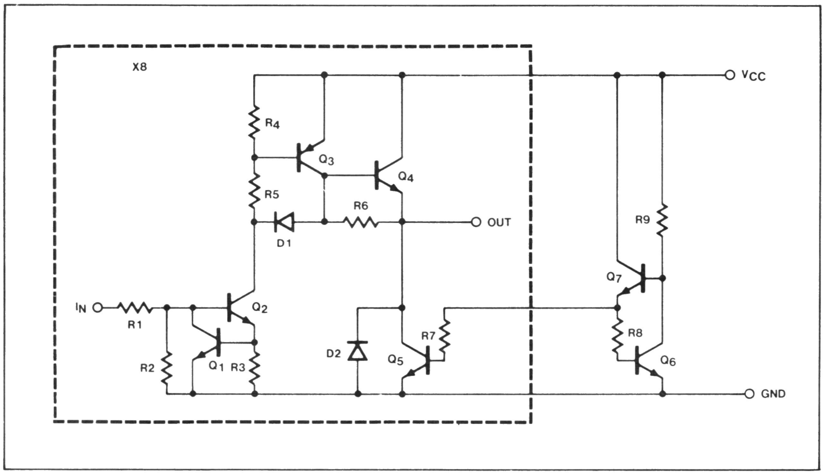
SA594N Plastic DIP
SA594F Ceramic DIP

ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise noted)

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	45	V
V_{OUT}	Output voltage	V_{CC}	
V_{IN}	Input voltage	−0.3, +20	V
I_{OUT}	Output current		
	Each output	50	mA
	All outputs	200	mA
Pd	Power dissipation* (at 25°C)	800	mW
T_A	Operating temperature range	−40 to +85	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_J	Maximum junction temperature	150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

NOTE
*Derate N (Plastic) Package above 38°C at 7.14 mW/°C.
Derate F (Ceramic) Package above 75°C at 10.8 mW/°C.

EQUIVALENT SCHEMATIC


X8
R4
Q3
Q4
R5
R6
OUT
D1
IN
R1
Q2
R2
Q1
R3
D2
Q5
R7
VCC
R9
Q7
R8
Q6
GND

DC ELECTRICAL CHARACTERISTICS $V_{CC} = +4.75$ to $+40V$, $T_A = -40$ to $+85°C$ unless otherwise stated.

PARAMETER		TEST CONDITIONS	SA594			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage range		4.75	35	40	V
I_{CCH}	Supply current (all outputs high)	$V_{CC} = 40V$ $V_{IN} = 3.5V$		3	6	mA
I_{CCL}	Supply current (all outputs low)	$V_{CC} = 40V$ $V_{IN} = 0.4V$		0.4	1	mA
V_{IN}	Input voltage range		0		15	V
V_{IH}	Input voltage to ensure logic '1'		2.6			V
V_{IL}	Input voltage to ensure logic '0'				0.8	V
I_{IH}	Input current to ensure logic '1'		100			μA
I_{IL}	Input current to ensure logic '0'				10	μA
I_{IN}	Input current	$V_{IN} = 2.6V$		60	100	μA
		$V_{IN} = 5.0V$		180	250	μA
		$V_{IN} = 15.0V$		.68	1.0	mA
V_{OH}	Output high voltage	$V_{IN} = 3.5V$, $T_A = 25°C$	$V_{CC}-1.5$	$V_{CC}-1.1$		V
		$I_{OUT} = -25mA$, Over Temp. V_{OUT} with respect to V_{CC}	$V_{CC}-2$	$V_{CC}-1.3$		V
V_{OH}	Output high, *no load* voltage	$V_{IN} = 3.5V$ $I_{OUT} = 0$, $T_A = 25°C$ V_{OUT} with respect to V_{CC}	$V_{CC}-1$	$V_{CC}-0.8$		V
V_{OFF}	Output 'OFF' voltage level	$V_{IN} = 0.8V$ $I_{OUT} = 0$		10	200	mV
I_{OH}	Available output current	$V_{CC} = 35V$ $V_{IN} = 3.5V$ $V_{OUT} = 30V$ $T_A = 25°C$	−35			mA
I_{OUT}	Output pulldown current	$V_{CC} = V_{OUT} = 35V$ Inputs open	100	200	400	μA
I_{CEX}	Output leakage current	$T_A = 25°C$ $V_{IN} = 0.4V$ $V_{CC} = 40V$, $V_{OUT} = 0V$		−1		μA

AC ELECTRICAL CHARACTERISTICS[1] $V_{CC} = 35V$, $T_A = 25°C$

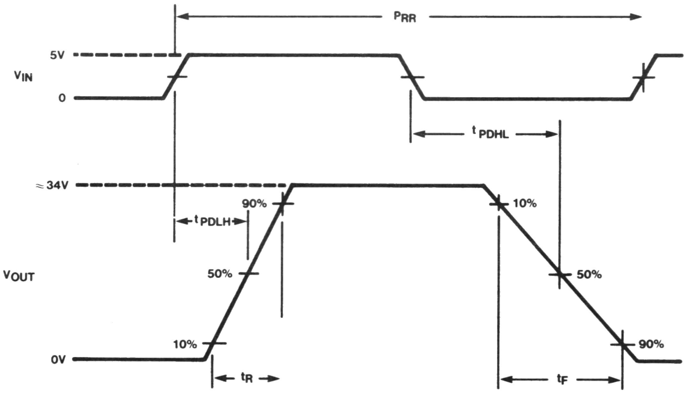
PARAMETER		TEST CONDITIONS	SA594			UNIT
			Min	Typ	Max	
t_{PdLH}	Propagation delay - low to high output transition.	50% V_{IN} to 50% V_{OUT}		1	5	μS
t_{PdHL}	Propagation delay - high to low output transition.	50% V_{IN} to 50% V_{OUT}		3	10	μS
t_R	Output rise time	10% V_{OUT} to 90% V_{OUT}		0.5	3	μS
t_F	Output fall time	90% V_{OUT} to 10% V_{OUT}		1.5	5	μS

NOTE

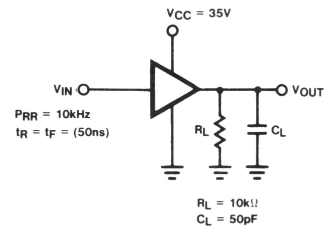
[1] See figure 1

SWITCHING TIMES OF DRIVERS

VOLTAGE WAVEFORMS


PRR
5V
VIN
0
tPDHL
≈34V
90%
tPDLH
10%
VOUT
50%
50%
10%
90%
0V
tR
tF

TEST CIRCUIT

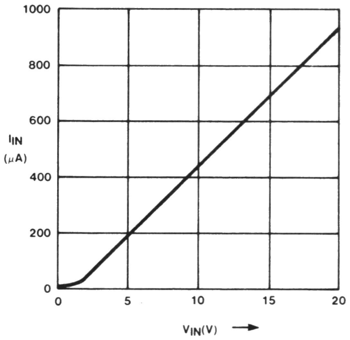

VCC = 35V
VIN
VOUT
PRR = 10kHz
tR = tF = (50ns)
RL
CL
RL = 10kΩ
CL = 50pF

INCLUDES PROBE AND FIXTURE CAPACITANCE

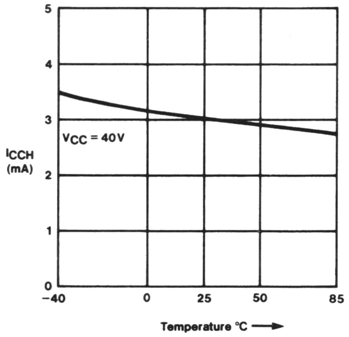
Figure 1

TYPICAL PERFORMANCE CHARACTERISTICS

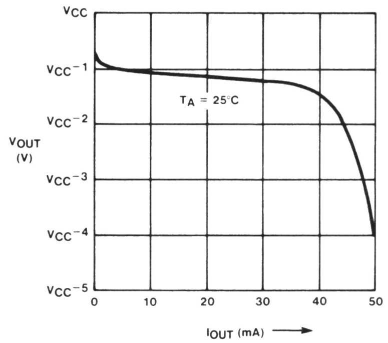
I_{IN} VS V_{IN}



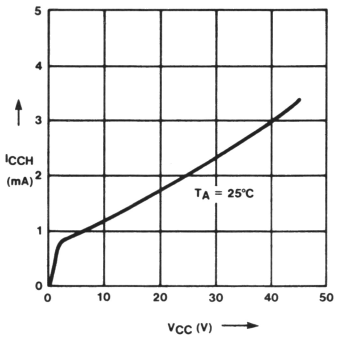
I_{CCH} VS TEMPERATURE



OUTPUT VOLTAGE VS OUTPUT CURRENT



I_{CC} VS V_{CC} (ALL INPUTS HIGH)



TYPICAL APPLICATION
DIGITAL CLOCK WITH ALARM

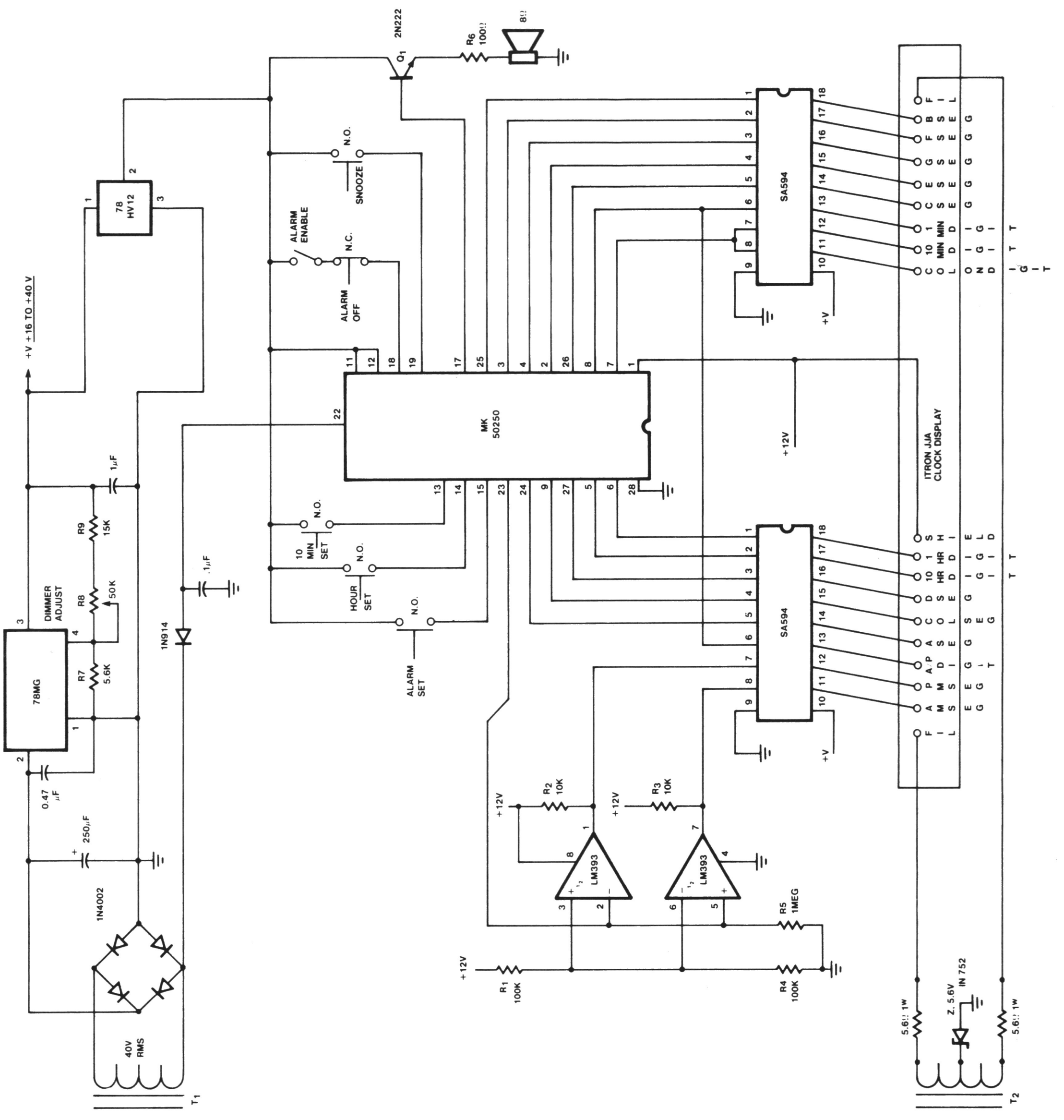

+V +16 TO +40V
78 HV12
2N222
Q1
R6 100Ω
8Ω
N.O.
SNOOZE
ALARM ENABLE
N.C.
ALARM OFF
MK 50250
SA594
SA594
+12V
ITRON JJA CLOCK DISPLAY
1μF
R9 15K
DIMMER ADJUST
R8 50K
R7 5.6K
78MG
0.47 μF
250μF
1N4002
40V RMS
T1
.1μF
1N914
10 MIN SET
HOUR SET
ALARM SET
R2 10K
R3 10K
LM393
LM393
R5 1MEG
R1 100K
R4 100K
+12V
+V
5.6Ω 1W
Z. 5.6V IN 752
T2
COLON
1 DIGIT
10 DIGIT
C SEG
E SEG
G SEG
F SEG
B SEG
FIL
MIN MIN
FIL
AM SEG
PM SEG
A.P DIGIT
A SEG
C SEG
D SEG
10 HR DIGIT
1 HR DIGIT
FIL

Figure 2

DESCRIPTION

The NE582 is a general interface device comprising a high current output transistor and drive circuitry in each of 6 elements. Each output transistor is individually capable of sinking 400mA with a typical saturation voltage of 0.5V. Input loading is such that direct interfacing with P-MOS, N-MOS, C-MOS or TTL is possible.

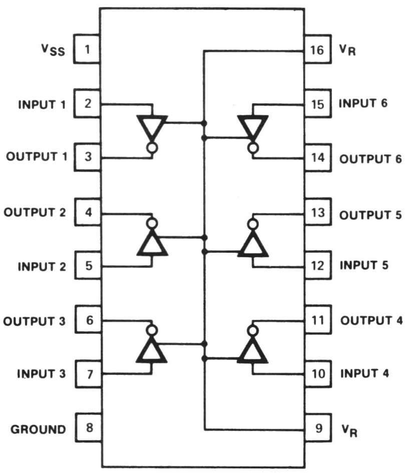
The NE582 has applications as a LED display driver, low voltage relay/lamp drivers and many others where high current capability without speed constraints is required.

The NE582 is supplied in a 16-pin high dissipation dual-in-line plastic package.

FEATURES

- **Low saturation voltage (typically 0.5V) for minimum power dissipation**
- **High output sink current capability—400mA**
- **Low input current loading for MOS compatibility**
- **Low standby power consumption**
- **Suitable for 3 volt battery operation**
- **Inputs/outputs are compatible with 75494**

PIN CONFIGURATION



ORDER PART NO.
NE582N

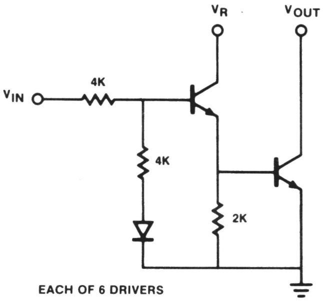
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Input voltage range[1]	-12 to V_{SS}	V
Output voltage[2]	10	V
Output to input voltage differential	10	V
Voltage at V_{SS} (pin 1)	10	V
Output current—each output	400	mA
Output current—all outputs	800	mA
Continuous total power dissipation at or below 25°C[3]	800	mW
Current in V_R (pin 9 or 16)	25	mA
Operating free-air temperature range	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature 1/16 inch from case for 10sec	260	°C

NOTES

1. The inputs are the only pins which may be negative with respect to ground.
2. Voltage values are with respect to ground.
3. Above 25°C, derate power dissipation at 6.25mW/°C.

EQUIVALENT SCHEMATIC



EACH OF 6 DRIVERS

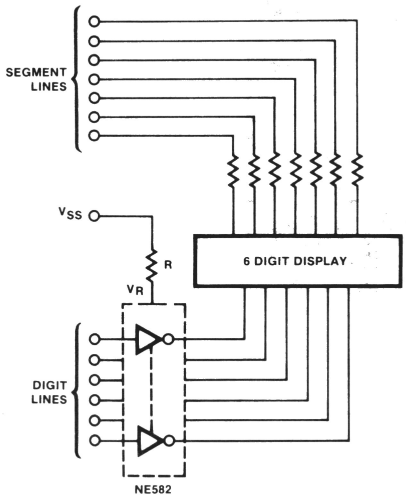
ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $70°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{OL}	Low level output voltage	V_{IN} I_R I_{OL} V mA mA 6.5 12 250 6.5 20 400 $R_{IN} = 1K$ (Series input resistance)		.320 .500	.450 .750	V V
I_{OH}	High level output current	$V_{OH} = 10V$, $I_{IN} = 40\mu A$ $V_{OH} = 10V$, $V_{IN} = 0.5V$			400 400	μA μA
I_{IN}	Input current at maximum Input voltage	$V_{IN} = 10V$, $I_{OL} = 20mA$, $I_R = 2mA$		2.2	3.3	mA
V_R		$V_{IN} = 6.5V$, $I_R = 6mA$, $I_{OL} = 80mA$		.9	1.5	V
I_{SS}	Current into pin 1	$V_{SS} = 10V$			100	μA

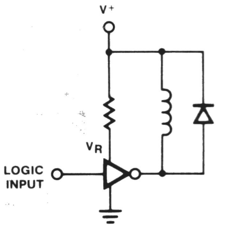
AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
T_{PLH}	Switching characteristics Propagation delay, low to high level input	$R_R = 680\Omega$ $R_L = 39\Omega$ $C_L = 15pF$		300		ns
T_{PHL}	Propagation delay, high to low level input	$V_{IH} = 7.5V$ $V_{IL} = 0V$ $t_r = t_f \leq 10ns$ $t_w = 1\mu s$ PRR = 100kHz		30		ns

TYPICAL APPLICATION FOR DIGIT DRIVING OF AN LED DISPLAY



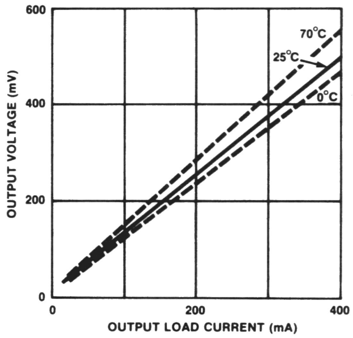
1/6 NE582 AS A RELAY DRIVER



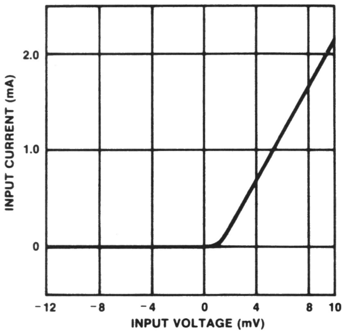
1/6 NE582 AS A RELAY DRIVER

PRELIMINARY SPECIFICATION

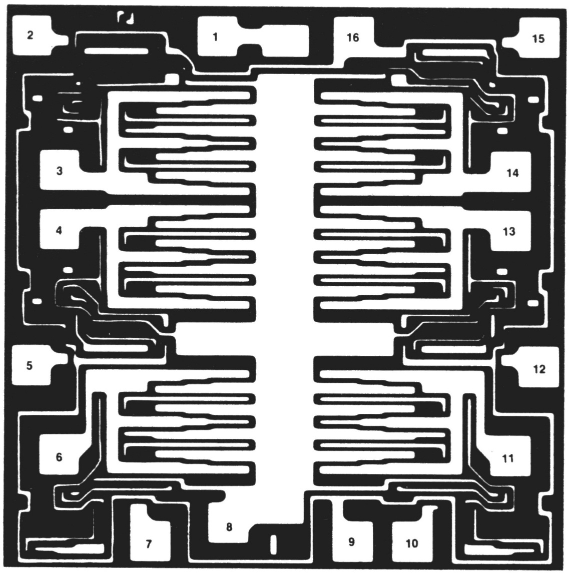
OUTPUT SATURATION VOLTAGE AS A FUNCTION OF OUTPUT LOAD CURRENT,
I_R = 25mA
V_{IN} = 6.5 VOLTS



INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE,
I_R = 25mA, V_{SS} = 10V, T_A = 25°C



CHIP LAYOUT


1
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13
14
15
16

SECTION 10

D/A-A/D CONVERTERS

Section 10—D/A—A/D CONVERTERS

NE5007 8-Bit Speed Multiplying D/A Converter 217
NE/SE5008 8-Bit Speed Multiplying D/A Converter 217
NE/SE5009 8-Bit Speed Multiplying Converter 222
NE/SE5018 8-Bit uP-Compatible D/A Converter, Voltage Output 229
NE/SE5019 8-Bit uP Compatible D/A Converter, Voltage Output 234
NE/SE5118 8-Bit uP-Compatible D/A Converter, Current Output 239
NE/SE5119 8-Bit uP-Compatible D/A Converter, Current Output 243
MC1408-8 8-Bit Multiplying D/A Converter .... *
MC1508-8 8-Bit Multiplying D/A Converter .... *
DAC-08/08A 8-Bit Multiplying D/A Converter .... *

NOTE

*Any product listed in this section but not incorporated within the text may be obtained by writing Information Services at Signetics, 811 E. Arques, M/S 027, Sunnyvale, California 94086, or by calling (408) 746-1682.

T_A

Ambient temperature range. Range of the surrounding environment of the operating device.

T_J

Junction Temperature. The maximum temperature of the device. 150°C is standard for silicon devices.

T_{STG}

Storage temperature range. Temperature range that the device can be stored in a non-operating condition.

T_{SOLD}

Soldering Temperature. The temperature which can be applied to the lead frame of the device for short periods of time (normally specified for a duration of 10 sec).

Truth Tables

0 is logic level low
1 is logic level high
X - don't care condition - has no effect under circuit conditions listed.

Absolute Maximum Rating

Operating safe zones exceeding these limits could cause permanent damage to the device and are not meant to imply that devices can operate at these limits.

Power Dissipation

The power that the device can safely handle at 25°C. The dissipation must be derated as indicated for the individual package type.

Package Type Designation

See full package designations in Appendix.

V_{CC} ($-V_{CC}$)

Supply Voltage. The range of power supply voltage over which the device will operate safely.

Accuracy

The maximum deviation of the DAC output relative to an ideal straight line drawn from zero to full scale; 1 LSB for any bit combination.

Monotonicity

For a 1 LSB increase of input code, the output either increases or remains the same.

Differential Linearity

The incremental error from an ideal 1 LSB analog output change when the digital input is changed 1 LSB; guaranteed monotonicity requires the differential linearity error be less than 1 LSB and with a tempco of essentially zero.

Absolute Accuracy

Error of a D/A converter output is the difference between the analog output expected and the actual output with a given code applied. Error of an A/D converter is the difference between the theoretical analog output required to produce a given output code and the actual input required to produce a given output code and the actual input required to produce that same code. The actual input is a range and the measured value is the midpoint of the measured band and the theoretical midpoint.

Resolution

The number of bits on the input or output of an A/D or D/A converter. The number of discrete steps or states is equal to 2^n when n is the resolution of the converter. However, n bits of resolution does not guarantee n bits of accuracy.

Quantizing Error

In an A/D converter, there is an infinite number of possible input voltages, but only 2^n output codes (n = number of bits). Therefore, there will be an error as great as 1/2LSB because of this quantizing effect and the greatest error will occur at the transition voltage where the output changes state.

No Missing Codes

This is a property of an A/D converter that is related to, but is more stringent than monotonicity. If a converter is guaranteed to have no missing codes, there will be no output digital state that will be skipped when the input voltage is varied over the entire range.

Most Significant Bit (MSB)

The highest-order bit or the bit with the greatest weight.

Least Significant Bit (LSB)

The lowest-order bit or the bit with the least weight.

Gain Error

The error in the input-to-output ratio, usually expressed in percent.

Offset Error

This is an error in the reference point of the transfer function. It appears as a constant amplitude error signal at a D/A output or an A/D input. It also appears as a constant frequency shift in the output of a V/F converter. It is nulled prior to adjusting gain error by setting the input to the most-negative input and adjusting the output to the proper value.

Settling Time

The time delay between a change of input signal value and the effected change in the output signal. It is usually expressed in terms of how long it takes the output to arrive at, and remain within, a certain error band around the final value and is often given for several different magnitudes of input step change.

Conversation Time

Time required for a complete measurement by an A/D converter. Conversion times are a function of the number of bits (resolution) and the clock frequency.

Switching Time

The time it takes for a multiplexer to change from one channel to the next with the new output signal being within a certain percentage of its final value. It is expressed for a maximum voltage transition.

Throughput Rate

An A/D converter or a data acquisition system has a finite number of points that it can convert in any given time. Throughput rate is an expression of that quantity. It is dependent on the time it takes to make a conversion and the time required to set up to make the next conversion. In a data acquisition system this time includes the composite delay due to switching and settling times of the mux, settling time of the amplifier and acquisition time of the sample-and-hold.

Full Scale Tempco

The change in DAC full scale current with change in temperature expressed in ppm/°C.

Differential Non-Linearity Tempco

The non-linearity specification over a specified range of temperatures. This specification generally appears as the range of temperatures that the device is monotonic (DAC) or has no missing codes (ADC).

Leakage Current

Multiplexer input current that does not flow through to the output but is shunted internally. It is also current that flows from OFF channels into the ON channel. In a current output D/A converter, there is a digital input code that ideally yields zero output current. If current flows with that input code, it is called leakage current. It is analogous to output voltage offset in a voltage-output D/A converter.

Power Supply Sensitivity

The change in DAC output current with changes in power supply voltage.

Output Voltage Compliance

The range of allowable voltage levels the output pins can assume without a major effect on circuit performance.

Compliance Voltage Range

For a current source the maximum range of terminal voltage for which the current source will maintain its specified values.

NOTE
Refer to Section 5 (Interface Circuits) of the 1979 Analog Applications Manual for an in-depth explanation of Converters and their applications

SIGNETICS REPLACEMENT STANDARDS

SE/NE 5018 DAC

COMPETITION	INDUSTRY VALUE	KEY PARAMETER	SIGNETICS AVAILABLE VALUE	SIGNETICS ORIGINATED DEVICES	QR&A		COMMENTS
					SURE II	SUPR II	
AMD Analog Devices Datel Fairchild Harris Precision National	8	Resolution (Bits)	8 Bits	NE5018 SE5018 NE5019 SE5019	Yes Yes Yes Yes	Yes Yes Yes Yes	*Not pin for pin replacement. Do not have total capability of the NE5018 μP compatible series.
	.19	Linearity	0.1 %				
	2- 300 μ sec	Settling Time ½ LSB	2 μsec				
	10-50	Gain TC	20 PPM/°C				
	0-4	Current (Output)	mA	NE/SE 5118 NE/SE 5119	Yes Yes	Yes Yes	
	−10 to +18	Voltage (Output)	0-10 ±5 Volts	NE5018 SE5019	Yes Yes	Yes Yes	

DAC-08/08A

COMPETITION	INDUSTRY VALUE	KEY PARAMETER	SIGNETICS AVAILABLE VALUE	SIGNETICS ORIGINATED DEVICES	QR&A		COMMENTS
					SURE II	SUPR II	
AMD Analog Devices Datel Motorola National	8	Resolution	8 Bits	NE/SE5008 NE/SE5009	Yes Yes	Yes Yes	
	.19	Linearity	19 %FS	NE/SE5008 NE/SE5009	Yes Yes	Yes Yes	
	85-300	Settling time	135 nsec	NE/SE5008 NE/SE5009	Yes Yes	Yes Yes	
	48-500	Power supply regulator	48 mW	NE/SE5008 NE/SE5009	Yes Yes	Yes Yes	

8-BIT HIGH SPEED MULTIPLYING D/A CONVERTER NE5007/5008/SE5008

NE5007/5008, SE5008-F,N

DESCRIPTION

The 5007/5008 series of 8-bit monolithic multiplying Digital-to-Analog Converters provide very high speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85ns settling times with very low glitch and at low power consumption. Monotonic multiplying performance is attained over a wide 40 to 1 reference current range. Matching to within 1 LSB between reference and full scale currents eliminates the need for full scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

Dual complementary outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. True high voltage compliance outputs allow direct output voltage conversion and eliminate output op amps in many applications.

All 5007/5008 series models guarantee full 8-bit monotonicity and linearities as tight as 0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the ±4.5V to ±18V power supply range, with 33mW power consumption attainable at ±5V supplies.

The compact size and low power consumption make the 5007/5008 attractive for portable and military/aerospace applications.

FEATURES

- **Fast settling output current—85ns**
- **Full scale current prematched to ±1 LSB**
- **Direct interface to TTL, CMOS, ECL, HTL, PMOS**
- **Relative accuracy to 0.1% maximum over temperature range**
- **High output compliance—-10V to +18V**
- **True and complemented outputs**
- **Wide range multiplying capability**
- **Low FS current drift—±10ppm/°C**
- **Wide power supply range—±4.5V to ±18V**
- **Low power consumption—33mW at ±5V**
- **SE5008 military qualifications pending**

APPLICATIONS

- **8-bit, 1μs A-to-D converters**
- **Servo-motor and pen drivers**
- **Waveform generators**
- **Audio encoders and attenuators**
- **Analog meter drivers**
- **Programmable power supplies**
- **CRT display drivers**
- **High speed modems**
- **Other applications where low cost, high speed and complete input/output versatility are required**

ORDERING INFORMATION

RELATIVE ACCURACY	0 to 70°C	-55 to 125°C
0.39% FS	NE5007N NE5007F	-
0.19% FS	NE5008N NE5008F	SE5008F

DEFINITION OF TERMS

Accuracy—The maximum deviation of the Dac output relative to an ideal straight line drawn from zero to full scale; 1 LSB for any bit combination

Differential linearity—The incremental error from an ideal 1 LSB analog output change when the digital input is changed 1 LSB; guaranteed monotonicity requires the differential linearity error be less than 1 LSB and with a tempco of essentially zero

Full scale tempco—The change in Dac full scale current with change in temperature expressed in ppm/°C

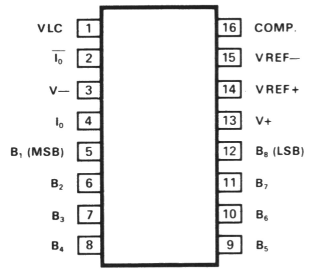
Monotonicity—For a 1 LSB increase of input code, the output either increases or remains the same

Output voltage compliance—The range of allowable voltage levels the output pins can assume without a major effect on circuit performance

Power supply sensitivity—The change in Dac output current with changes in power supply voltage

PIN CONFIGURATION

F,N PACKAGE*



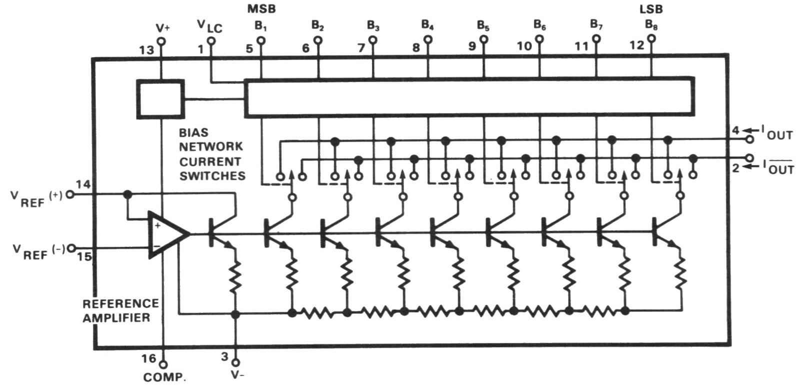
*N = Plastic DIP
F = Cerdip

CROSS REFERENCE

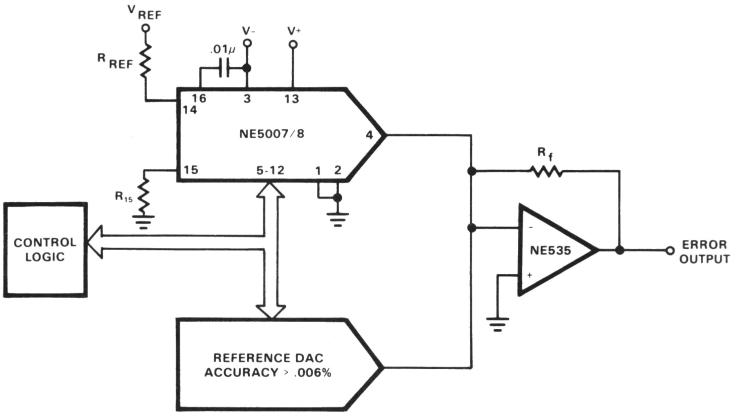
The 5007/5008 series are pin and functionally compatible with the DAC-08 series of devices.

PMI	SIGNETICS
DAC-08A	SE5009
DAC-08	SE5008
DAC-08H	NE5009
DAC-08E	NE5008
DAC-08C	NE5007

BLOCK DIAGRAM



TEST CIRCUIT


V REF
R REF
.01μ
V-
V+
16
3
13
14
NE5007/8
4
15
5-12
1
2
R15
Rf
CONTROL LOGIC
NE535
ERROR OUTPUT
REFERENCE DAC ACCURACY > .006%

ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

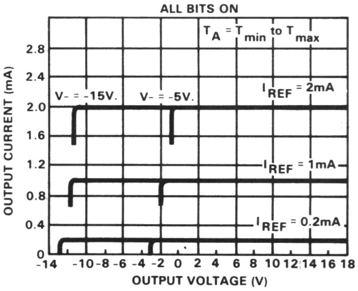
	PARAMETER	RATING	UNIT
T_A	Operating temperature range		°C
	SE5008	-55 to +125	
	NE5007/8	0 to +70	
t_{stg}	Storage temperature	-65 to +150	°C
P_D	Power dissipation	500	mW
	Lead soldering temperature (60sec)	300	°C
	V+ to V- supply	36	V
	Logic inputs	V- to V- plus 36V	
V_{LC}	Logic threshold control	V- to V+	
	Analog current outputs	See output current or output voltage performance curve	
V_{14}, V_{15}	Reference inputs	V- to V+	
V_{14} to V_{15}	Reference input differential voltage	±18	V
I_{14}	Reference input current	5.0	mA

AC ELECTRICAL CHARACTERISTICS V_S = ±15V, I_{REF} = 2.0mA, Output characteristics refer to both IOUT and $\overline{\text{IOUT}}$ unless otherwise noted. NE5008: T_A = 0°C to 70°C. SE5008: T_A = -55°C to 125°C.

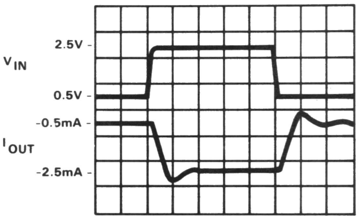
PARAMETER		TEST CONDITIONS	NE5007			NE5008			SE5008			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	8	8	8	Bits
	Relative accuracy	Over temperature range			±0.39			±0.19			±0.19	%FS
t_S	Settling time	To ±½ LSB, all bits switched on or off, T_A=25°C		85	135		85	135		85	135	ns
t_{PLH} t_{PHL}	Propagation delay Low-to-high High-to-low	T_A=25°C, each bit. All bits switched		35	60		35	60		35	60	ns
TCI_{FS}	Full scale tempco			±10			±10			±10		ppm/°C
V_{OC}	Output voltage compliance	Full scale current change <½ LSB	-10		+18	-10		+18	-10		+18	V
I_{FS4}	Full scale current	V_{REF}=10.000V, R_{14}, R_{15}=5.000kΩ, T_A=25°C	1.94	1.99	2.04	1.94	1.99	2.04	1.94	1.99	2.04	mA
I_{FSS}	Full scale symmetry	$I_{FS4}-I_{FS2}$		±2.0	±16		±1.0	±8.0		±1.0	±8.0	μA
I_{ZS}	Zero scale current			0.2	4.0		0.2	2.0		0.2	2.0	μA
I_{FSR}	Output current	V-=-5.0V	0	2.0	2.1	0	2.0	2.1	0	2.0	2.1	mA
		V-=-7.0V to -18V	0	2.0	4.2	0	2.0	4.2	0	2.0	4.2	
	Logic input levels											V
V_{IL}	Low	V_{LC}=0V			0.8			0.8			0.8	
V_{IH}	High		2.0			2.0			2.0			
	Logic input current	V_{LC}=0V										μA
I_{IL}	Low	V_{IN}=-10V to +0.8V		-2.0	-10		-2.0	-10		-2.0	-10	
I_{IH}	High	V_{IN}=2.0V to 18V		0.002	10		0.002	10		0.002	10	
V_{IS}	Logic input swing	V-=-15V	-10		+18	-10		+18	-10		+18	V
V_{THR}	Logic threshold range	V_S=±15V	-10		+13.5	-10		+13.5	-10		+13.5	V
I_{15}	Reference bias current			-1.0	-3.0		-1.0	-3.0		-1.0	-3.0	μA
dI/dt	Reference input slew rate	Figures 1, 3	4.0	8.0		4.0	8.0		4.0	8.0		mA/μs
	Power supply sensitivity	I_{REF}=1mA										%FS/%VS
$PSSI_{FS+}$	Positive	V+=4.5 to 5.5V, V-=-15V; V+=13.5 to 16.5V, V-=-15V		0.0003	0.01		0.0003	0.01		0.0003	0.01	
$PSSI_{FS-}$	Negative	V-=-4.5 to -5.5V, V+=+15V; V-=-13.5 to -16.5, V+=+15V		0.002	0.01		0.002	0.01		0.002	0.01	
	Power supply current											mA
I+	Positive	V_S=±5V, IREF=1.0mA		2.3	3.8		2.3	3.8		2.3	3.8	
I-	Negative			-4.3	-5.8		-4.3	-5.8		-4.3	-5.8	
I+	Positive	V_S=+5V, -15V, I_{REF}=2.0mA		2.4	3.8		2.4	3.8		2.4	3.8	
I-	Negative			-6.4	-7.8		-6.4	-7.8		-6.4	-7.8	
I+	Positive	V_S=±15V, I_{REF}=2.0mA		2.5	3.8		2.5	3.8		2.5	3.8	
I-	Negative			-6.5	-7.8		-6.5	-7.8		-6.5	-7.8	
P_D	Power dissipation	±5V, I_{REF}=1.0mA		33	48		33	48		33	48	mW
		+5V, -15V, I_{REF}=2.0mA		108	136		108	136		108	136	
		±15V, I_{REF}=2.0mA		135	174		135	174		135	174	

TYPICAL PERFORMANCE CHARACTERISTICS

OUTPUT CURRENT vs OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE)

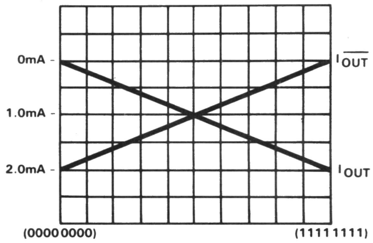


FAST PULSED REFERENCE OPERATION

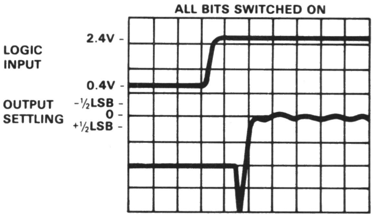


200ns/division
See Figure 1
R_{EQ} = 200Ω, R_L = 100Ω, CC = O

TRUE AND COMPLEMENTARY OUTPUT OPERATION



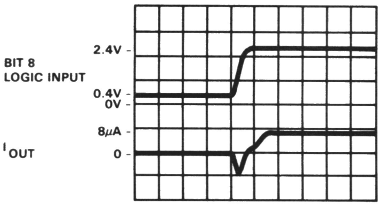
FULL SCALE SETTLING TIME



50ns/division

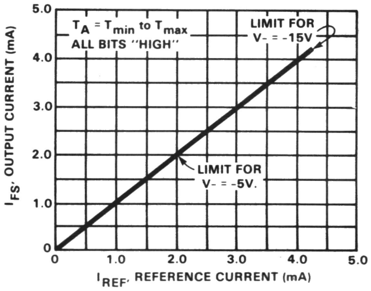
IFS = 2mA, R_L = 1kΩ ½ LSB = 4μA

LSB SWITCHING

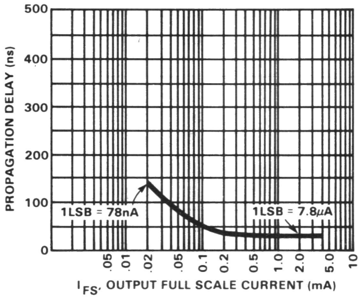


50ns/division

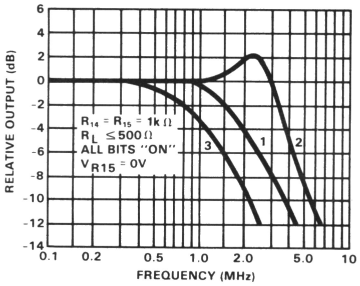
FULL SCALE CURRENT vs REFERENCE CURRENT



LSB PROPAGATION DELAY vs IFS



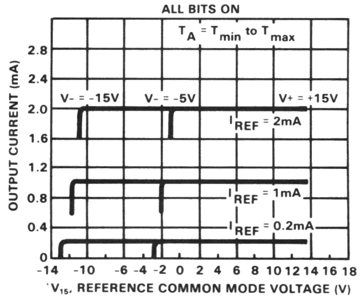
REFERENCE INPUT FREQUENCY RESPONSE



Curve 1: CC = 15pF, V_{IN} = 2.0V p-p centered at +1.0V.
Curve 2: CC = 15pF, V_{IN} = 50mV p-p centered at +200mV.
Curve 3: CC = 0pF, V_{IN} = 100mV p-p centered at 0V and applied thru 50Ω connected to pin 14. +2.0V applied to R_{14}.

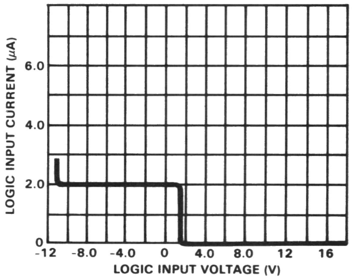
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

REFERENCE AMP COMMON MODE RANGE

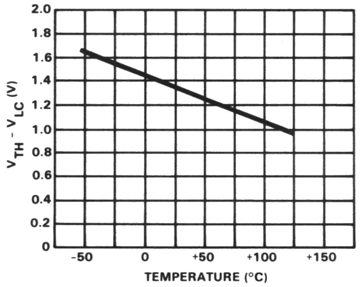


Positive common mode range is always (V+) - 1.5V

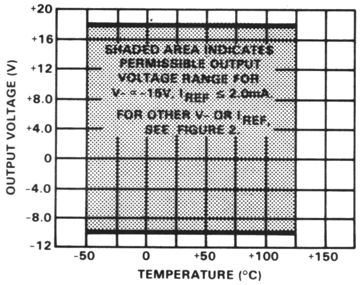
LOGIC INPUT CURRENT vs INPUT VOLTAGE



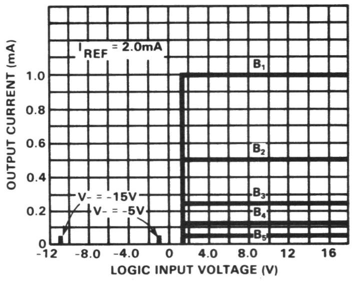
V_{TH} - V_{LC} vs TEMPERATURE



OUTPUT VOLTAGE COMPLIANCE vs TEMPERATURE



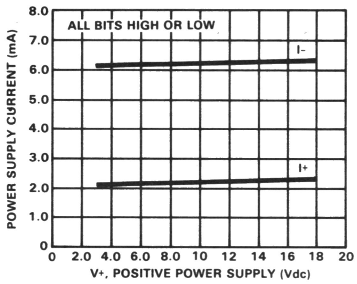
BIT TRANSFER CHARACTERISTICS



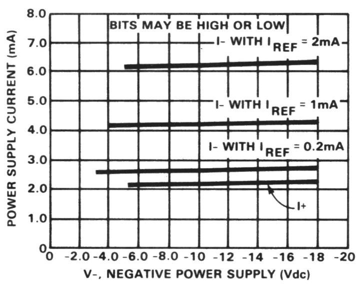
NOTE

B_1 through B_8 have identical transfer characteristics. Bits are fully switched, with less than ½ LSB error, at less than ±100mV from actual threshold. These switching points are guaranteed to lie between 0.8 and 2.0 volts over the operating temperature range (VLC = 0.0V).

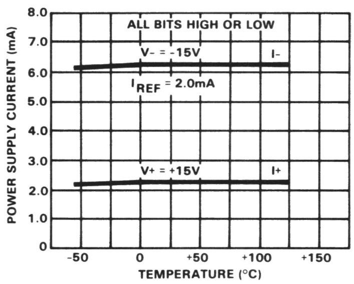
POWER SUPPLY CURRENT vs V+



POWER SUPPLY CURRENT vs V-

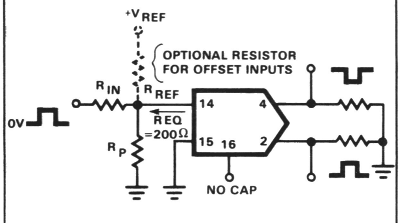


POWER SUPPLY CURRENT vs TEMPERATURE



TYPICAL APPLICATION

PULSED REFERENCE OPERATION



TYPICAL VALUES

R_{IN} = 5K
$+V_{IN}$ = 10V

8-BIT HIGH SPEED MULTIPLYING D/A CONVERTER NE/SE5009

NE5009-F,N • SE5009-F

DESCRIPTION

The 5009 monolithic 8-bit digital-to-analog converter is an electrical selection of the 5007/8 series of 8-bit D/A converters. Relative accuracy is specified to ±1/4 LSB maximum over the operating temperature range. Differential nonlinearity and settling times are also specified to maximum limits.

The device is specifically designed for precision applications in process control and military systems. The SE5009 is specified as equal or superior to the PMI DAC-08A in all respects. Additional relevant testing and application material is shown in the data sheet and application notes for the NE5007/8.

FEATURES

- **Fast settling output current—60ns typical, 135ns maximum**
- **Relative accuracy— ±0.1% maximum**
- **Differential nonlinearity—±0.19% maximum**
- **Low full-scale current drift, ±10 ppm/°C typical**
- **SE5009 military qualifications pending**

APPLICATIONS

- **Fast 8-bit A/D converter**
- **Variable gain amplifiers**
- **Waveform generators**
- **3 digit BCD D/A converter (0.1%)**
- **Programmable power supplies**

DEFINITION OF TERMS

Relative Accuracy—The maximum deviation of the DAC output relative to an ideal straight line drawn from zero to full scale; 1 LSB for any bit combination.

Differential Nonlinearity—The incremental error from an ideal 1 LSB analog output change when the digital input is changed 1 LSB; guaranteed monotonicity requires the differential linearity error be less than 1 LSB and with a tempco of essentially zero.

Full Scale Tempco—The change in DAC full scale current with change in temperature expressed in ppm/°C.

Monotonicity—For a 1 LSB increase of input code, the output either increases or remains the same.

Output Voltage Compliance—The range of allowable voltage levels the output pins can assume without a major effect on circuit performance.

Power Supply Sensitivity—The change in DAC output current with changes in power supply voltage.

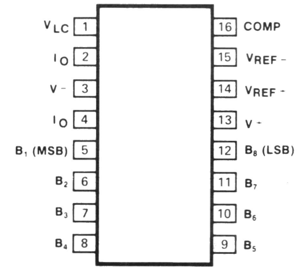
CROSS REFERENCE

The 5009 series are pin and functionally compatible with the DAC-08 series of devices.

PMI	SIGNETICS
DAC-08A	SE-5009
DAC-08	SE-5008
DAC-08H	NE-5009
DAC-08E	NE-5008
DAC-08C	NE-5007

PIN CONFIGURATION

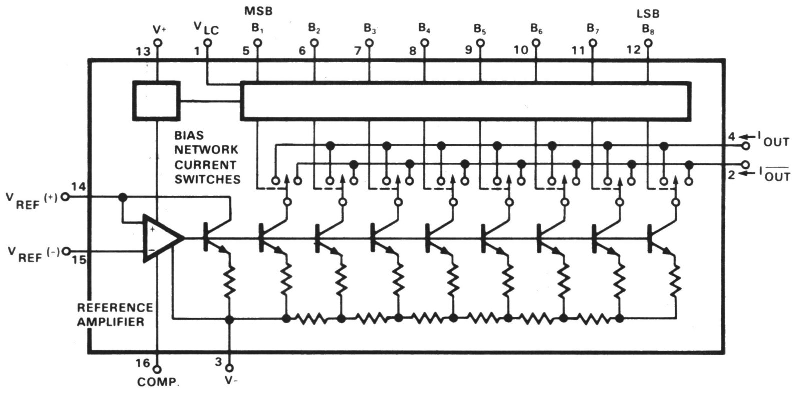
F,N PACKAGE*



NOTE

*SE5009 is in F package only.

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise specified.

PARAMETER	RATING	UNIT
Total supply voltage (V+ - V-)	36	V
Logic input voltage	V- + 36	V
V_{LC} Voltage at pin 1	V- to V+	V
Reference input voltage	V- to V+	V
Reference input differential voltage	±18	V
Reference input current	5.0	mA
Operating temperature range		
SE5009	-55 to +125	°C
NE5009	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead soldering temperature (10sec)	300	°C
Power dissipation*	500	mW

NOTE

*Derate F package at 10mW/°C above 100°C.

DC ELECTRICAL CHARACTERISTICS

These specs apply for V_S = ± 15V, I_{REF} = 2mA,
T_A for NE5009 0° to 70°C, T_A for SE5009 -55° to +125°C.
Output characteristic for both I_{OUT} and $\overline{I_{OUT}}$.

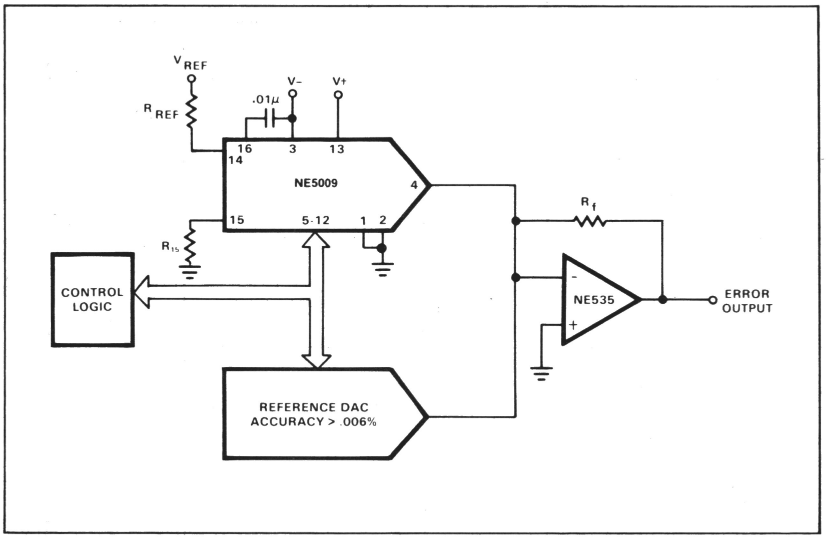
PARAMETER		TEST CONDITIONS	NE5009			SE5009			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	bits
	Monotonicity		8	8	8	8	8	8	bits
	Relative accuracy	Over temperature range			±0.1			±0.1	% FS
	Differential nonlinearity			±0.1	±0.19		±0.1	±0.19	% FS
TCI_{FS}	Full scale tempco			±10	±50		±10	±50	ppm/°C
V_{OC}	Output voltage compliance	Full scale current change < 1/2 LSB	-10		+18	-10		+18	V
I_{FS4}	Full scale current	V_{REF} = 10.000V, R_{14}·R_{15} = 5.000K T_A = 25°C	1.984	1.992	2.000	1.984	1.992	2.000	mA
I_{FSS}	Full scale symmetry	I_{FS4} - I_{FS2}		±0.5	±4.0		±0.5	±4.0	μA
I_{ZS}	Zero scale current			0.1	1.0		0.1	1.0	μA
I_{FSR}	Output current range	V- = -5.0V	0	2.0	2.1	0	2.0	2.1	mA
		V- = -7.0V to -18V	0	2.0	4.2	0	2.0	4.2	mA
	Logic input levels								
V_{IL}	Logic "0"	V_{LC} = 0V			0.8			0.8	V
V_{IH}	Logic "1"	V_{LC} = 0V	2.0			2.0			V
	Logic input current	V_{LC} = 0V							
I_{IL}	Logic "0"	V_{IN} = -10V to +0.8V		-2.0	-10		-2.0	-10	μA
I_{IH}	Logic "1"	V_{IN} = 2.0V to 18V		0.002	10		0.002	10	μA
V_{IS}	Logic input swing	V- = -15V	-10		+18	-10		+18	V
V_{THR}	Logic threshold range	V_S = ±15V	-10		+13.5	-10		+13.5	V
I_{15}	Reference bias current			-1.0	-3.0		-1.0	-3.0	μA
di/dt	Reference input slew rate		4.0	8.0		4.0	8.0		mA/μs
	Power supply sensitivity								
PSSIFS+		I_{REF} = 1mA, V- = -15V:							
		V+ = 4.5 to 5.5V		0.0003	0.01		0.0003	0.01	%FS/%VS
		V+ = 13.5 to 16.5V		0.0003	0.01		0.0003	0.01	%FS/%VS
PSSIFS-		I_{REF} = 1mA, V+ = +15V:							
		V- = -4.5 to -5.5V		0.0003	0.01		0.0003	0.01	%FS/%VS
		V- = -13.5 to -16.5V		0.0003	0.01		0.0003	0.01	%FS/%VS
	Power supply current	V_S = ±15V, I_{REF} = 1.0mA							
I+				2.3	3.8		2.3	3.8	mA
I-				-4.3	-5.8		-4.3	-5.8	mA
	Power supply current	V_S = +5V, -15V; I_{REF} = 2.0mA							
I+				2.4	3.8		2.4	3.8	mA
I-				-6.4	-7.8		-6.4	-7.8	mA
	Power supply current	V_S = ±15V, I_{REF} = 2.0mA							
I+				2.5	3.8		2.5	3.8	mA
I-				-6.5	-7.8		-6.5	-7.8	mA
P_D	Power dissipation	±5V, I_{REF} = 1.0mA		33	48		33	48	mW
		+5V, -15V, I_{REF} = 2.0mA		108	136		108	136	mW
		±15V, I_{REF} = 2.0mA		135	174		135	174	mW

AC ELECTRICAL CHARACTERISTICS

These specs apply for $V_S = \pm 15V$, $I_{REF} = 2mA$, Output characteristic for both I_{OUT} and $\overline{I_{OUT}}$.

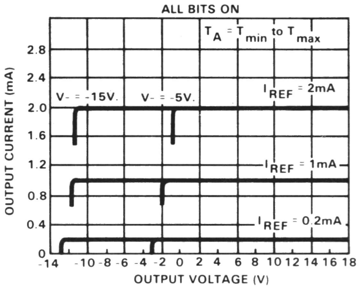
PARAMETER		TEST CONDITIONS	SE/NE5009			UNIT
			Min	Typ	Max	
t_s	Settling time	To ±1/2 LSB all bits switched ON or OFF, $T_A = 25°C$		60	135	ns
	Major carry transition	To 90% complete, $T_A = 25°C$		20		ns
t_{PLH}, t_{PHL}	Propagation delay	$T_A = 25°C$				
	Each bit			35	60	ns
	All bits switched			35	60	ns

TEST CIRCUIT

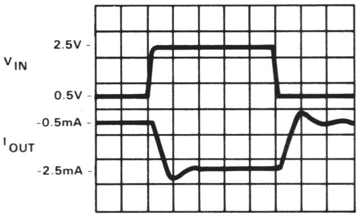

V REF
R REF
.01µ
V-
V+
16
14
3
13
NE5009
4
15
5-12
1 2
R15
R f
CONTROL LOGIC
NE535
ERROR OUTPUT
REFERENCE DAC ACCURACY > .006%

TYPICAL PERFORMANCE CHARACTERISTICS

OUTPUT CURRENT vs OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE)

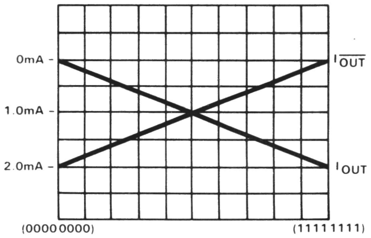


FAST PULSED REFERENCE OPERATION



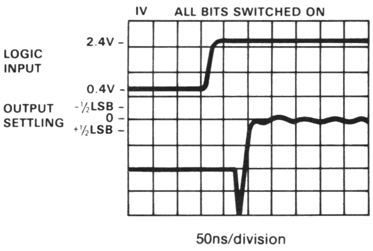
200ns/division
See Figure 1
$R_{EQ} = 200\Omega$, $R_L = 100\Omega$, CC = O

TRUE AND COMPLEMENTARY OUTPUT OPERATION



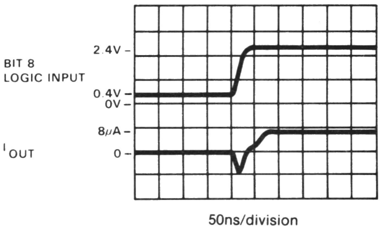
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

FULL SCALE SETTLING TIME

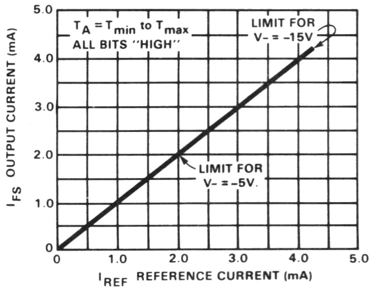


See Figure 13 for settling time fixture

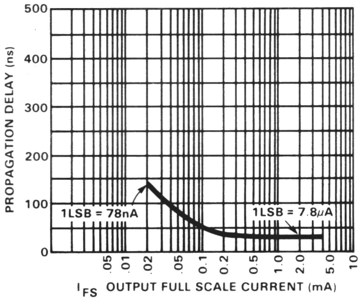
LSB SWITCHING



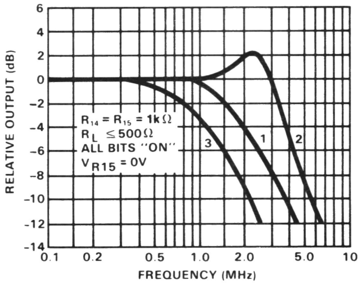
FULL SCALE CURRENT vs REFERENCE CURRENT



LSB PROPAGATION DELAY vs IFS



REFERENCE INPUT FREQUENCY RESPONSE

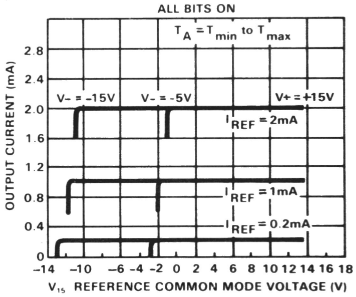


Curve 1:CC = 15pF, V_{IN} = 2.0V p-p centered at +1.0V.

Curve 2:CC = 15pF, V_{IN} = 50mV p-p centered at +200mV.

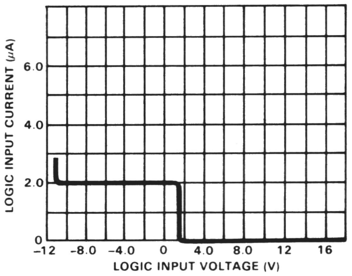
Curve 3:CC = 0pF, V_{IN} = 100mV p-p centered at 0V and applied thru 50Ω connected to pin 14. +2.0V applied to R_{14}.

REFERENCE AMP COMMON MODE RANGE

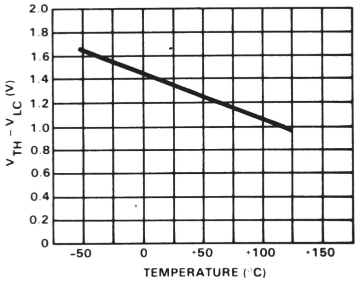


Positive common mode range is always (V+) - 1.5V

LOGIC INPUT CURRENT vs INPUT VOLTAGE

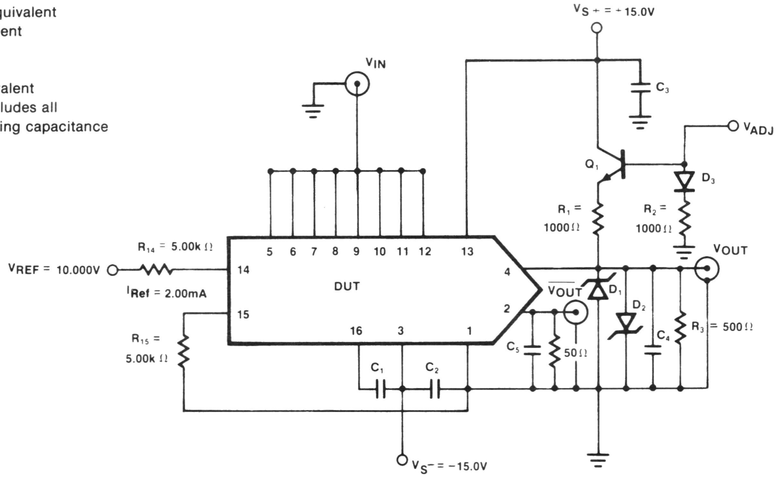


V_{TH}-V_{LC} vs TEMPERATURE

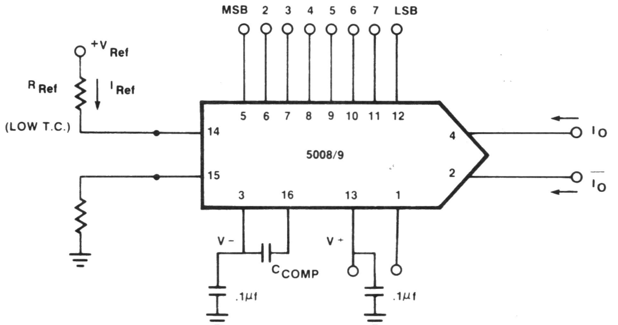


SETTLING TIME AND PROPAGATION DELAY

D_1, D_2 = IN6263 or equivalent
D_3 = IN914 or equivalent
C_1 = 0.01μf
C_2, C_3 = 0.1μf
Q_1 = 2N3904 or equivalent
C_4, C_5 = 15pf and includes all
probe and fixturing capacitance

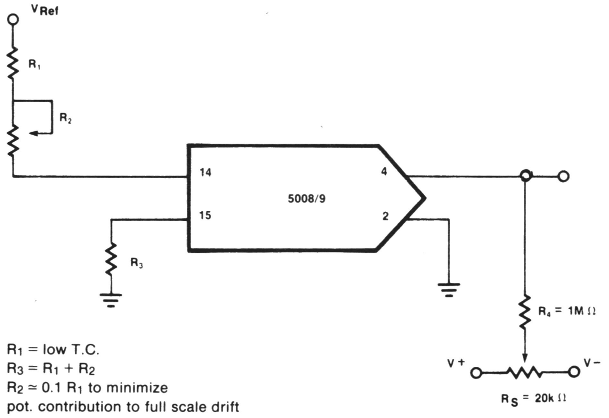

VS+ = +15.0V
VIN
C3
VADJ
Q1
D3
R1 = 1000Ω
R2 = 1000Ω
VOUT
R14 = 5.00kΩ
VREF = 10.000V
IRef = 2.00mA
5 6 7 8 9 10 11 12 13
14
DUT
4
VOUT
D1
D2
2
15
16 3 1
R15 = 5.00kΩ
C5
50Ω
C4
R3 = 500Ω
C1
C2
VS− = −15.0V

BASIC 5008/5009 CONFIGURATION


MSB 2 3 4 5 6 7 LSB
+V Ref
R Ref
I Ref
(LOW T.C.)
5 6 7 8 9 10 11 12
14
4
IO
5008/9
15
2
IO
3 16 13 1
V−
V+
CCOMP
.1μf
.1μf

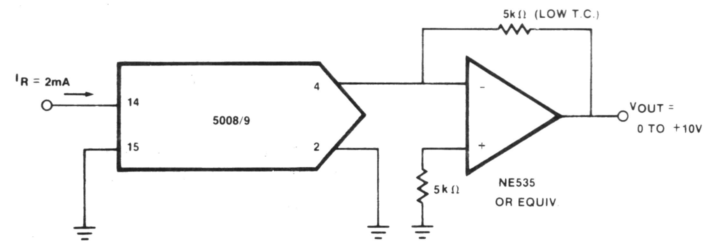
$$I_{FS} \approx \frac{+V_{Ref}}{R_{Ref}} \times \frac{255}{256} \text{ ; } I_O + \bar{I}_O = I_{FS} \text{ for all logic states}$$

RECOMMENDED FULL SCALE AND ZERO SCALE ADJ.


VRef
R1
R2
14
4
5008/9
15
2
R3
R4 = 1M Ω
V+
V−
RS = 20k Ω

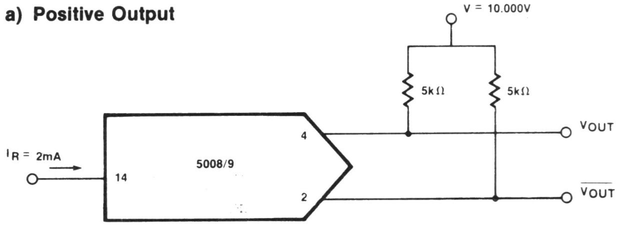
R_1 = low T.C.
$R_3 = R_1 + R_2$
$R_2 \simeq 0.1\ R_1$ to minimize
pot. contribution to full scale drift

UNIPOLAR VOLTAGE OUTPUT FOR LOW IMPEDANCE OUTPUT

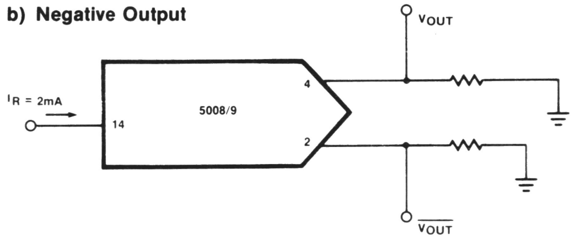

5kΩ (LOW T.C.)
I_R = 2mA
14
15
5008/9
4
2
-
+
5kΩ
NE535
OR EQUIV
V_{OUT} =
0 TO +10V

UNIPOLAR VOLT OUTPUT FOR HIGH IMPEDANCE OUTPUT

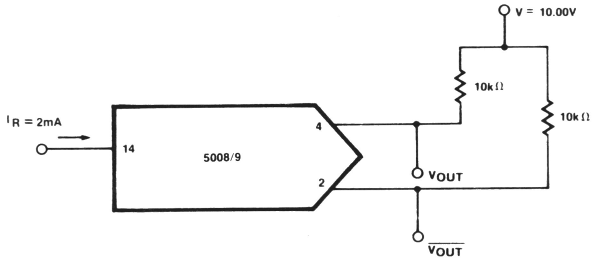
a) Positive Output


V = 10.000V
5kΩ
5kΩ
I_R = 2mA
14
5008/9
4
2
V_{OUT}
$\overline{V_{OUT}}$

b) Negative Output


V_{OUT}
I_R = 2mA
14
5008/9
4
2
$\overline{V_{OUT}}$

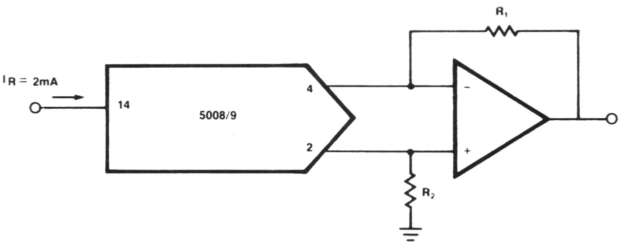
BASIC BIPOLAR OUTPUT OPERATION (OFFSET BINARY)


V = 10.00V
10kΩ
10kΩ
I_R = 2mA
14
5008/9
4
2
V_{OUT}
$\overline{V_{OUT}}$

CODE CHART

	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	V_{OUT}	$\overline{V_{OUT}}$
POS full scale	1	1	1	1	1	1	1	1	- 9.920V	+10.000
POS f.s. - 1LSB	1	1	1	1	1	1	1	0	- 9.840V	+9.920
+ Zero scale + 1LSB	1	0	0	0	0	0	0	1	- 0.080V	+0.160
Zero scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero scale - 1LSB	0	1	1	1	1	1	1	1	0.080	0.000
Neg full scale - 1LSB	0	0	0	0	0	0	0	1	+ 9.920	-9.840
Neg full scale	0	0	0	0	0	0	0	0	+10.000	-9.920

SYMMETRICAL OFFSET BINARY (BIPOLAR)


I_R = 2mA
14
5008/9
4
2
R_1
R_2
-
+

V_{OUT} = 0 to ±V*

±V *Range:
±5V for $R_1 = R_2$ = 2.5K
±10V for $R_1 = R_2$ = 5.0K

3 DIGIT BCD CONVERTER

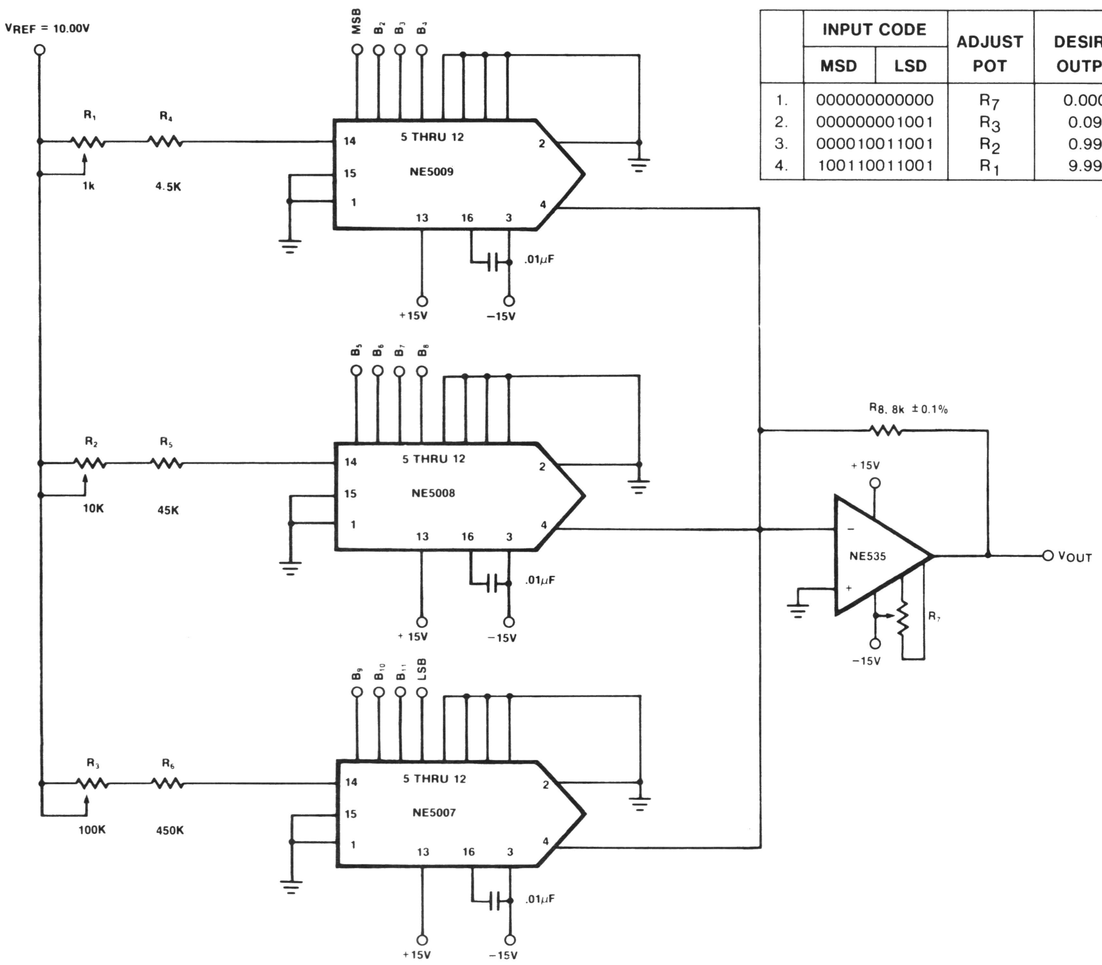
A 3 digit BCD converter, using inexpensive 8-bit binary DACs, can achieve ±0.1% accuracy. The circuit shown in Figure 20 utilizes three DACs, one for each decade, to provide 0 to 999 output steps. DAC 1 contains the first four significant digits controlling the hundreds digit; DAC 2 controls the tens digit and DAC 3 steps 0 to 9. The feedback resistor (R_7) sets the full scale at 9.99V.

The input coding is the popular 8-4-2-1 coding; i.e. the weighting ratios are 8, 4, 2 and 1. The full scale (999) BCD code is input code 100110011001.

Full scale adjustment procedure.

In the sequence below, switch on the following code combinations and adjust the indicated potentiometer for the proper output.

3 DIGIT BCD CONVERTER WITH ±0.1% ACCURACY


V_{REF} = 10.00V
MSB
B_2
B_3
B_4
R_1
R_4
1k
4.5K
14
15
1
5 THRU 12
NE5009
2
4
13
16
3
.01µF
+15V
−15V
B_5
B_6
B_7
B_8
R_2
R_5
10K
45K
NE5008
B_9
B_{10}
B_{11}
LSB
R_3
R_6
100K
450K
NE5007
R_8, 8k ±0.1%
NE535
R_7
VOUT

	INPUT CODE		ADJUST POT	DESIRED OUTPUT
	MSD	LSD		
1.	000000000000		R_7	0.000V
2.	000000001001		R_3	0.09V
3.	000010011001		R_2	0.99V
4.	100110011001		R_1	9.99V

8-BIT μP-COMPATIBLE D/A CONVERTER SE/NE5018

SE/NE5018 F,N

DESCRIPTION

The NE5018 is a complete 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most micro-processors.

The chip also comprises a stable voltage reference (5V nominal) and a high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

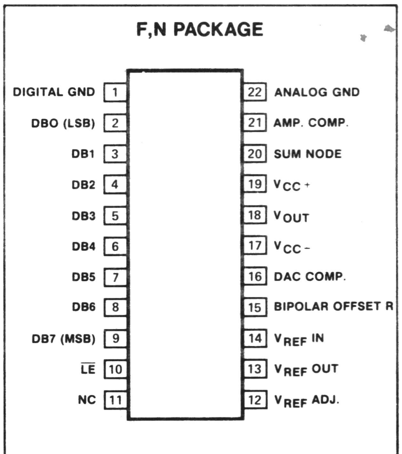
FEATURES

- **8-bit resolution**
- **Input latches**
- **Low-loading data inputs**
- **On-chip voltage reference**
- **Output buffer amplifier**
- **Accurate to ± 1/4 LSB (.1%)**
- **Monotonic to 8 bits**
- **Amplifier and reference both short-circuit protected**
- **Compatible with 2650,8080 and many other μP's**

APPLICATIONS

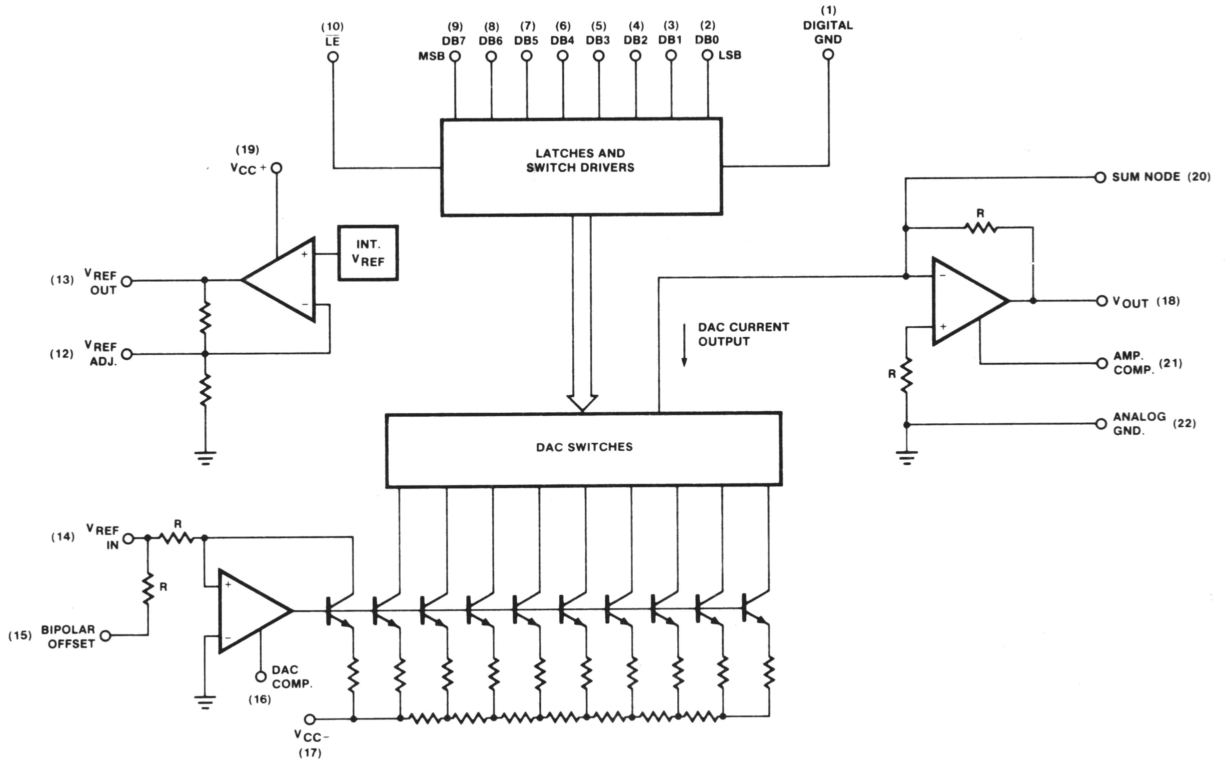
- **Precision 8-bit D/A converters**
- **A/D converters**
- **Programmable power supplies**
- **Test equipment**
- **Measuring instruments**
- **Analog-digital multiplication**

PIN CONFIGURATION


F,N PACKAGE
DIGITAL GND 1
DBO (LSB) 2
DB1 3
DB2 4
DB3 5
DB4 6
DB5 7
DB6 8
DB7 (MSB) 9
LE 10
NC 11
22 ANALOG GND
21 AMP. COMP.
20 SUM NODE
19 VCC+
18 VOUT
17 VCC-
16 DAC COMP.
15 BIPOLAR OFFSET R
14 VREF IN
13 VREF OUT
12 VREF ADJ.

SE/NE5018 available in F package only.

BLOCK DIAGRAM


(10) LE
(9) DB7
(8) DB6
(7) DB5
(6) DB4
(5) DB3
(4) DB2
(3) DB1
(2) DB0
MSB
LSB
(1) DIGITAL GND
LATCHES AND SWITCH DRIVERS
(19) VCC+
INT. VREF
(13) VREF OUT
(12) VREF ADJ.
SUM NODE (20)
R
VOUT (18)
AMP. COMP. (21)
ANALOG GND. (22)
DAC CURRENT OUTPUT
DAC SWITCHES
(14) VREF IN
R
R
(15) BIPOLAR OFFSET
DAC COMP. (16)
VCC- (17)

All R values equal 5KΩ and are thermally matched.

Figure 1

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF}IN$	Voltage at V_{REF} input	12	V
$V_{REF}ADJ$	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at V_{REF} OUT	Continuous	
I_{OUTSC}	Short-circuit current to ground or either supply at V_{OUT}	Continuous	
I_{REF}	Reference input current	5	mA
P_D	Power dissipation*		
	-N package	800	mW
	-F package	1000	mW
T_A	Operating temperature range		
	SE5018	−55 to +125	°C
	NE5018	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES

For N package, derate at 120°C/W above 35°C

For F package, derate at 75°C/W above 75°C

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5018. $-55°C \leq T_A \leq 125°C$, NE5018. $0°C \leq T_A \leq 70°C$ unless otherwise specified.[1] Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	SE5018			NE5018			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy				±0.1			±0.1	%FS
$V_{CC}+$	Positive supply voltage		11.4	15		11.4	15		V
$V_{CC}-$	Negative supply voltage		−11.4	−15		−11.4	−15		V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1 = 0V	2.0			2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1 = 0V			0.8			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1 = 0V, $2V < V_{IN} < 18V$		0.1	10		0.1	10	μA
$I_{IN(0)}$	Logic "0" input current	Pin 1 = 0V, $-5V < V_{IN} < 0.8V$		−2.0	−10		−2.0	−10	μA
V_{FS}	Full scale output voltage	Unipolar operation $V_{REF\ IN} = 5.000V$, $T_A = 25°C$	9.50	9.961	10.50	9.50	9.961	10.50	V
V_{FS}	Full scale output voltage	Bipolar operation $V_{REF\ IN} = 5.000V$, $T_A = 25°C$		+4.961 −5.000			+4.961 −5.000		V
V_{ZS}	Zero scale voltage			5			5		mV
I_{OS}	Output short circuit current	$T_A = 25°C$ $V_{OUT} = 0V$		15	40		15	40	mA
PSR+(out)	Output power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01		.001	.01	%FS/%VS
PSR−(out)	Output power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq -16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01		.001	.01	%FS/%VS
TC_{FS}	Full scale temperature coefficient	$V_{REF\ IN} = 5.000V$		20			20		ppm/°C
TC_{ZS}	Zero scale temperature coefficient			5			5		ppm/°C

DC ELECTRICAL CHARACTERISTICS (Cont'd) $V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5018. $-55°C \leq T_A \leq 125°C$, NE5018. $0°C \leq T_A \leq 70°C$ unless otherwise specified.[1] Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	SE/5018			NE5018			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{REF}	Reference output current	$\Delta V_{REF} \leq 0.1\%$		5			5		mA
I_{REFSC}	Reference short circuit current	$T_A = 25°C$ $V_{REF\ OUT} = 0V$		15			15		mA
$PSR+_{(REF)}$	Reference power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, $I_{REF} = 1.0mA$		.003	.01		.003	.01	%VR/ %VS
$PSR-_{(REF)}$	Reference power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq 16.5V$,		.003	.01		.003	.01	%VR/ %VS
V_{REF}	Reference voltage	$I_{REF} = 1.0mA$	4.5	5.0	5.5	4.5	5.0	5.5	V
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$		60			60		ppm/°C
Z_{IN}	DAC V_{REF} IN input impedance	$I_{REF} = 1.0mA$	4.0	5.0	6.0	4.0	5.0	6.0	KΩ
$I_{CC}+$	Positive supply current	$V_{CC}+ = 15V$		7	14		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		−10	−15		−10	−15	mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$		255	435		255	435	mW

NOTE

[1] Refer to Figure 2.

AC ELECTRICAL CHARACTERISTICS[2] $V_{CC} = \pm 15V$, $T_A = 25°C$

PARAMETER		TO	FROM	TEST CONDITIONS	SE/NE5018			UNIT
					Min	Typ	Max	
T_{SLH}	Settling time	±½ LSB	Input	All bits low to high[3]		1.8		μs
T_{SHL}	Settling time	±½ LSB	Input	All bits high to low[4]		2.3		μs
t_{plh}	Propagation delay	Output	Input	All bits switched low to high[3]		300		ns
t_{phl}	Propagation delay	Output	Input	All bits switched high to low[4]		150		ns
t_{plsb}	Propagation delay	Output	Input	1 LSB change[3,4]		150		ns
t_{plh}	Propagation delay	Output	$\overline{LE}$	low to high transition[5]		300		ns
t_{phl}	Propagation delay	Output	$\overline{LE}$	high to low transition[6]		150		ns
t_s	Set-up time	$\overline{LE}$	Input	2, 7	100			ns
t_h	Hold time	Input	$\overline{LE}$	2, 7	50			ns
t_{pw}	Latch enable pulse width			2, 7	150			ns
	Reference input Slew rate			2		25		v/μs

NOTES

[2] Refer to Figure 3.
[3] See Figure 6.
[4] See Figure 7.
[5] See Figure 8.
[6] See Figure 9.
[7] See Figure 10.

DC PARAMETRIC TEST CONFIGURATION

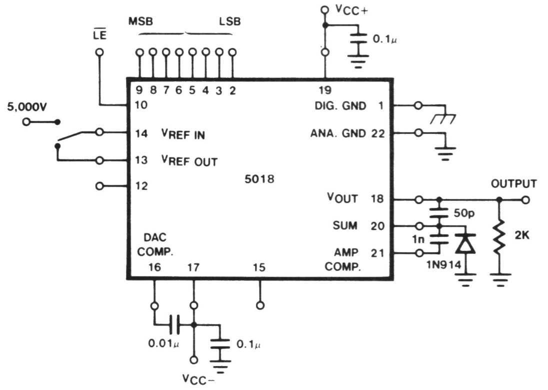

LE
MSB
LSB
VCC+
0.1μ
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
5,000V
14 VREF IN
ANA. GND 22
13 VREF OUT
12
5018
OUTPUT
VOUT 18
SUM 20
50p
1n
2K
DAC COMP.
AMP COMP. 21
1N914
16
17
15
0.01μ
0.1μ
VCC−

Figure 2

AC PARAMETRIC TEST CONFIGUTATION

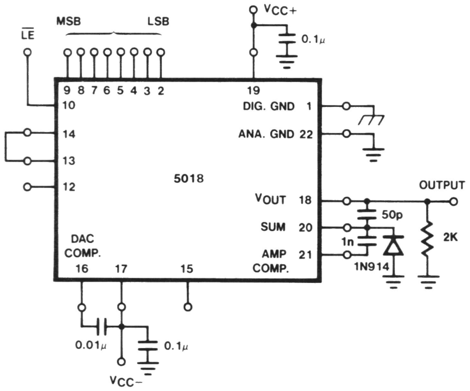

LE
MSB
LSB
VCC+
0.1μ
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
14
ANA. GND 22
13
12
5018
OUTPUT
VOUT 18
SUM 20
50p
1n
2K
DAC COMP.
AMP COMP. 21
1N914
16
17
15
0.01μ
0.1μ
VCC−

Figure 3

FULL/ZERO SCALE ADJUST—UNIPOLAR OUTPUT (0-10V)

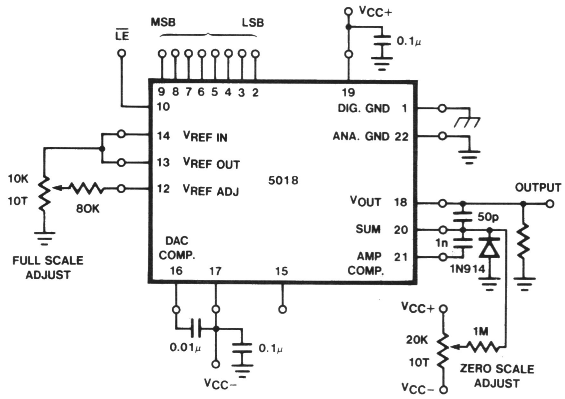

LE
MSB
LSB
VCC+
0.1μ
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
14 VREF IN
ANA. GND 22
13 VREF OUT
12 VREF ADJ
5018
10K
10T
80K
FULL SCALE ADJUST
OUTPUT
VOUT 18
SUM 20
50p
1n
DAC COMP.
AMP COMP. 21
1N914
16
17
15
0.01μ
0.1μ
VCC−
VCC+
20K
10T
1M
ZERO SCALE ADJUST
VCC−

Figure 4

BIPOLAR OUTPUT OPERATION (−5 to +5V)

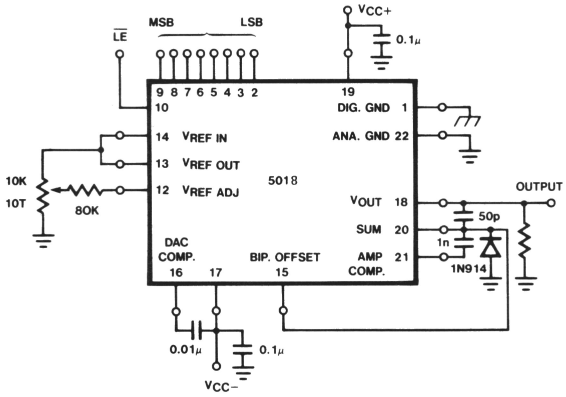

LE
MSB
LSB
VCC+
0.1μ
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
14 VREF IN
ANA. GND 22
13 VREF OUT
12 VREF ADJ
5018
10K
10T
80K
OUTPUT
VOUT 18
SUM 20
50p
1n
DAC COMP.
BIP. OFFSET
AMP COMP. 21
1N914
16
17
15
0.01μ
0.1μ
VCC−

Figure 5

SETTLING TIME AND PROPAGATION DELAY, LOW TO HIGH DATA

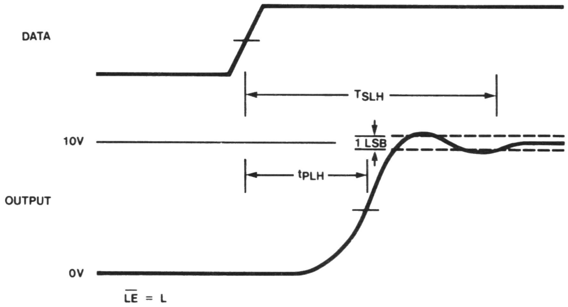

DATA
TSLH
10V
1 LSB
tPLH
OUTPUT
0V
LE = L

Figure 6

SETTLING TIME AND PROPAGATION DELAY, HIGH TO LOW DATA

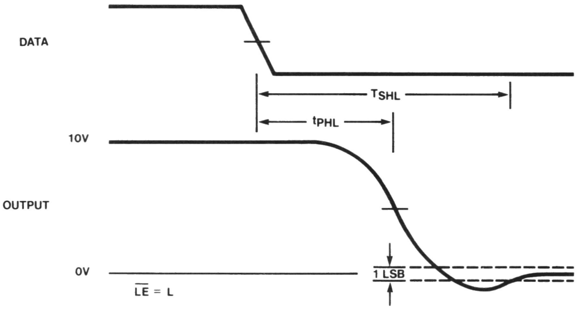

DATA
TSHL
tPHL
10V
OUTPUT
0V
1 LSB
LE = L

Figure 7

PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

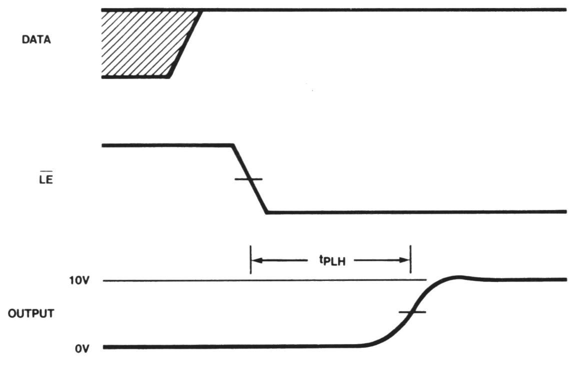

DATA
$\overline{LE}$
t_{PLH}
10V
OUTPUT
0V

Figure 8

PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

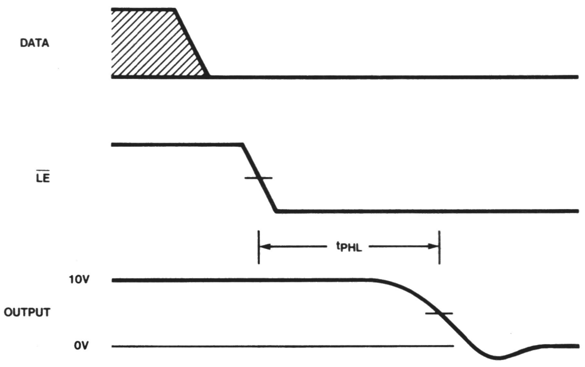

DATA
$\overline{LE}$
t_{PHL}
10V
OUTPUT
0V

Figure 9

LATCH ENABLE PULSE WIDTH, SET-UP AND HOLD TIMES

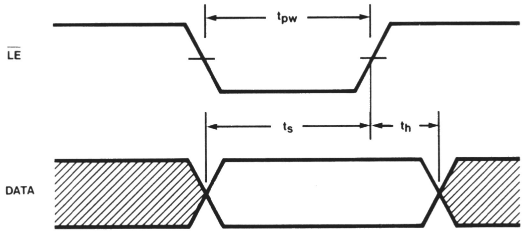

t_{pw}
$\overline{LE}$
t_s
t_h
DATA

Figure 10

8-BIT µP-COMPATIBLE D/A CONVERTER — SE/NE5019

SE/NE5019 F,N

DESCRIPTION

The NE5019 is a complete 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most micro-processors.

The chip also comprises a stable voltage reference (5V nominal) and a high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

FEATURES

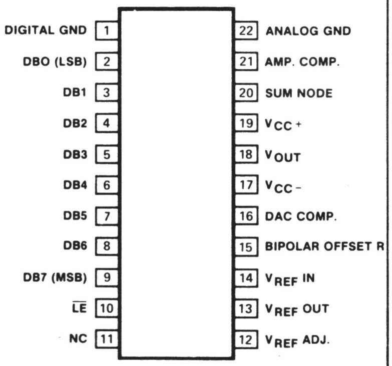
- **8-bit resolution**
- **Input latches**
- **Low-loading data inputs**
- **On-chip voltage reference**
- **Output buffer amplifier**
- **Accurate to ± 1/4 LSB (.1%)**
- **Monotonic to 8 bits**
- **Amplifier and reference both short-circuit protected**
- **Compatible with 2650,8080 and many other µP's**

APPLICATIONS

- **Precision 8-bit D/A converters**
- **A/D converters**
- **Programmable power supplies**
- **Test equipment**
- **Measuring instruments**
- **Analog-digital multiplication**

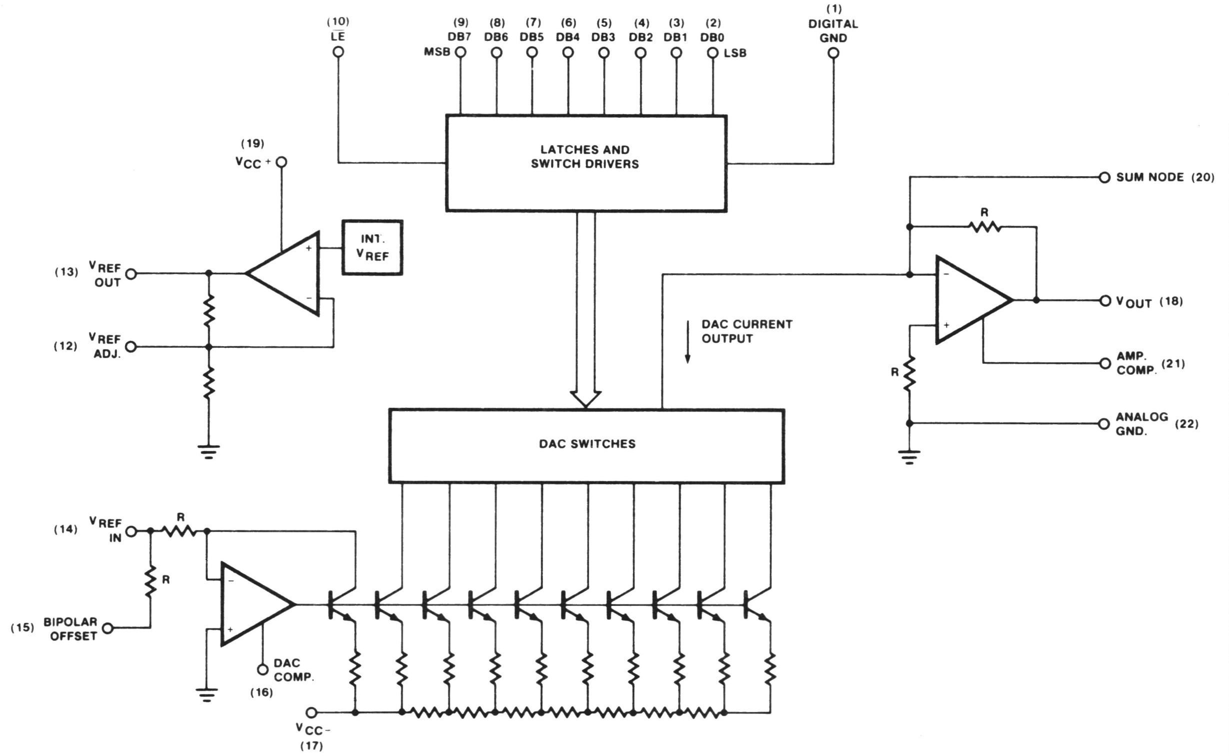
PIN CONFIGURATION

F,N PACKAGE


DIGITAL GND 1
DBO (LSB) 2
DB1 3
DB2 4
DB3 5
DB4 6
DB5 7
DB6 8
DB7 (MSB) 9
$\overline{LE}$ 10
NC 11
22 ANALOG GND
21 AMP. COMP.
20 SUM NODE
19 V_{CC+}
18 V_{OUT}
17 V_{CC-}
16 DAC COMP.
15 BIPOLAR OFFSET R
14 V_{REF} IN
13 V_{REF} OUT
12 V_{REF} ADJ.

SE/NE5019 available in F package only.

BLOCK DIAGRAM


(10) $\overline{LE}$
(9) DB7
(8) DB6
(7) DB5
(6) DB4
(5) DB3
(4) DB2
(3) DB1
(2) DB0
MSB
LSB
(1) DIGITAL GND
LATCHES AND SWITCH DRIVERS
(19) V_{CC+}
INT. V_{REF}
(13) V_{REF} OUT
(12) V_{REF} ADJ.
SUM NODE (20)
R
V_{OUT} (18)
DAC CURRENT OUTPUT
AMP. COMP. (21)
R
ANALOG GND. (22)
DAC SWITCHES
(14) V_{REF} IN
R
R
(15) BIPOLAR OFFSET
DAC COMP. (16)
V_{CC-} (17)

All R values equal 5KΩ and are thermally matched.

Figure 1

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF}IN$	Voltage at V_{REF} input	12	V
$V_{REF}ADJ$	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at V_{REF} OUT	Continuous	
I_{OUTSC}	Short-circuit current to ground or either supply at V_{OUT}	Continuous	
I_{REF}	Reference input current	5	mA
P_D	Power dissipation*		
	-N package	800	mW
	-F package	1000	mW
T_A	Operating temperature range		
	SE5019	−55 to +125	°C
	NE5019	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES
For N package, derate at 120°C/W above 35°C
For F package, derate at 75°C/W above 75°C

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5019. $-55°C \leq T_A \leq 125°C$, NE5019. $0°C \leq T_A \leq 70°C$ unless otherwise specified.[1] Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	SE5019			NE5019			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy				±0.1			±0.1	%FS
$V_{CC}+$	Positive supply voltage		11.4	15		11.4	15		V
$V_{CC}-$	Negative supply voltage		−11.4	−15		−11.4	−15		V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1 = 0V	2.0			2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1 = 0V			0.8			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1 = 0V, $2V<V_{IN}<18V$		0.1	10		0.1	10	μA
$I_{IN(0)}$	Logic "0" input current	Pin 1 = 0V, $-5V<V_{IN}<0.8V$		−2.0	−10		−2.0	−10	μA
V_{FS}	Full scale output voltage	Unipolar operation $V_{REF\ IN} = 5.000V$, $T_A = 25°C$	9.50	9.961	10.50	9.50	9.961	10.50	V
V_{FS}	Full scale output voltage	Bipolar operation $V_{REF\ IN} = 5.000V$, $T_A = 25°C$		+4.961 −5.000			+4.961 −5.000		V
V_{ZS}	Zero scale voltage			5			5		mV
I_{OS}	Output short circuit current	$T_A = 25°C$ $V_{OUT} = 0V$		15	40		15	40	mA
$PSR+_{(out)}$	Output power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01		.001	.01	%FS/%VS
$PSR-_{(out)}$	Output power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq -16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01		.001	.01	%FS/%VS
TC_{FS}	Full scale temperature coefficient	$V_{REF\ IN} = 5.000V$		20			20		ppm/°C
TC_{ZS}	Zero scale temperature coefficient			5			5		ppm/°C

NOTE
1. Refer to Figure 2.

DC ELECTRICAL CHARACTERISTICS (Cont'd) $V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5019. $-55°C \leq T_A \leq 125°C$, NE5019. $0°C \leq T_A \leq 70°C$ unless otherwise specified.[1] Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	SE5019			NE5019			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{REF}	Reference output current	$\Delta V_{REF} \leq 0.1\%$		5			5		mA
I_{REFSC}	Reference short circuit current	$T_A = 25°C$ $V_{REF\ OUT} = 0V$		15			15		mA
$PSR+_{REF}$	Reference power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, $I_{REF} = 1.0mA$		.003	.01		.003	.01	%VR/ %VS
$PSR-_{REF}$	Reference power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq 16.5V$,		.003	.01		.003	.01	%VR/ %VS
V_{REF}	Reference voltage	$I_{REF} = 1.0mA$	4.5	5.0	5.5	4.5	5.0	5.5	V
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$		60			60		ppm/°C
Z_{IN}	DAC $V_{REF}IN$ input impedance	$I_{REF} = 1.0mA$	4.0	5.0	6.0	4.0	5.0	6.0	KΩ
$I_{CC}+$	Positive supply current	$V_{CC}+ = 15V$		7	14		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		−10	−15		−10	−15	mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$		255	435		255	435	mW

NOTE

[1] Refer to Figure 2.

AC ELECTRICAL CHARACTERISTICS[2] $V_{CC} = \pm 15V$, $T_A = 25°C$

PARAMETER		TO	FROM	TEST CONDITIONS	SE/NE5019			UNIT
					Min	Typ	Max	
T_{SLH}	Settling time	± ½ LSB	Input	All bits low to high[3]		1.8		μs
T_{SHL}	Settling time	± ½ LSB	Input	All bits high to low[4]		2.3		μs
t_{plh}	Propagation delay	Output	Input	All bits switched low to high[3]		300		ns
t_{phl}	Propagation delay	Output	Input	All bits switched high to low[4]		150		ns
t_{plsb}	Propagation delay	Output	Input	1 LSB change[3,4]		150		ns
t_{plh}	Propagation delay	Output	$\overline{LE}$	low to high transition[5]		300		ns
t_{phl}	Propagation delay	Output	$\overline{LE}$	high to low transition[6]		150		ns
t_s	Set-up time	$\overline{LE}$	Input	2, 7	100			ns
t_h	Hold time	Input	$\overline{LE}$	2, 7	50			ns
t_{pw}	Latch enable pulse width			2, 7	150			ns
	Reference input Slew rate			2		25		v/μs

NOTES

[2] Refer to Figure 3.

[3] See Figure 6.

[4] See Figure 7.

[5] See Figure 8.

[6] See Figure 9.

[7] See Figure 10.

DC PARAMETRIC TEST CONFIGURATION

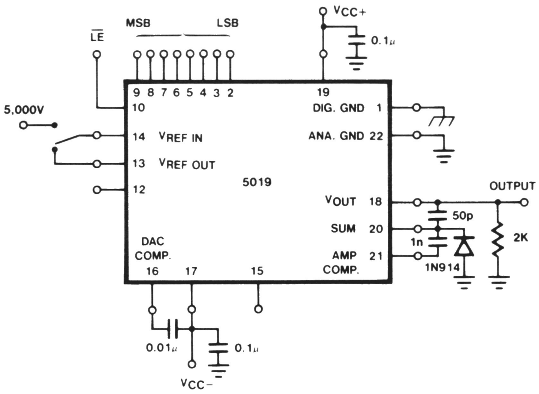

MSB
LSB
LE
VCC+
0.1µ
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
5,000V
14 VREF IN
ANA. GND 22
13 VREF OUT
12
5019
VOUT 18
OUTPUT
SUM 20
50p
1n
2K
DAC COMP.
AMP COMP. 21
1N914
16
17
15
0.01µ
0.1µ
VCC−

Figure 2

AC PARAMETRIC TEST CONFIGUTATION

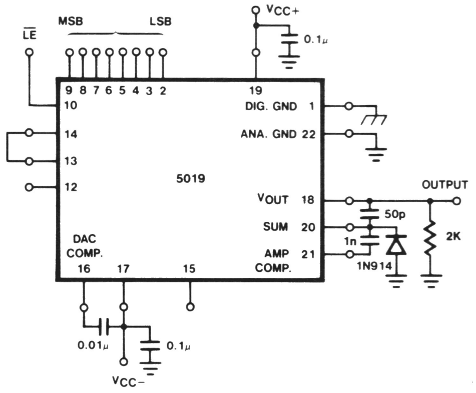

MSB
LSB
LE
VCC+
0.1µ
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
14
ANA. GND 22
13
12
5019
VOUT 18
OUTPUT
SUM 20
50p
1n
2K
DAC COMP.
AMP COMP. 21
1N914
16
17
15
0.01µ
0.1µ
VCC−

Figure 3

FULL/ZERO SCALE ADJUST—UNIPOLAR OUTPUT (0-10V)

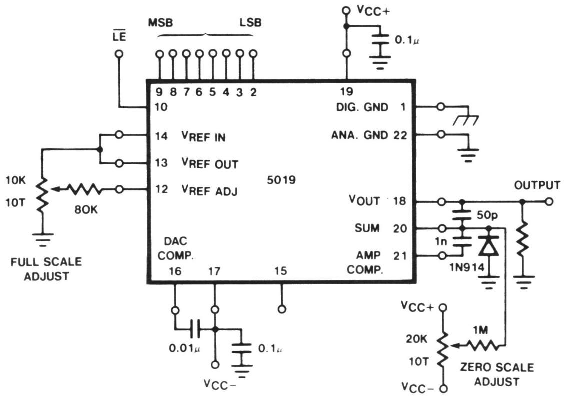

MSB
LSB
LE
VCC+
0.1µ
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
14 VREF IN
ANA. GND 22
13 VREF OUT
10K
10T
80K
12 VREF ADJ
5019
VOUT 18
OUTPUT
SUM 20
50p
1n
FULL SCALE ADJUST
DAC COMP.
AMP COMP. 21
1N914
16
17
15
VCC+
20K
10T
1M
ZERO SCALE ADJUST
VCC−
0.01µ
0.1µ
VCC−

Figure 4

BIPOLAR OUTPUT OPERATION (−5 to +5V)

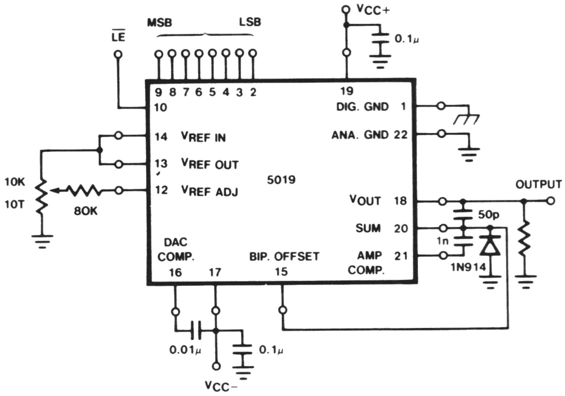

MSB
LSB
LE
VCC+
0.1µ
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
14 VREF IN
ANA. GND 22
13 VREF OUT
10K
10T
80K
12 VREF ADJ
5019
VOUT 18
OUTPUT
SUM 20
50p
1n
DAC COMP.
BIP. OFFSET
AMP COMP. 21
1N914
16
17
15
0.01µ
0.1µ
VCC−

Figure 5

SETTLING TIME AND PROPAGATION DELAY, LOW TO HIGH DATA

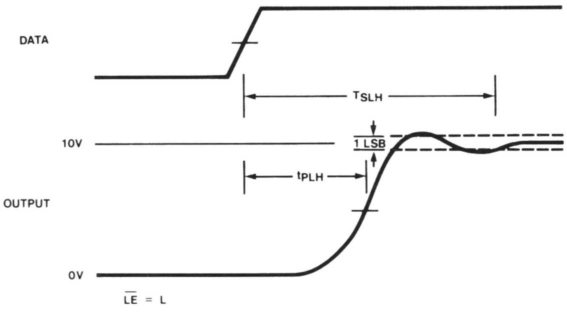

DATA
TSLH
10V
1 LSB
tPLH
OUTPUT
0V
LE = L

Figure 6

SETTLING TIME AND PROPAGATION DELAY, HIGH TO LOW DATA

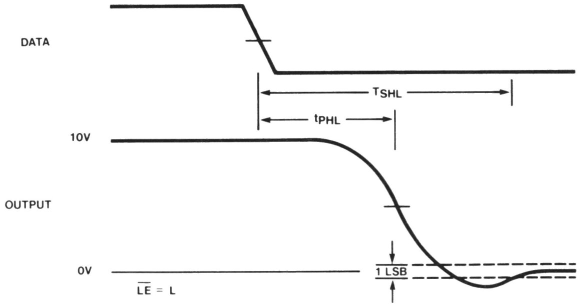

DATA
TSHL
tPHL
10V
OUTPUT
0V
1 LSB
LE = L

Figure 7

PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

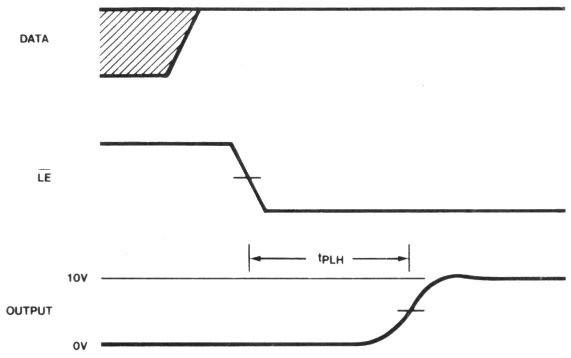

DATA
$\overline{LE}$
t_{PLH}
10V
OUTPUT
0V

Figure 8

PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

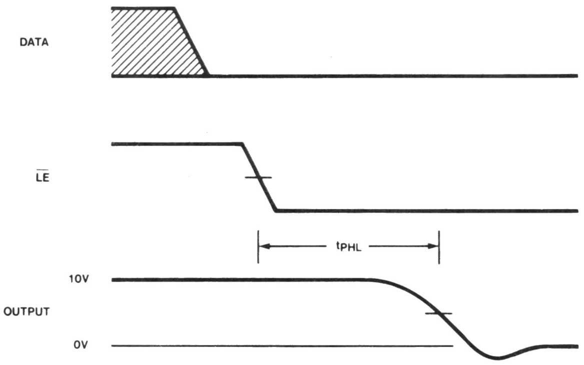

DATA
$\overline{LE}$
t_{PHL}
10V
OUTPUT
0V

Figure 9

LATCH ENABLE PULSE WIDTH, SET-UP AND HOLD TIMES

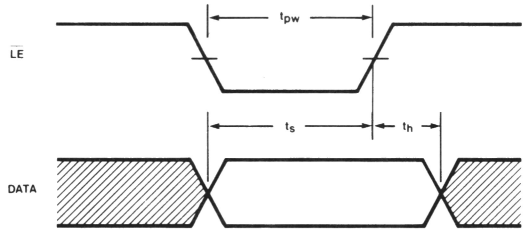

t_{pw}
$\overline{LE}$
t_s
t_h
DATA

Figure 10

8-BIT μP-COMPATIBLE D/A CONVERTER—CURRENT OUTPUT SE/NE5118

SE5118-F • NE5118-N

DESCRIPTION

The NE5118 is a high-speed 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most microprocessors.

The chip also comprises a stable voltage reference (5V nominal). The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output has high voltage compliance increasing versatility.

FEATURES

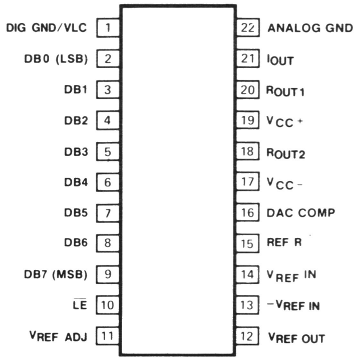
- **8-bit resolution**
- **Input latches**
- **Low-loading data inputs**
- **On-chip voltage reference**
- **Fast settling output current—200ns**
- **Accurate to ±1/2 LSB**
- **Monotonic to 8 bits**
- **Reference short-circuit protected**
- **Compatible with 2650, 8080 and many other μP's**

APPLICATIONS

- **Precision 8-bit D/A converters**
- **A/D converters**
- **Programmable power supplies**
- **Test equipment**
- **Measuring instruments**
- **Analog-digital multiplication**
- **CRT display drivers**
- **High-speed modems**

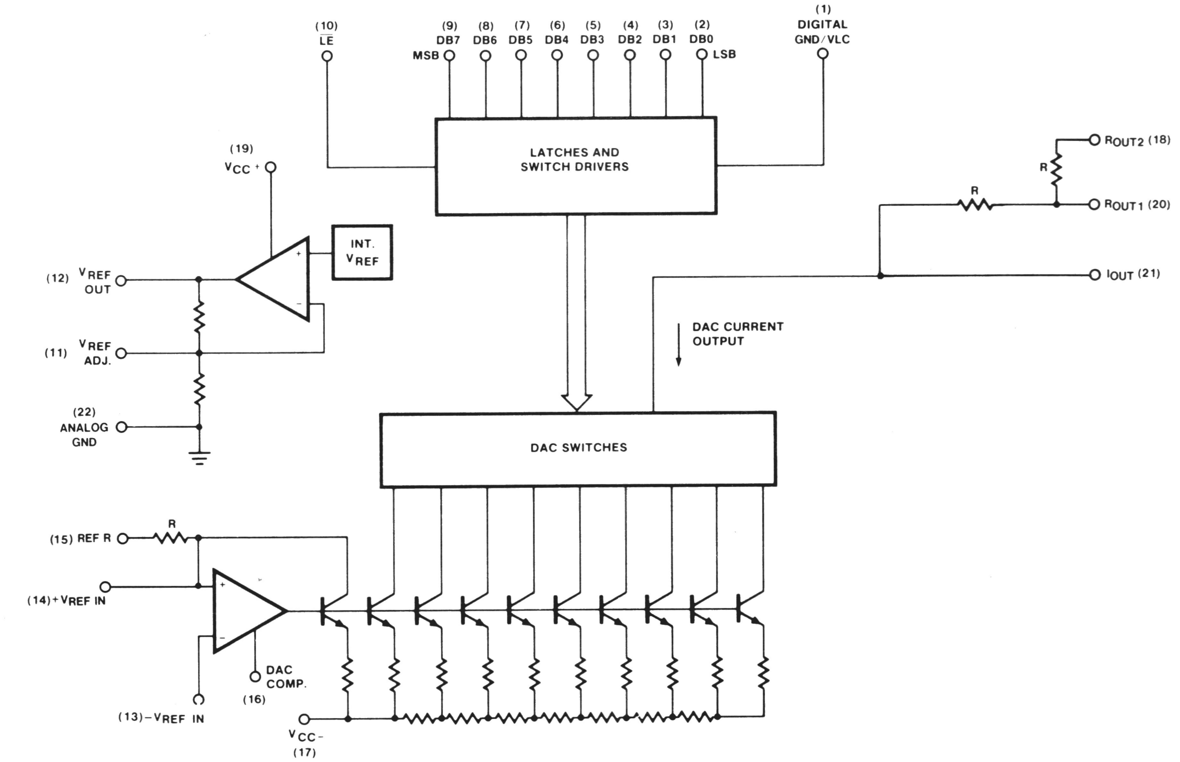
PIN CONFIGURATION

F,N PACKAGE


DIG GND/VLC 1
DB0 (LSB) 2
DB1 3
DB2 4
DB3 5
DB4 6
DB5 7
DB6 8
DB7 (MSB) 9
$\overline{LE}$ 10
VREF ADJ 11
22 ANALOG GND
21 IOUT
20 ROUT1
19 VCC+
18 ROUT2
17 VCC−
16 DAC COMP
15 REF R
14 VREF IN
13 −VREF IN
12 VREF OUT

SE5118 available in F package only.

BLOCK DIAGRAM


(10) $\overline{LE}$
(9) DB7 MSB
(8) DB6
(7) DB5
(6) DB4
(5) DB3
(4) DB2
(3) DB1
(2) DB0 LSB
(1) DIGITAL GND/VLC
LATCHES AND SWITCH DRIVERS
(19) VCC+
INT. VREF
(12) VREF OUT
(11) VREF ADJ.
(22) ANALOG GND
ROUT2 (18)
R
R
ROUT1 (20)
IOUT (21)
DAC CURRENT OUTPUT
DAC SWITCHES
(15) REF R
R
(14)+VREF IN
DAC COMP. (16)
(13)−VREF IN
VCC− (17)

All R values equal 5kΩ and are thermally matched.

Figure 1

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF}IN$	Voltage at R_{REF} input	12	V
$V_{REF}ADJ$	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at V_{REF} OUT	Continuous	
I_{REF}	Reference input current	5	mA
P_D	Power dissipation*		
	-N package	800	mW
	-F package	1000	mW
T_A	Operating temperature range		
	SE5118	−55 to +125	°C
	NE5118	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES

For N package, derate at 120°C/W above 35°C

For F package, derate at 75° C/W above 75°C

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5118. $-55°C \leq T_A \leq 125°C$, NE5118. $0°C \leq T_A \leq 70°C$ unless otherwise specified. Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	SE5118			NE5118			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy				±0.19			±0.19	%FS
$V_{CC}+$	Positive supply voltage		11.4	15		11.4	15		V
$V_{CC}-$	Negative supply voltage		−11.4	−15		−11.4	−15		V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1 = 0V	2.0			2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1 = 0V			0.8			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1 = 0V, $2V < V_{IN} < 18V$		0.1	10		0.1	10	μA
$I_{IN(0)}$	Logic "0" input current	Pin 1 = 0V, $-5V < V_{IN} < 0.8V$		−2.0	−10		−2.0	−10	μA
I_{FS}	Full scale output current	Unipolar operation $V_{REF\ IN} = 5.000V$, $T_A = 25°C$	1.90	1.992	2.10	1.90	1.992	2.10	mA
I_{ZS}	Zero scale current			1			1		μA
V_{REF}	Internal reference voltage	$I_O = 1mA$	4.5	5.0	5.5	4.5	5.0	5.5	V
$PSR+_{(out)}$	Output power supply rejection (+)	$V- = -15V$, $11.4V \leq V+ \leq 16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01		.001	.01	%FS/%VS
$PSR-_{(out)}$	Output power supply rejection (−)	$V+ = 15V$, $-11.4V \leq V- \leq -16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01		.001	.01	%FS/%VS
TC_{FS}	Full scale temperature coefficient	$V_{REF\ IN} = 5.000V$		20			20		ppm/°C
TC_{ZS}	Zero scale temperature coefficient			5			5		ppm/°C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) $V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5118. $-55°C \le T_A \le 125°C$, NE5118. $0°C \le T_A \le 70°C$ unless otherwise specified. Typical values are specified at 25°C

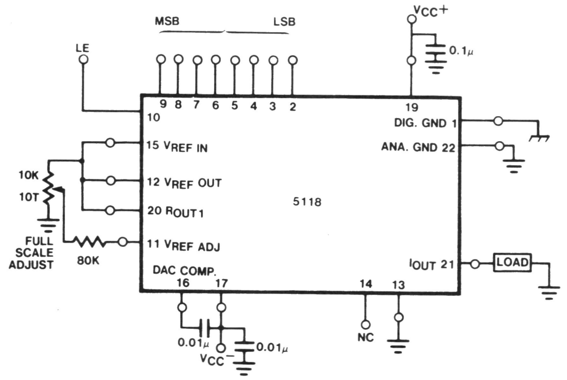
PARAMETER		TEST CONDITIONS	SE5118			NE5118			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{REF}	Reference output current	$\Delta V_{REF} \le 0.1\%$		5			5		mA
I_{REFSC}	Reference short circuit current	$T_A = 25°C$ $V_{REF\ OUT} = 0V$		15	30		15	30	mA
$PSR+_{(REF)}$	Reference power supply rejection (+)	$V- = -15V$, $13.5V \le V+ \le 16.5V$, $I_{REF} = 1.0mA$		.003	.01		.003	.01	%VR/%VS
$PSR-_{(REF)}$	Reference power supply rejection (−)	$V+ = 15V$, $-13.5V \le V- \le 16.5V$, $I_{REF} = 1.0mA$		.003	.01		.003	.01	%VR/%VS
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$		60			60		ppm/°C
Z_{IN}	DAC $R_{REF}IN$ input impedance		4.0	5.0	6.0	4.0	5.0	6.0	kΩ
$I_{CC}+$	Positive supply current	$V_{CC}+ = 15V$		7	14		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		−10	−15		−10	−15	mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$		255	435		255	435	mW

AC ELECTRICAL CHARACTERISTICS

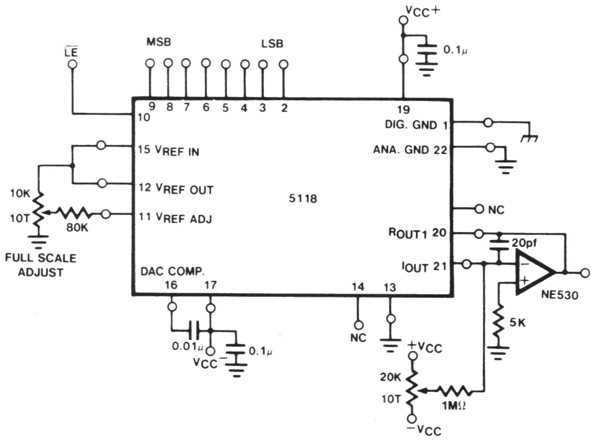
$V_{CC} = \pm 15V$, $T_A = 25°C$

PARAMETER		TO	FROM	TEST CONDITIONS	SE/NE5118			UNIT
					Min	Typ	Max	
T_{SLH}	Settling time	± ½ LSB	Input	All bits Low-to-high		200		ns
T_{SHL}	Settling time	± ½ LSB	Input	All bits High-to-low		200		ns
t_{PLH}	Propagation delay	Output	Input	All bits switched Low-to-high		60		ns
t_{PHL}	Propagation delay	Output	Input	All bits switched High-to-low		60		ns
t_{PLSB}	Propagation delay	Output	Input	1 LSB change		60		ns
t_{PLH}	Propagation delay	Output	$\overline{LE}$	Low-to-high transition		60		ns
t_{PHL}	Propagation delay	Output	$\overline{LE}$	High-to-low transition		60		ns
t_s	Set-up time	$\overline{LE}$	Input		100			ns
t_h	Hold time	Input	$\overline{LE}$		50			ns
t_{pw}	Latch enable pulse width				150			ns
	Reference input Slew rate					5		mA/μs

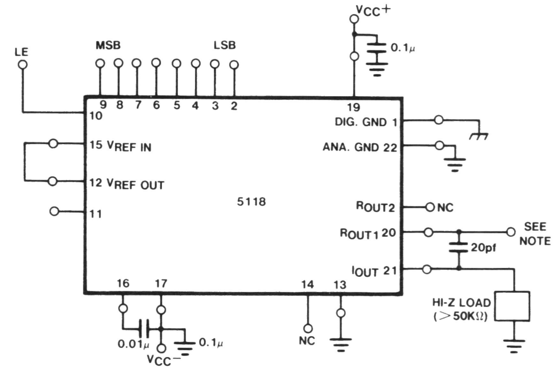
BIPOLAR OUTPUT OPERATION (−1mA TO +1mA)


MSB
LSB
LE
VCC+
0.1μ
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
ANA. GND 22
15 VREF IN
12 VREF OUT
20 ROUT1
11 VREF ADJ
10K
10T
FULL SCALE ADJUST
80K
5118
DAC COMP.
16 17
14 13
IOUT 21
LOAD
0.01μ
0.01μ
VCC−
NC

UNIPOLAR VOLTAGE OUTPUT (0 →+10V)


VCC+
0.1μ
LE
MSB
LSB
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
ANA. GND 22
15 VREF IN
12 VREF OUT
11 VREF ADJ
10K
10T
80K
FULL SCALE ADJUST
5118
NC
ROUT1 20
20pf
IOUT 21
NE530
5K
DAC COMP.
16 17
14 13
0.01μ
0.1μ
VCC−
NC
+VCC
20K
10T
1MΩ
−VCC

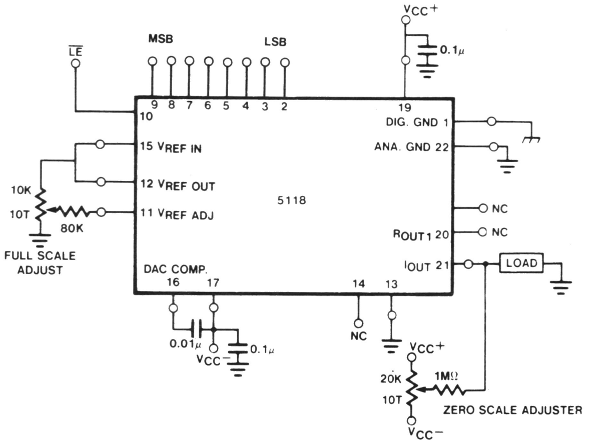
FAST VOLTAGE OUTPUT


VCC+
0.1μ
LE
MSB
LSB
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
ANA. GND 22
15 VREF IN
12 VREF OUT
11
5118
ROUT2
NC
ROUT1 20
SEE NOTE
20pf
IOUT 21
HI-Z LOAD (>50KΩ)
16 17
14 13
0.01μ
0.1μ
VCC−
NC

NOTE

DATA INPUT CODE	VOLTAGE OUTPUT (PIN 21)	
0 0 0 0 0 0 0 0	+10V	0V
1 1 1 1 1 1 1 1	0V	−10V
	Pin 20 tied to +10V	Pin 20 tied to 0V

BASIC UNIPOLAR CURRENT OUTPUT (0 →−2mA)


VCC+
0.1μ
LE
MSB
LSB
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
ANA. GND 22
15 VREF IN
12 VREF OUT
11 VREF ADJ
10K
10T
80K
FULL SCALE ADJUST
5118
NC
ROUT1 20
NC
IOUT 21
LOAD
DAC COMP.
16 17
14 13
0.01μ
0.1μ
VCC−
NC
VCC+
20K
10T
1MΩ
ZERO SCALE ADJUSTER
VCC−

8-BIT μP-COMPATIBLE D/A CONVERTER—CURRENT OUTPUT SE/NE5119

SE5119-F • NE5119-N

DESCRIPTION

The NE5119 is a high-speed 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most microprocessors.

The chip also comprises a stable voltage reference (5V nominal). The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output has high voltage compliance increasing versatility.

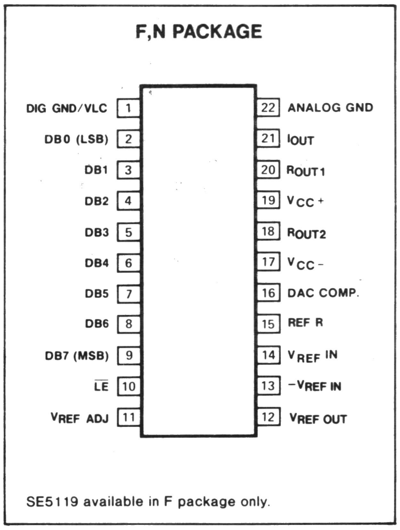
FEATURES

- **8-bit resolution**
- **Input latches**
- **Low-loading data inputs**
- **On-chip voltage reference**
- **Fast settling output current—200ns**
- **Accurate to ± 1/4 LSB**
- **Monotonic to 8 bits**
- **Reference short-circuit protected**
- **Compatible with 2650, 8080 and many other μP's**

APPLICATIONS

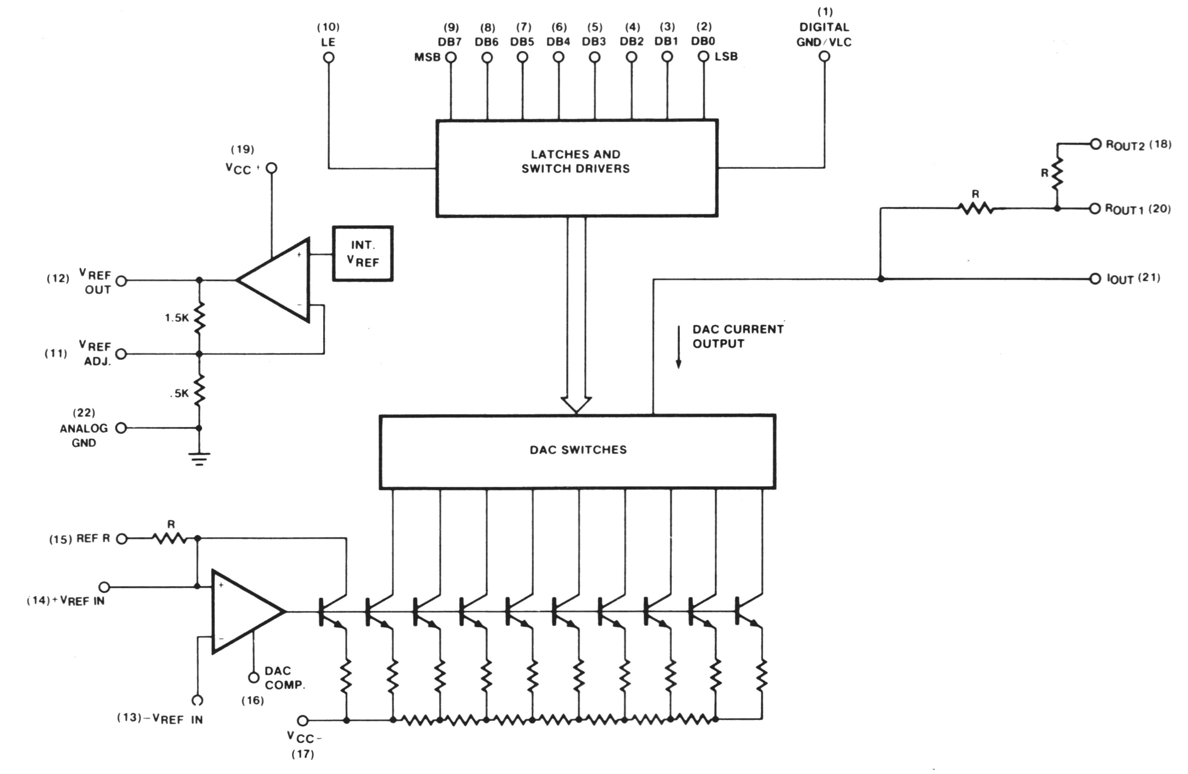
- **Precision 8-bit D/A converters**
- **A/D converters**
- **Programmable power supplies**
- **Test equipment**
- **Measuring instruments**
- **Analog-digital multiplication**
- **CRT display drivers**
- **High-speed modems**

PIN CONFIGURATION


F,N PACKAGE
DIG GND/VLC 1
DB0 (LSB) 2
DB1 3
DB2 4
DB3 5
DB4 6
DB5 7
DB6 8
DB7 (MSB) 9
LE 10
VREF ADJ 11
22 ANALOG GND
21 IOUT
20 ROUT1
19 VCC+
18 ROUT2
17 VCC-
16 DAC COMP.
15 REF R
14 VREF IN
13 -VREF IN
12 VREF OUT

SE5119 available in F package only.

BLOCK DIAGRAM


(10) LE
(9) DB7
(8) DB6
(7) DB5
(6) DB4
(5) DB3
(4) DB2
(3) DB1
(2) DB0
MSB
LSB
(1) DIGITAL GND/VLC
LATCHES AND SWITCH DRIVERS
(19) VCC+
INT. VREF
(12) VREF OUT
1.5K
(11) VREF ADJ.
.5K
(22) ANALOG GND
ROUT2 (18)
R
R
ROUT1 (20)
IOUT (21)
DAC CURRENT OUTPUT
DAC SWITCHES
R
(15) REF R
(14)+VREF IN
DAC COMP.
(16)
(13)-VREF IN
VCC-
(17)

All R values equal 5kΩ and are thermally matched.

Figure 1

SE5119-F • NE5119-N

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF}IN$	Voltage at R_{REF} input	12	V
$V_{REF}ADJ$	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at V_{REF} OUT	Continuous	
I_{REF}	Reference input current	5	mA
P_D	Power dissipation*		
	-N package	800	mW
	-F package	1000	mW
T_A	Operating temperature range		
	SE5119	−55 to +125	°C
	NE5119	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES

For N package, derate at 120°C/W above 35°C

For F package, derate at 75° C/W above 75°C

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5119. $-55°C \leq T_A \leq 125°C$, NE5119. $0°C \leq T_A \leq 70°C$ unless otherwise specified. Typical values are specified at 25°C

	PARAMETER	TEST CONDITIONS	SE5119			NE5119			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy				±0.1			±0.1	%FS
$V_{CC}+$	Positive supply voltage		11.4	15		11.4	15		V
$V_{CC}-$	Negative supply voltage		−11.4	−15		−11.4	−15		V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1 = 0V	2.0			2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1 = 0V			0.8			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1 = 0V, $2V<V_{IN}<18V$		0.1	10		0.1	10	μA
$I_{IN(0)}$	Logic "0" input current	Pin 1 = 0V, $-5V<V_{IN}<0.8V$		−2.0	−10		−2.0	−10	μA
I_{FS}	Full scale output current	Unipolar operation $V_{REF\ IN} = 5.000V$, $T_A = 25°C$	1.90	1.992	2.10	1.90	1.992	2.10	mA
I_{ZS}	Zero scale current			1			1		μA
V_{REF}	Internal reference voltage	$I_O = 1mA$	4.5	5.0	5.5	4.5	5.0	5.5	V
PSR+(out)	Output power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01		.001	.01	%FS/%VS
PSR−(out)	Output power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq -16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01		.001	.01	%FS/%VS
TC_{FS}	Full scale temperature coefficient	$V_{REF\ IN} = 5.000V$		20			20		ppm/°C
TC_{ZS}	Zero scale temperature coefficient			5			5		ppm/°C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) $V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5119. $-55°C \leq T_A \leq 125°C$, NE5119. $0°C \leq T_A \leq 70°C$ unless otherwise specified. Typical values are specified at 25°C

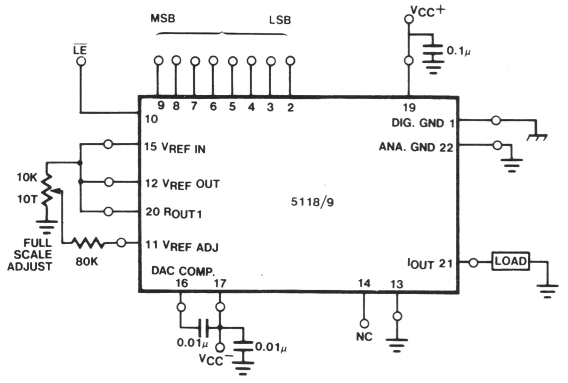
PARAMETER		TEST CONDITIONS	SE5119			NE5119			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{REF}	Reference output current	$\Delta V_{REF} \leq 0.1\%$		5			5		mA
I_{REFSC}	Reference short circuit current	$T_A = 25°C$ $V_{REF\ OUT} = 0V$		15	30		15	30	mA
$PSR+_{(REF)}$	Reference power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, $I_{REF} = 1.0mA$		.003	.01		.003	.01	%VR/ %VS
$PSR-_{(REF)}$	Reference power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq 16.5V$, $I_{REF} = 1.0mA$		.003	.01		.003	.01	%VR/ %VS
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$		60			60		ppm/°C
Z_{IN}	DAC $R_{REF}IN$ input impedance		4.0	5.0	6.0	4.0	5.0	6.0	kΩ
$I_{CC}+$	Positive supply current	$V_{CC}+ = 15V$		7	14		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		−10	−15		−10	−15	mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$		255	435		255	435	mW

AC ELECTRICAL CHARACTERISTICS

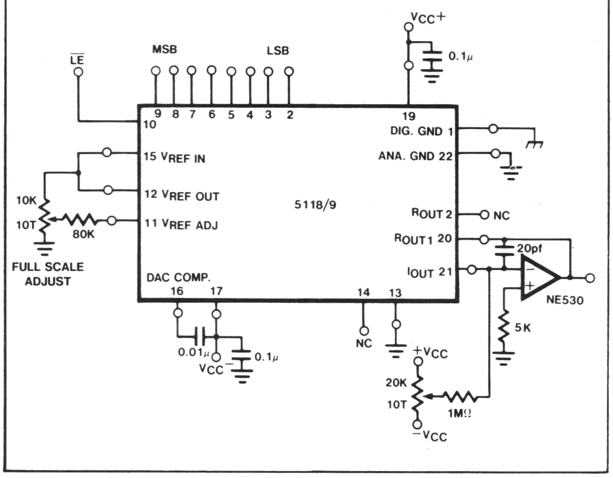
$V_{CC} = \pm 15V$, $T_A = 25°C$

PARAMETER		TO	FROM	TEST CONDITIONS	SE/NE5119			UNIT
					Min	Typ	Max	
T_{SLH}	Settling time	± ½ LSB	Input	All bits Low-to-high		200		ns
T_{SHL}	Settling time	± ½ LSB	Input	All bits High-to-low		200		ns
t_{PLH}	Propagation delay	Output	Input	All bits switched Low-to-high		60		ns
t_{PHL}	Propagation delay	Output	Input	All bits switched High-to-low		60		ns
t_{PLSB}	Propagation delay	Output	Input	1 LSB change		60		ns
t_{PLH}	Propagation delay	Output	$\overline{LE}$	Low-to-high transition		60		ns
t_{PHL}	Propagation delay	Output	$\overline{LE}$	High-to-low transition		60		ns
t_s	Set-up time	$\overline{LE}$	Input		100			ns
t_h	Hold time	Input	$\overline{LE}$		50			ns
t_{pw}	Latch enable pulse width				150			ns
	Reference input Slew rate					5		mA/μs

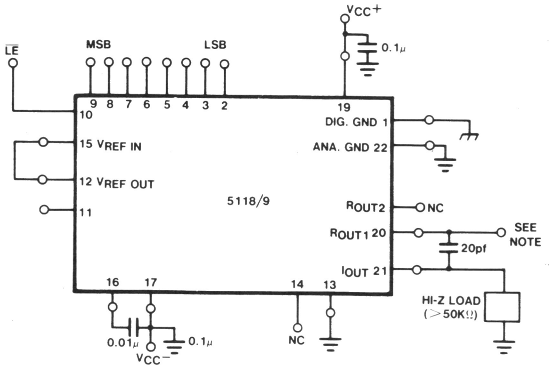
BIPOLAR OUTPUT OPERATION (−1mA TO +1mA)


MSB
LSB
$V_{CC}+$
0.1μ
LE
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
ANA. GND 22
15 V_{REF} IN
12 V_{REF} OUT
20 R_{OUT1}
11 V_{REF} ADJ
5118/9
10K
10T
FULL SCALE ADJUST
80K
DAC COMP.
16 17
14 13
I_{OUT} 21
LOAD
0.01μ
$V_{CC}-$
0.01μ
NC

UNIPOLAR VOLTAGE OUTPUT (0 →+10V)


$V_{CC}+$
0.1μ
MSB
LSB
LE
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
ANA. GND 22
15 V_{REF} IN
12 V_{REF} OUT
11 V_{REF} ADJ
5118/9
R_{OUT2}
NC
R_{OUT1} 20
I_{OUT} 21
20pf
NE530
5K
10K
10T
80K
FULL SCALE ADJUST
DAC COMP.
16 17
14 13
0.01μ
$V_{CC}-$
0.1μ
NC
$+V_{CC}$
20K
10T
1MΩ
$-V_{CC}$

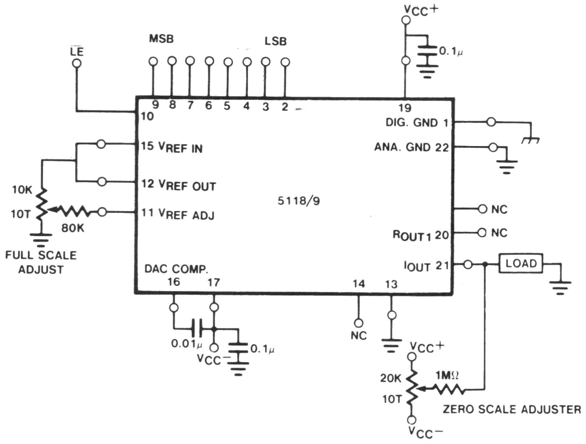
FAST VOLTAGE OUTPUT


$V_{CC}+$
0.1μ
LE
MSB
LSB
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
ANA. GND 22
15 V_{REF} IN
12 V_{REF} OUT
11
5118/9
R_{OUT2}
NC
R_{OUT1} 20
SEE NOTE
20pf
I_{OUT} 21
HI-Z LOAD (>50KΩ)
16 17
14 13
0.01μ
$V_{CC}-$
0.1μ
NC

NOTE

DATA INPUT CODE	VOLTAGE OUTPUT (PIN 21)	
0 0 0 0 0 0 0 0	+10V	0V
1 1 1 1 1 1 1 1	0V	−10V
	Pin 20 tied to +10V	Pin 20 tied to 0V

BASIC UNIPOLAR CURRENT OUTPUT (0 →−2mA)


$V_{CC}+$
0.1μ
MSB
LSB
LE
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
ANA. GND 22
15 V_{REF} IN
12 V_{REF} OUT
11 V_{REF} ADJ
5118/9
10K
10T
80K
FULL SCALE ADJUST
NC
NC
R_{OUT1} 20
I_{OUT} 21
LOAD
DAC COMP.
16 17
14 13
0.01μ
$V_{CC}-$
0.1μ
NC
$V_{CC}+$
20K
10T
1MΩ
ZERO SCALE ADJUSTER
$V_{CC}-$

SECTION II
AUDIO/RADIO CIRCUITS

Section 11—AUDIO/RADIO CIRCUITS

NE/SE540	Power Driver	251
NE542	Dual Low-Noise Preamp	256
NE570	Compandor	259
NE571	Compandor	259
N5596	Balanced Modulator-Demodulator	*
CA3089	FM IF System	*
LM387	Dual Low-Noise Preamp	261
MC1496	Balanced Modulator-Demodulator	*
MC1596	Balanced Modulator-Demodulator	*
TCA440	AM Receiver Circuit	265
μA758	FM Stereo Multiplex Decoder, Phase Locked Loop	*
NE545	Dolby-B Noise Processor	*
NE645B	Dolby-B Type Noise Reduction Circuit	*
ULN2209	FM Gain Block	*
ULN2231	Dual Audio Preamplifier	*

NOTE

*Any product listed in this section but not incorporated within the text may be obtained by writing Information Services at Signetics, 811 E. Arques, M/S 027, Sunnyvale, California 94086, or by calling (408) 746-1682.

POWER DRIVER NE/SE540

NE/SE540-H

DESCRIPTION

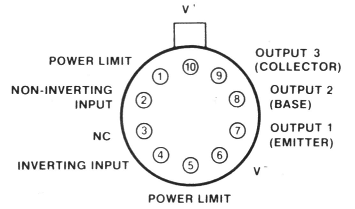
The NE/SE540 is a monolithic, class AB power amplifier designed specifically to drive a pair of complementary output transistors. The device features low standby current yet retains a high output current drive capability with internal current limiting. A wide power bandwidth and excellent linearity make this device ideal for use an audio power amplifier.

FEATURES

- **Internal current limiting**
- **Low standby current**
- **High output current capability**
- **Wide power bandwidth**
- **Low distortion**

PIN CONFIGURATION

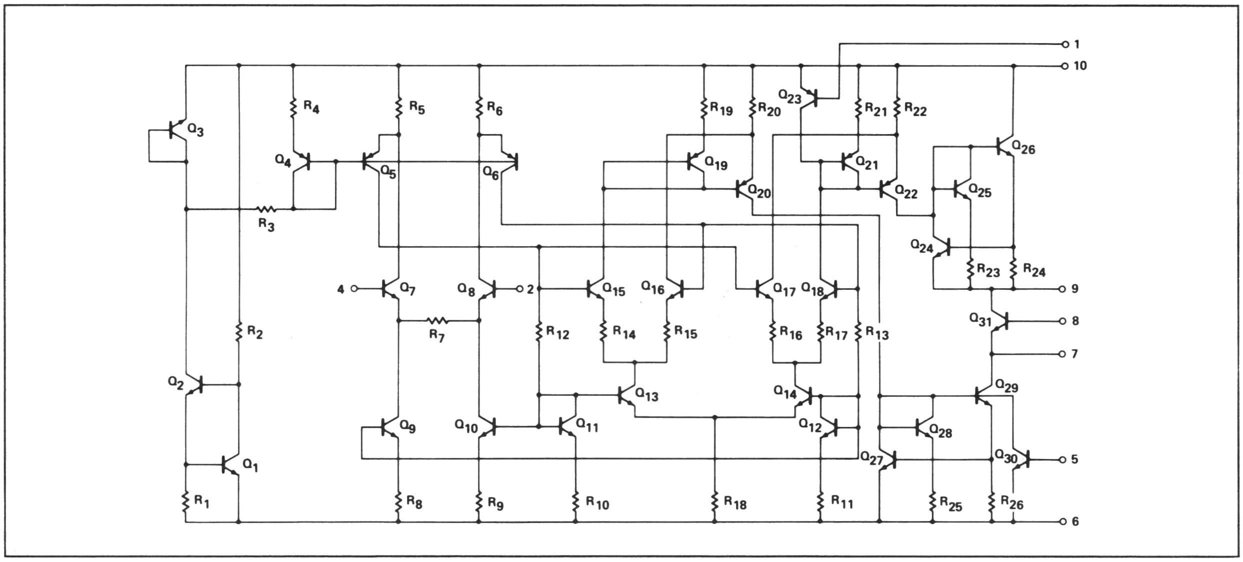
H PACKAGE



V+
POWER LIMIT
NON-INVERTING INPUT
NC
INVERTING INPUT
POWER LIMIT
OUTPUT 3 (COLLECTOR)
OUTPUT 2 (BASE)
OUTPUT 1 (EMITTER)
V−
①
②
③
④
⑤
⑥
⑦
⑧
⑨
⑩

ORDER PART NO.
NE540H, SE540H

EQUIVALENT SCHEMATIC



1
10
9
8
7
5
6
4
2
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q26
Q27
Q28
Q29
Q30
Q31
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
SE540	±27	V
NE540	±22	V
Operating temperature range		
SE540	-55 to +125	°C
NE540	0 to +70	°C
Storage temperature range	-65 to +150	°C
Output short circuit duration (Not exceeding maximum dissipation.)	Indefinite	

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ and $V_{CC} = ±20V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE540			NE540			UNIT
		Min	Typ	Max	Min	Typ	Max	
Operating supply voltage		±5		±25	±5		±20	V
Quiescent current			13	20		13	20	mA
Input offset voltage			5	7		7	10	mV
Input offset current			0.3	0.7		0.5	1	μA
Input bias current			1.5	3		2	5	μA
Input impedance			20			20		kΩ
Current gain		80	100		70	90		dB
Gain variation over temperature range	40dB gain		±0.1			±0.1		dB
Power supply rejection ratio	40dB gain	80	90		60	80		dB
Common mode rejection ratio			110			90		dB
Output drive current		±120	±150		±80	±100		mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ and $V_{CC} = ±20V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE540			NE540			UNIT
		Min	Typ	Max	Min	Typ	Max	
Frequency response	40dB gain ±1dB		500			100		kHz
Distortion	40dB gain, Output 3dB below clipping $R_L = 600Ω$		0.25	0.5		0.5	1.0	%
	$R_L = 2kΩ$		0.06			0.06		
Equivalent input noise voltage	$R_S = 600Ω$ 50Hz to 500kHz		10			10		μV
Slew rate	$V_{CC} = ±20V$ $V_{OUT} = ±15V$		200			200		V/μs

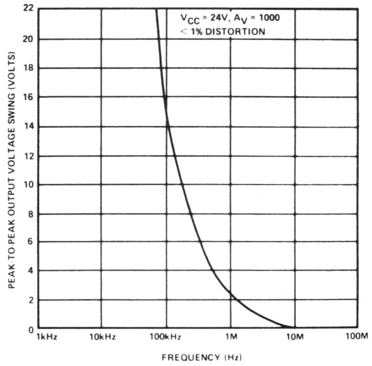
NE542-N

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 14V$ unless otherwise specified.

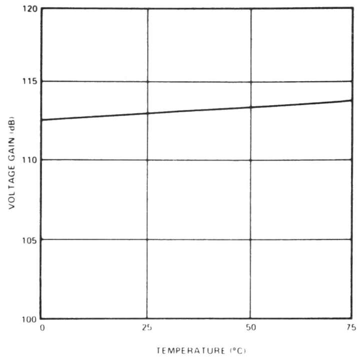
PARAMETER	TEST CONDITIONS	NE542			UNIT
		Min	Typ	Max	
Voltage gain	Open loop		160,000		V/V
Input current Negative input			.5		μA
Output current	Source Sink (linear operation)	8 2	14 3		mA mA
Output voltage swing		V_{CC} -2.5	V_{CC} -2		V
Small signal bandwidth			15		MHz
Slew rate			5		V/μs
Power bandwidth	15V p-p		100		kHz
Maximum input voltage	Linear operation			300	mVrms
Supply rejection ratio	f=60, 120Hz f = 1kHz		100 110		dB dB
Channel separation	f = 1kHz		70		dB
Total harmonic distortion	75dB gain, f = 1kHz		.1		%
Total equivalent input Noise	RS = 600Ω, 100 - 10,000Hz		.7	1.2	μVrms
Noise figure	RS = 50kΩ, 10 - 10,000Hz RS = 20kΩ, 10 10,000Hz RS = 10kΩ, 10 - 10,000Hz RS = 5kΩ, 10 - 10,000Hz		1.2 1.2 1.5 2.4		dB dB dB dB

TYPICAL PERFORMANCE CHARACTERISTICS

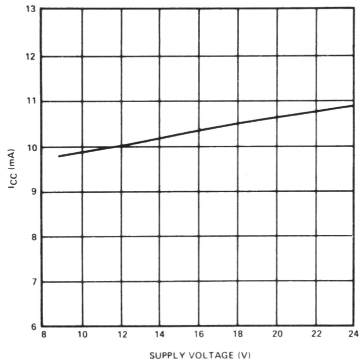
LARGE SIGNAL FREQUENCY RESPONSE



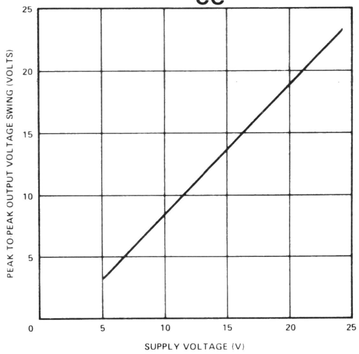
GAIN vs TEMPERATURE



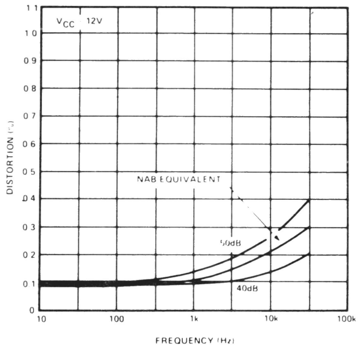
V_{CC} vs I_{CC}



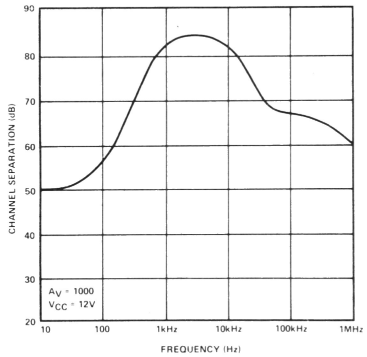
P-P OUTPUT VOLTAGE SWING vs V_{CC}



% DISTORTION

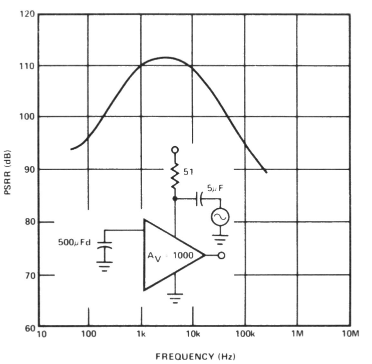


CHANNEL SEPARATION

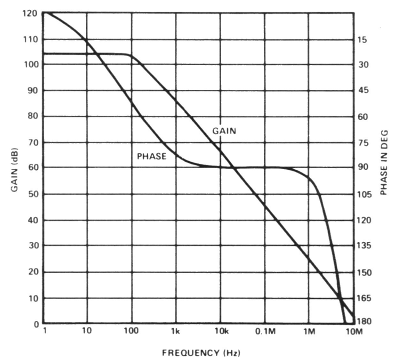


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

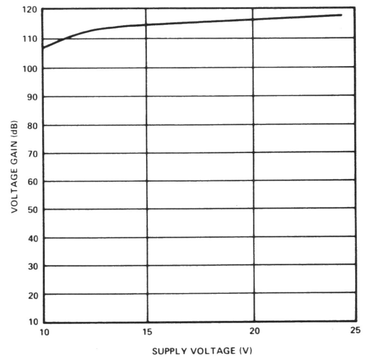
PSRR vs FREQUENCY



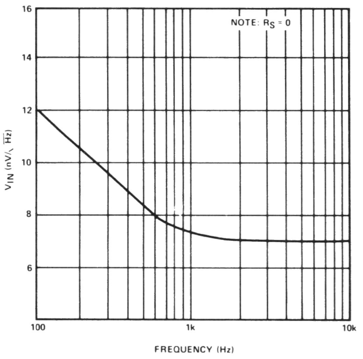
GAIN AND PHASE RESPONSE



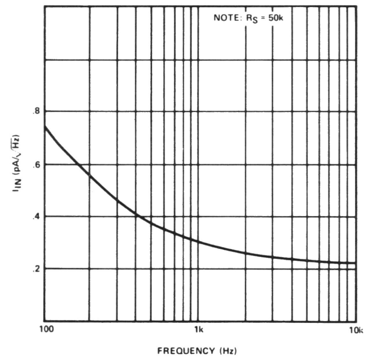
VOLTAGE GAIN vs SUPPLY VOLTAGE



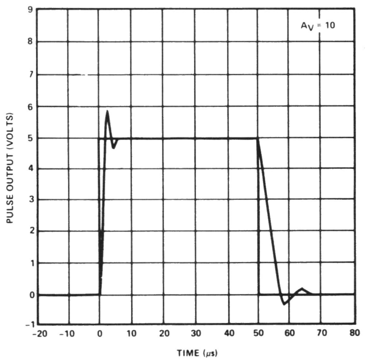
NOISE VOLTAGE vs FREQUENCY



NOISE CURRENT vs FREQUENCY

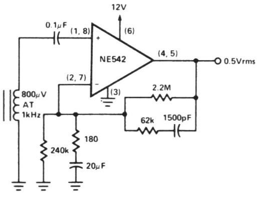


PULSE RESPONSE

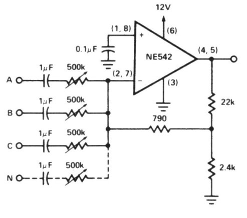


TYPICAL APPLICATIONS

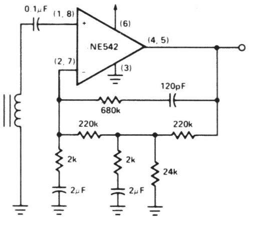
TYPICAL TAPE PLAYBACK AMPLIFIER


12V
0.1µF
(1, 8)
(6)
NE542
(4, 5)
0.5Vrms
(2, 7)
(3)
2.2M
800µV
AT
1kHz
62k
1500pF
180
240k
20µF

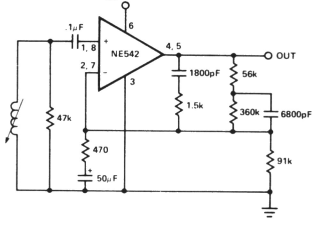
AUDIO MIXER


12V
(1, 8)
(6)
0.1µF
NE542
(4, 5)
1µF
500k
(2, 7)
(3)
A
B
C
N
22k
790
2.4k

TWO-POLE FAST TURN-ON NAB TAPE PREAMP


12V
0.1µF
(1, 8)
(6)
NE542
(4, 5)
(2, 7)
(3)
120pF
680k
220k
220k
2k
2k
24k
2µF
2µF

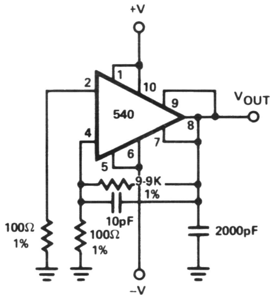
R1AA MAGNETIC PHONO PREAMP


VCC = +16V
6
.1µF
1, 8
NE542
4, 5
OUT
2, 7
3
1800pF
56k
1.5k
360k
6800pF
47k
470
50µF
91k

NOTE: All resistors values are typical and in ohms.

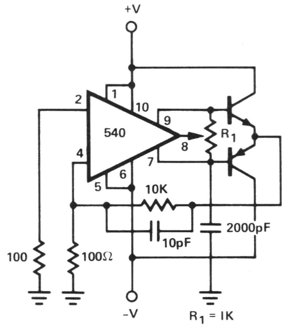
TEST CIRCUITS

OFFSET VOLTAGE MEASUREMENT


+V
540
1
2
10
9
8
7
4
6
5
VOUT
9.9K 1%
10pF
100Ω 1%
100Ω 1%
2000pF
−V

$V_{OFFSET} = \frac{V_{OUT}}{100}$

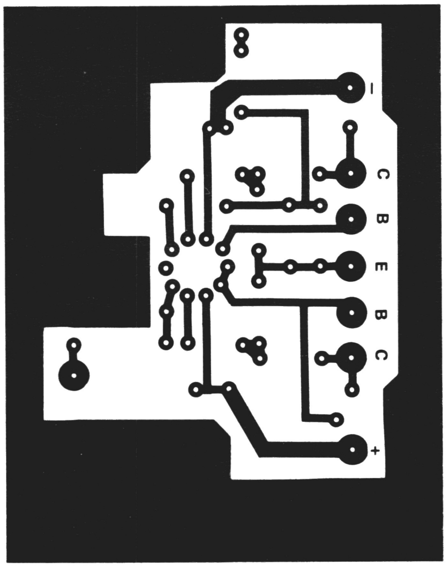
OUTPUT BIAS CONTROL


+V
540
1
2
10
9
8
7
4
6
5
R1
10K
10pF
2000pF
100
100Ω
−V
R1 = IK

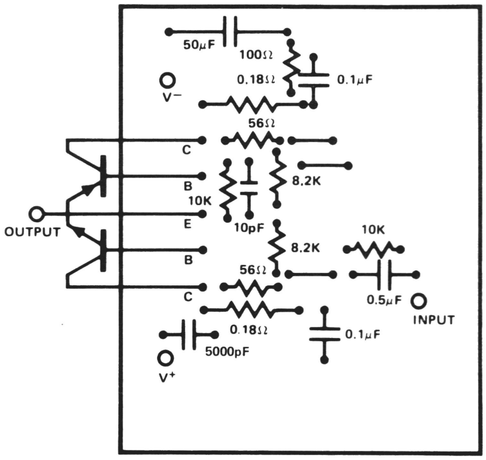
BIAS CONTROL FOR OUTPUT TRANSISTORS

35 WATT AMPLIFIER

P.C. BOARD LAYOUT (Bottom View)



PARTS LAYOUT (Top View)


50μF
100Ω
0.18Ω
0.1μF
V−
56Ω
C
B
10K
10pF
8.2K
E
OUTPUT
8.2K
10K
B
56Ω
C
0.5μF
INPUT
0.18Ω
0.1μF
5000pF
V+

DUAL LOW-NOISE PREAMP

NE542

NE542-N

DESCRIPTION

The NE542 is a dual preamplifier for the amplification of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with individual internal power supply decoupler-regulator, providing 110dB supply rejection and 70dB channel separation. Other outstanding features include high gain (104dB), large output voltage swing (V_{CC} -2Vp-p), and internal compensation to 10dB. The NE542 operates from a single supply across the wide range of 9 to 24V.

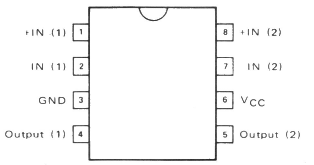
The NE542 is ideal for use in stereo phono, tape, or microphone preamps and other applications requiring low noise amplication of small signals.

FEATURES

- **Low noise—.7μV total input noise**
- **High gain—104dB open loop**
- **Single supply operation**
- **Wide supply range 9 to 24V**
- **Power supply rejection 110dB**
- **Large output voltage swing (V_{CC} -2V p-p)**
- **Wide bandwidth 15MHz unity gain**
- **Power bandwidth 100kHz (15V p-p)**
- **Internally compensated (stable at 10dB)**
- **Short circuit protected**
- **High slew rate 5V/μs**

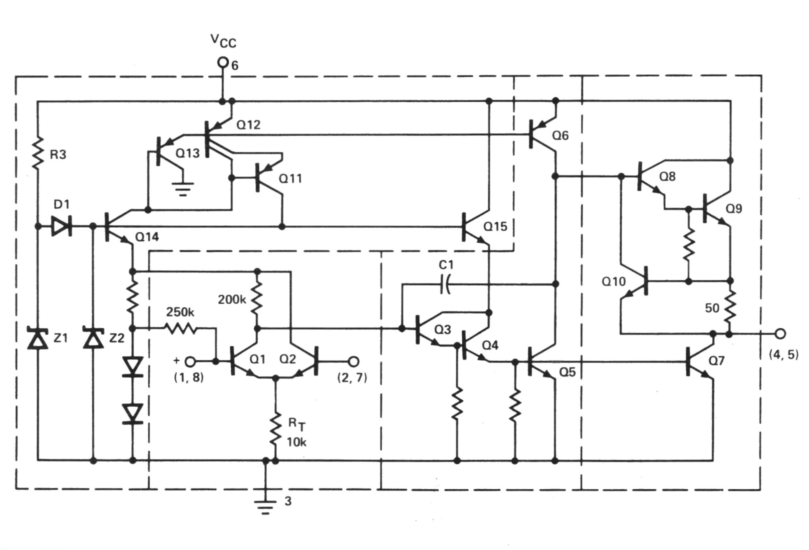
PIN CONFIGURATION

N PACKAGE



ORDER NO.
NE542N

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	+24	V
Power dissipation	500	mW
Operating temperature range	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	+300	°C

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = 14V$ unless otherwise specified.

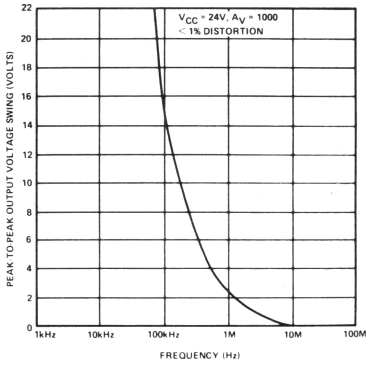
PARAMETER	TEST CONDITIONS	NE542			UNIT
		Min	Typ	Max	
Supply voltage		9		24	V
Supply current	V_{CC} = 9 to 18V, $R_L = \infty$		9	15	mA
Input resistance					
Positive input			100		kΩ
Negative input			200		kΩ
Output resistance	Open loop		150		Ω

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 14V$ unless otherwise specified.

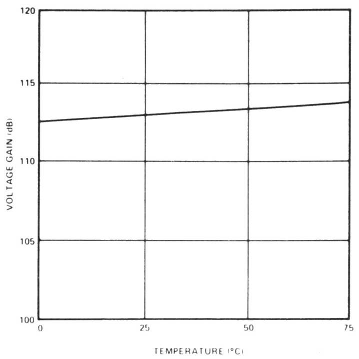
PARAMETER	TEST CONDITIONS	NE542			UNIT
		Min	Typ	Max	
Voltage gain	Open loop		160,000		V/V
Input current Negative input			.5		μA
Output current	Source	8	14		mA
	Sink (linear operation)	2	3		mA
Output voltage swing		V_{CC} -2.5	V_{CC} -2		V
Small signal bandwidth			15		MHz
Slew rate			5		V/μs
Power bandwidth	15V p-p		100		kHz
Maximum input voltage	Linear operation			300	mVrms
Supply rejection ratio	f = 60, 120Hz		100		dB
	f = 1kHz		110		dB
Channel separation	f = 1kHz		70		dB
Total harmonic distortion	75dB gain, f = 1kHz		.1		%
Total equivalent input Noise	RS = 600Ω, 100 - 10,000Hz		.7	1.2	μVrms
Noise figure	RS = 50kΩ, 10 - 10,000Hz		1.2		dB
	RS = 20kΩ, 10 10,000Hz		1.2		dB
	RS = 10kΩ, 10 - 10,000Hz		1.5		dB
	RS = 5kΩ, 10 - 10,000Hz		2.4		dB

TYPICAL PERFORMANCE CHARACTERISTICS

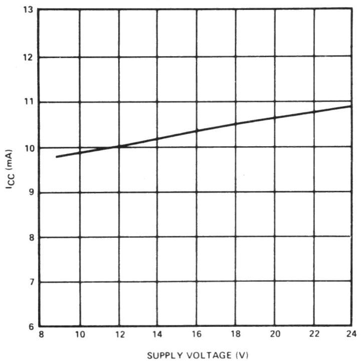
LARGE SIGNAL FREQUENCY RESPONSE



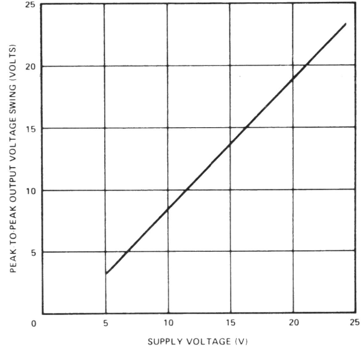
GAIN vs TEMPERATURE



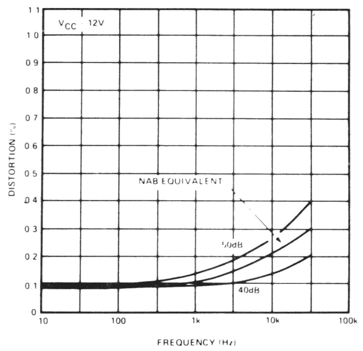
V_{CC} vs I_{CC}



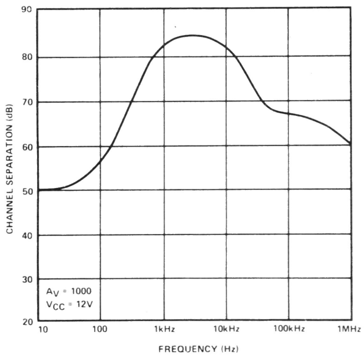
P-P OUTPUT VOLTAGE SWING vs V_{CC}



% DISTORTION

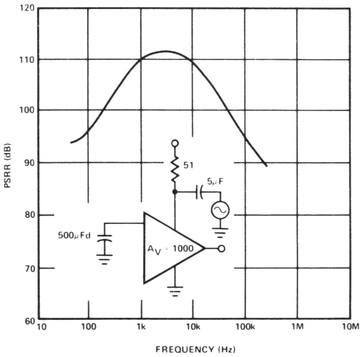


CHANNEL SEPARATION

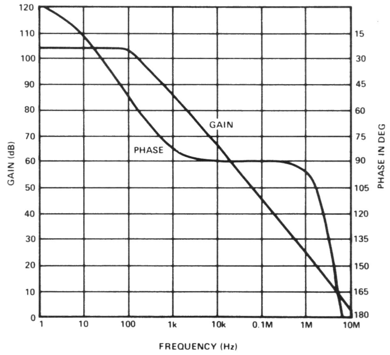


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

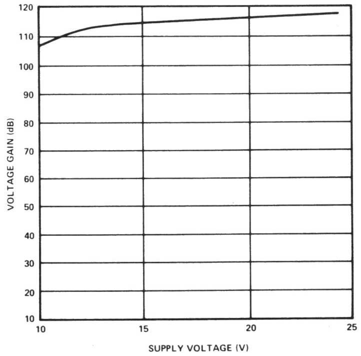
PSRR vs FREQUENCY



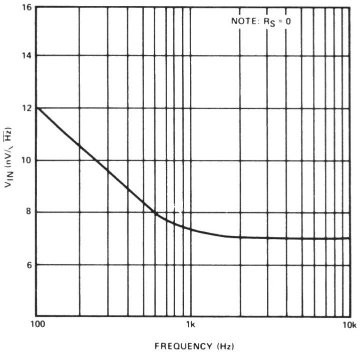
GAIN AND PHASE RESPONSE



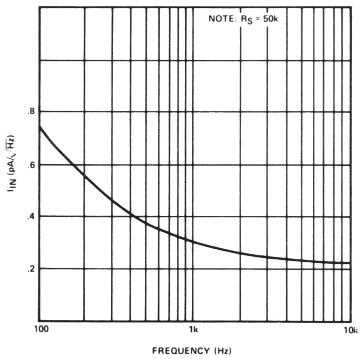
VOLTAGE GAIN vs SUPPLY VOLTAGE



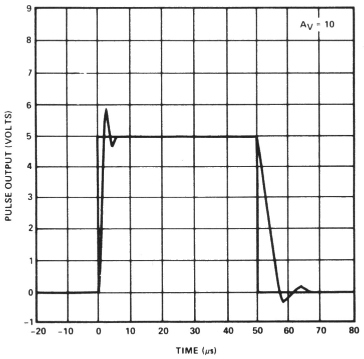
NOISE VOLTAGE vs FREQUENCY



NOISE CURRENT vs FREQUENCY

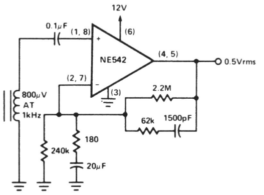


PULSE RESPONSE

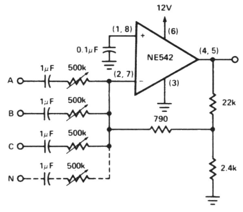


TYPICAL APPLICATIONS

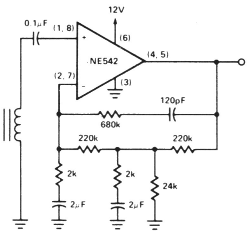
TYPICAL TAPE PLAYBACK AMPLIFIER


12V
0.1μF
(1, 8)
(6)
NE542
(4, 5)
0.5Vrms
(2, 7)
(3)
2.2M
800μV
AT
1kHz
62k
1500pF
180
240k
20μF

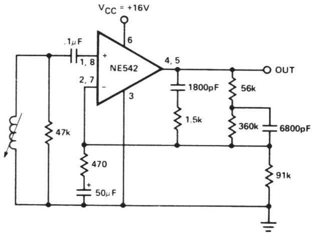
AUDIO MIXER


12V
(1, 8)
(6)
0.1μF
NE542
(4, 5)
(2, 7)
(3)
1μF
500k
A
B
C
N
790
22k
2.4k

TWO-POLE FAST TURN-ON NAB TAPE PREAMP


12V
0.1μF
(1, 8)
(6)
NE542
(4, 5)
(2, 7)
(3)
120pF
680k
220k
220k
2k
2k
24k
2μF
2μF

R1AA MAGNETIC PHONO PREAMP


V_{CC} = +16V
.1μF
6
1, 8
2, 7
NE542
4, 5
3
OUT
1800pF
56k
1.5k
360k
6800pF
47k
470
50μF
91k

NOTE: All resistors values are typical and in ohms.

DESCRIPTION

The NE570/571 is a versatile low cost dual gain control circuit in which either channel may be used as a dynamic range compressor or expandor. Each channel has a full wave rectifier to detect the average value of the signal; a linerarized, temperature compensated variable gain cell; and an operational amplifier.

The NE570/571 is well suited for use in telephone subscriber and trunk carrier systems, communications systems and hi-fi audio systems.

FEATURES

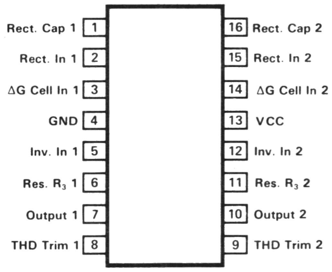
- **Complete compressor and expandor in 1 IC**
- **Temperature compensated**
- **Greater than 110dB dynamic range**
- **Operates down to 6Vdc**
- **System levels adjustable with external components**
- **Distortion may be trimmed out**

APPLICATIONS

- **Telephone trunk compandor—570**
- **Telephone subscriber compandor—571**
- **High level limiter**
- **Low level expandor—noise gate**
- **Dynamic noise reduction systems**
- **Voltage controlled amplifier**
- **Dynamic filters**

PIN CONFIGURATION

F, N PACKAGE

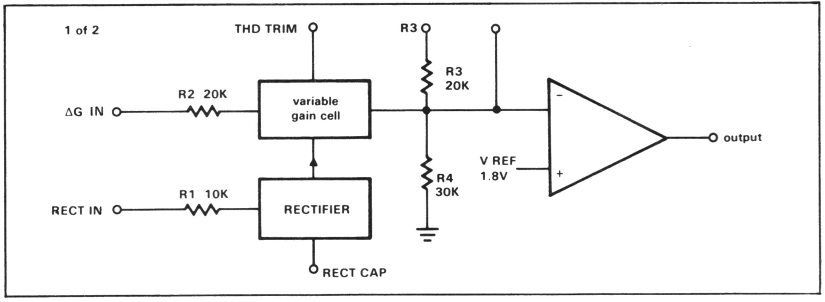


Order Part No.
NE570 N,F
NE571 N,F

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
	Positive supply		Vdc
	570	24	
	571	18	
T_A	Operating temperature range	-40 to +70	°C
P_D	Power dissipation	400	mW

BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The NE570/571 compandor building blocks, as shown in the block diagram, are a full wave rectifier, a variable gain cell, an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.

The full wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at V_{REF}. The rectified current is averaged on an external filter capacitor tied to the C_{RECT} terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively coupled voltage inputs as shown in the following equation. Note that for capacitively coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than .1μA.

$$G \propto \frac{|V_{IN} - V_{REF}|\ ave}{R_1}$$

or

$$G \propto \frac{|V_{IN}|\ ave}{R_1}$$

The speed with which gain changes to follow changes in input signal levels is determined by the rectifier filter capacitor. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the variable gain cell. In an expandor or compressor application, this would lead to third harmonic distortion, so there is a tradeoff to be made between fast attack and decay times, and distortion. For step changes in amplitude, the change in gain with time is shown by this equation.

$$G(t) = (G_{initial} - G_{final})\ e^{-t/\tau}$$

$$+ G_{final};\ \tau = 10K \times C_{RECT}$$

The variable gain cell is a current in, current out device with the ratio I_{OUT}/I_{IN} controlled by the rectifier. I_{IN} is the current which flows from the ΔG input to an internal summing node biased at V_{REF}. The following equation applies for capacitively coupled inputs. The output current, I_{OUT}, is fed to the summing node of the op amp.

$$I_{IN} = \frac{V_{IN} - V_{REF}}{R_2} = \frac{V_{IN}}{R_2}$$

A compensation scheme built into the ΔG cell compensates for temperature, and cancels out odd harmonic distortion. The only distortion which remains is even harmonics, and they exist only because of internal offset voltages. The THD trim terminal provides a means for nulling the internal offsets for low distortion operation.

The operational amplifier (which is internally compensated) has the non-inverting input tied to V_{REF}, and the inverting input connected to the ΔG cell output as well as brought out externally. A resistor, R_3, is brought out from the summing node and allows compressor or expandor gain to be determined only by internal components.

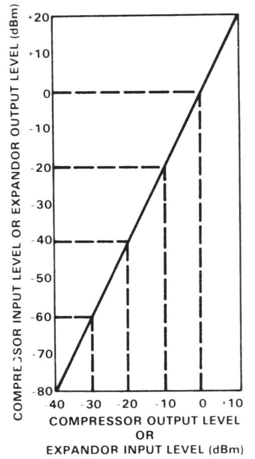
The output stage is capable of ±20mA output current. This allows a +13dBm (3.5V rms) output into a 300Ω load which, with a series resistor and proper transformer, can result in +13dBm with a 600Ω output impedance.

A band gap reference provides the reference voltage for all summing nodes, a regulated supply voltage for the rectifier and ΔG cell, and a bias current for the ΔG cell. The low tempco of this type of reference provides very stable biasing over a wide temperature range.

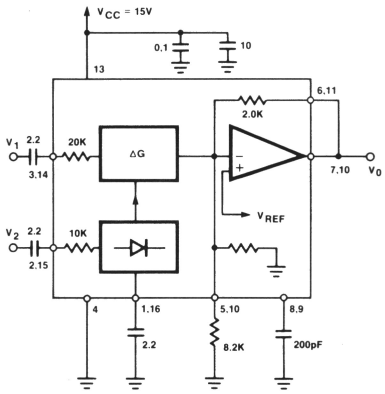
The typical performance characteristics illustration shows the basic input-output transfer curve for basic compressor or expandor circuits.

TYPICAL PERFORMANCE CHARACTERISTICS

BASIC INPUT-OUTPUT TRANSFER CURVE



TYPICAL TEST CIRCUIT



DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 15V$[1]

PARAMETER	TEST CONDITIONS	NE570 Min	NE570 Typ	NE570 Max	NE571 Min	NE571 Typ	NE571 Max	UNIT
V_{CC} Supply voltage		6		24	6		18	V
I_{CC} Supply current	No signal		3.2	4.0		3.2	4.8	mA
Output current capability		±20						mA
Output slew rate			±.5					V/us
Gain cell distortion[2]	Untrimmed		.3	1.0		.5	2.0	%
	Trimmed		.05			.1		
Resistor tolerance			±5	±15				%
Internal reference voltage		1.7	1.8	1.9	1.65	1.8	1.95	V
Output dc shift[3]	Untrimmed		±20	±50		±30	±100	mV
Expandor output noise	No signal, 20Hz-20kHz		20					μV
			−15					dBRNC
Unity gain level		−1	0	+1	−1.5	0	+1.5	dBm
Gain change[2,4]	−40°C < T < 70°C		±.1			±.1		dB
	0°C < T < 70°C		±.1	±.2		±.1	±.4	
Reference drift[4]	−40°C < T < 70°C		+2, −25	·10, −40		+2, −25	+20, −50	mV
	0°C < T < 70°C		±5	±10		±5	±20	
Resistor drift[4]	−40°C < T < 70°C		+8,−0					%
	0°C < T < 70°C		+1,−0					
Tracking error [5], input V_1 = OdBm	Rectifier input, V_2 =							dB
	+6dBm		±.2					
	−10dBm		+.2	−.2,+.4		+.2	−.2,+.5	
	−20dBm		+.2	−.3,+.6		+.2	−.4,+.7	
	−30dBm		+.2	−.5,+1		+.2	−1,+1.5	
	−40dBm		+.2,−.4			+.2,−.4		

NOTES

1. Except where indicated, the 571 specifications are identical to the 570
2. Measured at OdBm,1kHz
3. Expandor ac input change from no signal to OdBm
4. Relative to value at T_A = 25°C
5. Relative to OdBm

DESCRIPTION

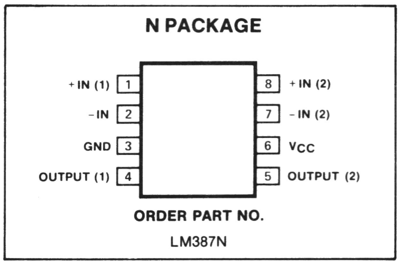
The LM387 is a dual preamplifier for the amplification of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with an internal power supply decoupler-regulator, providing 110dB supply rejection and 60dB channel separation. Other outstanding features include high gain (104dB), large output voltage swing (V_{CC} - 2V p-p), and wide power bandwidth (75kHz, 20V p-p). The LM387 operates from a single supply across the wide range of 9 to 40V.

The amplifiers are internally compensated for all gains greater than 10. The LM387 is available in an 8 lead dual-in-line package.

FEATURES

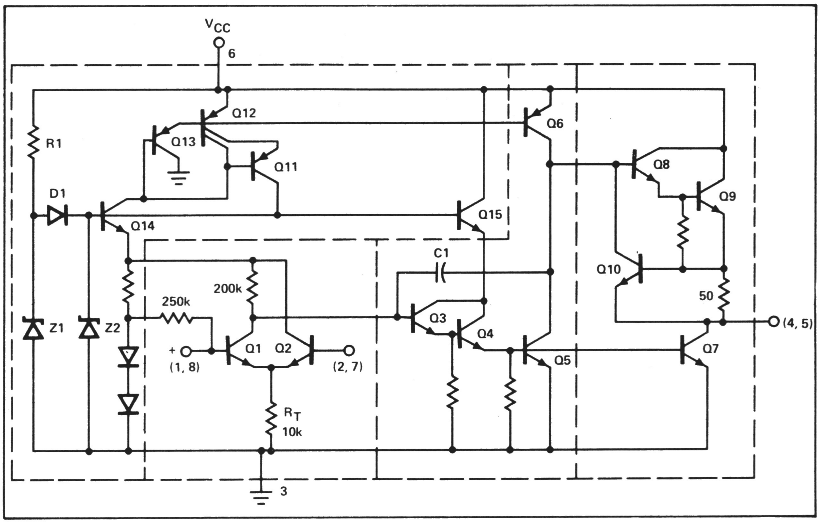
- **Low noise—0.8μV total input noise**
- **High gain—104dB open loop**
- **Single supply operation**
- **Wide supply range 9 to 40V**
- **Power supply rejection—110dB**
- **Large output voltage swing (VCC - 2V p-p)**
- **Wide bandwidth 15MHz unity gain**
- **Power bandwidth 75kHz, 20V p-p**
- **Internally compensated**
- **Short circuit protected**

PIN CONFIGURATION



ORDER PART NO.
LM387N

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	+40	V
Power dissipation	500	mW
Operating temperature range	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	+300	°C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 14V unless otherwise specified.

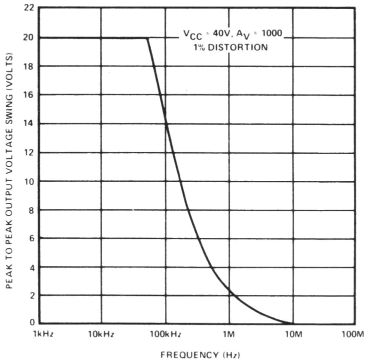
PARAMETER	TEST CONDITIONS	LM387			UNIT
		Min	Typ	Max	
Voltage gain	Open loop		160,000		V/V
Supply current	V_{CC} 9 to 40V, $R_L = \infty$		10		mA
Input resistance	Positive input		100		kΩ
	Negative input		200		kΩ
Input current	Negative input		0.5		μA
Output resistance	Open loop		150		Ω
Output current	Source		8		mA
	Sink		2		mA
Output voltage swing	Peak-to-peak		V_{CC}-2		V

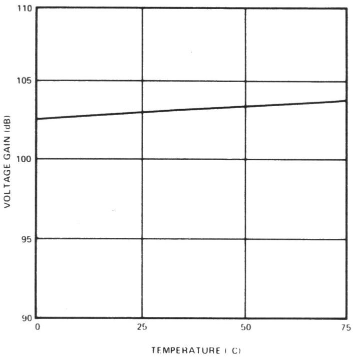
AC ELECTRICAL CHARACTERISTICS

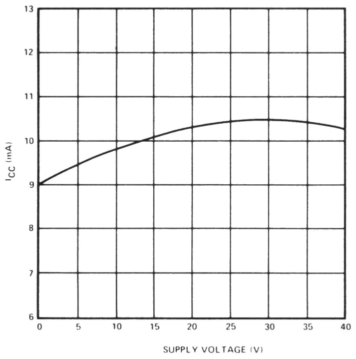
$T_A = 25\ °C$, $V_{CC} = 14V$ unless otherwise specified.

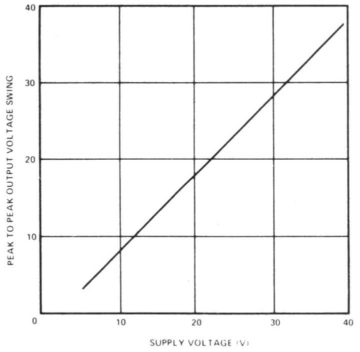
PARAMETER	TEST CONDITIONS	LM387 Min	LM387 Typ	LM387 Max	UNIT
Small signal bandwidth			15		MHz
Power bandwidth	20V p-p ($V_{CC} = 24V$)		75		kHz
Maximum input voltage	Linear operation			300	μVrms
Supply rejection ratio	f = 1kHz		110		dB
Channel separation	f = 1kHz		60		dB
Total harmonic distortion	75dB gain, f = 1kHz		0.1		%
Total equivalent input noise	$R_S = 600\Omega$, 100-10,000Hz		0.8	1.4	μVrms
Noise figure	50kΩ, 100-10,000Hz		1.0		dB
	10kΩ, 100-10,000Hz		1.6		dB
	5kΩ, 100-10,000Hz		2.8		dB

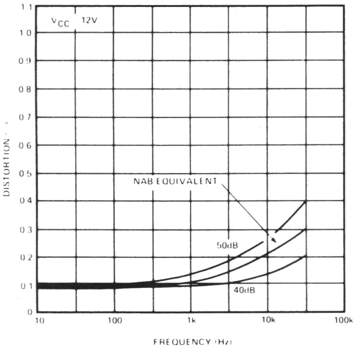
TYPICAL PERFORMANCE CHARACTERISTICS

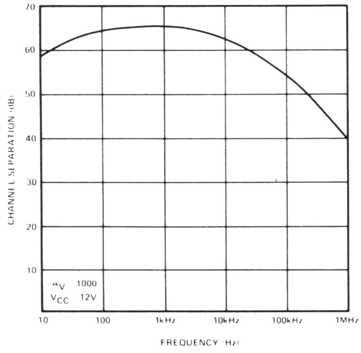

LARGE SIGNAL FREQUENCY RESPONSE


GAIN vs TEMPERATURE


V_{CC} vs I_{CC}

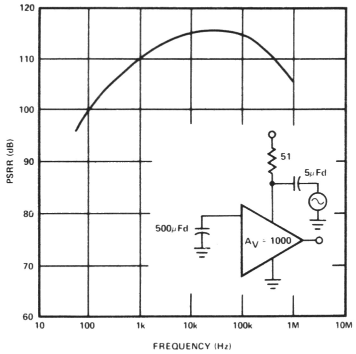

P-P OUTPUT VOLTAGE SWING vs V_{CC}


% DISTORTION

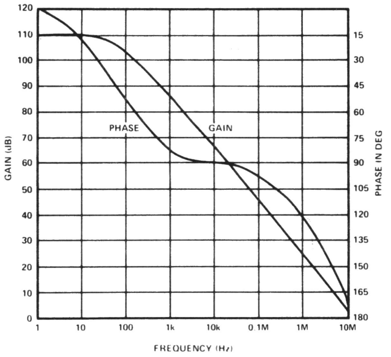

CHANNEL SEPARATION

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

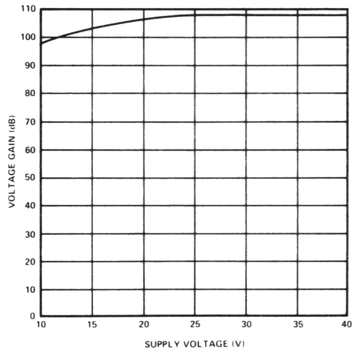
PSRR vs FREQUENCY



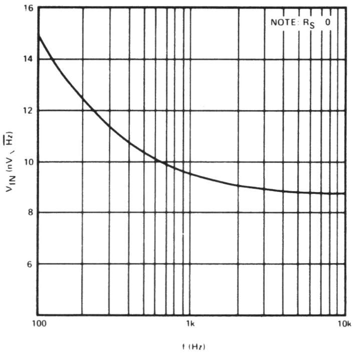
GAIN AND PHASE RESPONSE



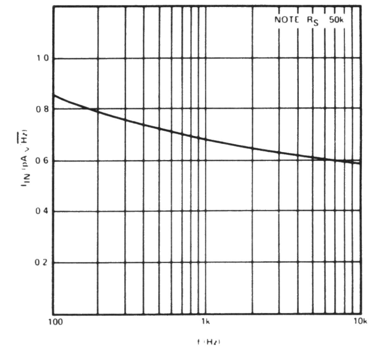
VOLTAGE GAIN vs SUPPLY VOLTAGE



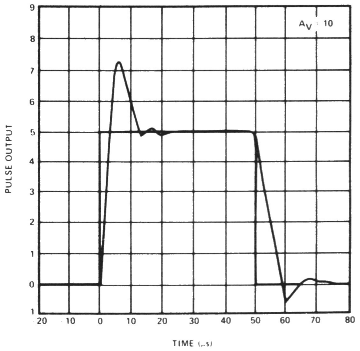
NOISE VOLTAGE vs FREQUENCY



NOISE CURRENT vs FREQUENCY

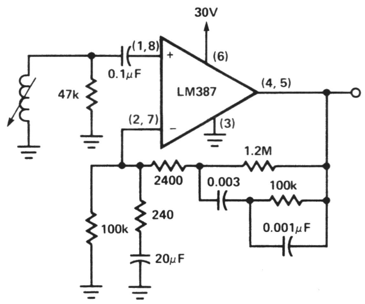


PULSE RESPONSE

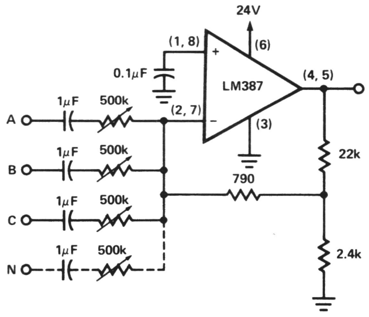


TYPICAL APPLICATIONS

TYPICAL MAGNETIC PHONO PREAMPLIFIER

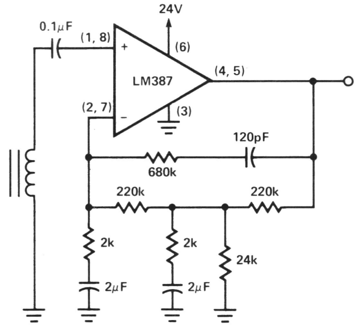

30V
(1, 8)
(6)
0.1µF
47k
LM387
(4, 5)
(2, 7)
(3)
1.2M
2400
0.003
100k
240
100k
0.001µF
20µF

AUDIO MIXER

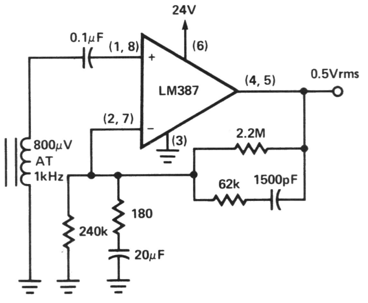

24V
(1, 8)
(6)
0.1µF
LM387
(4, 5)
(2, 7)
(3)
A
B
C
N
1µF
500k
1µF
500k
1µF
500k
1µF
500k
790
22k
2.4k

TYPICAL APPLICATIONS (Cont'd)

TWO-POLE FAST TURN-ON NAB TAPE PREAMPLIFIER


24V
0.1μF
(1, 8)
+
(6)
LM387
(4, 5)
(2, 7)
−
(3)
120pF
680k
220k
220k
2k
2k
24k
2μF
2μF

TYPICAL TAPE PLAYBACK AMPLIFIER


24V
0.1μF
(1, 8)
+
(6)
LM387
(4, 5)
0.5Vrms
(2, 7)
−
(3)
2.2M
800μV
AT
1kHz
62k
1500pF
180
240k
20μF

AM RECEIVER CIRCUIT — TCA 440

TCA 440-N

DESCRIPTION

TCA440 is a monolithic IC, especially developed for AM receivers up to 50MHz. It includes a RF stage with AGC, a balanced mixer, separate oscillator and an IF amplifier with AGC. Because of its low current consumption and of its internal stabilization the TCA440 is perfectly suited for battery operated portables, car and home radios.

FEATURES

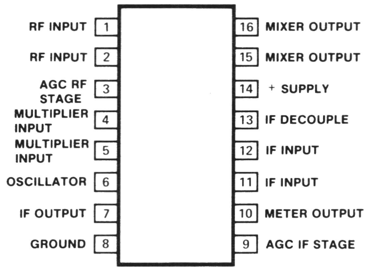
- **Balanced circuit**
- **Separately controllable prestage**
- **Multiplicative push-pull mixer with separate oscillator**
- **High signal handling capability even with 4.5V supply voltage**
- **100dB feedback control range in 5 stages**
- **Direct connection for tuning meter**
- **Minimum external components**

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	15	V
T_{amb}	Ambient temperature in operation	-15 to +80	°C
T_s	Storage temperature	-30 to +125	°C
V_{CC}	Range of operation	4.5 to 15	V

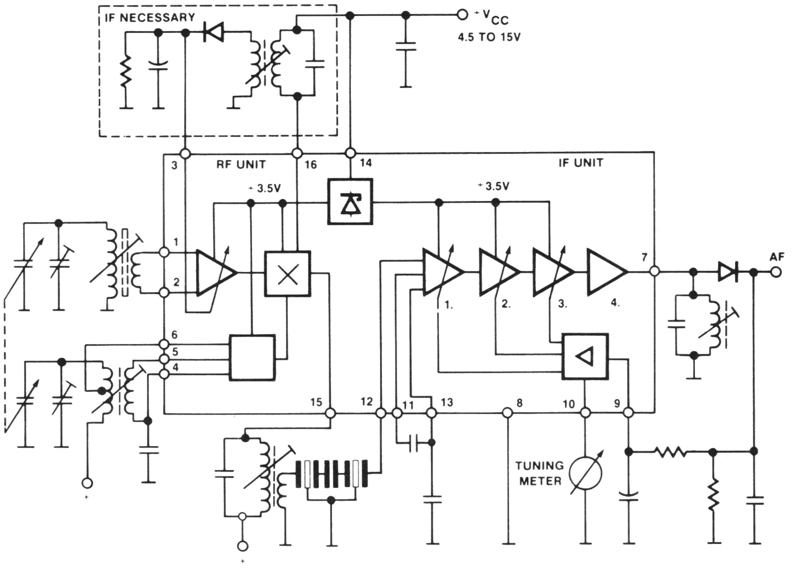
PIN CONFIGURATION

N PACKAGE


RF INPUT 1
RF INPUT 2
AGC RF STAGE 3
MULTIPLIER INPUT 4
MULTIPLIER INPUT 5
OSCILLATOR 6
IF OUTPUT 7
GROUND 8
16 MIXER OUTPUT
15 MIXER OUTPUT
14 + SUPPLY
13 IF DECOUPLE
12 IF INPUT
11 IF INPUT
10 METER OUTPUT
9 AGC IF STAGE

ORDER PART NO.
TCA440N

BLOCK DIAGRAM


IF NECESSARY
+VCC
4.5 TO 15V
3
RF UNIT
16
14
IF UNIT
+3.5V
+3.5V
1
2
1.
2.
3.
4.
7
AF
6
5
4
15
12
11
13
8
10
9
TUNING METER

TUNING METER

Recommended instruments:

500μA ($R_1 = 800k\Omega$)
or
300μA ($R_1 = 1.5k\Omega$)

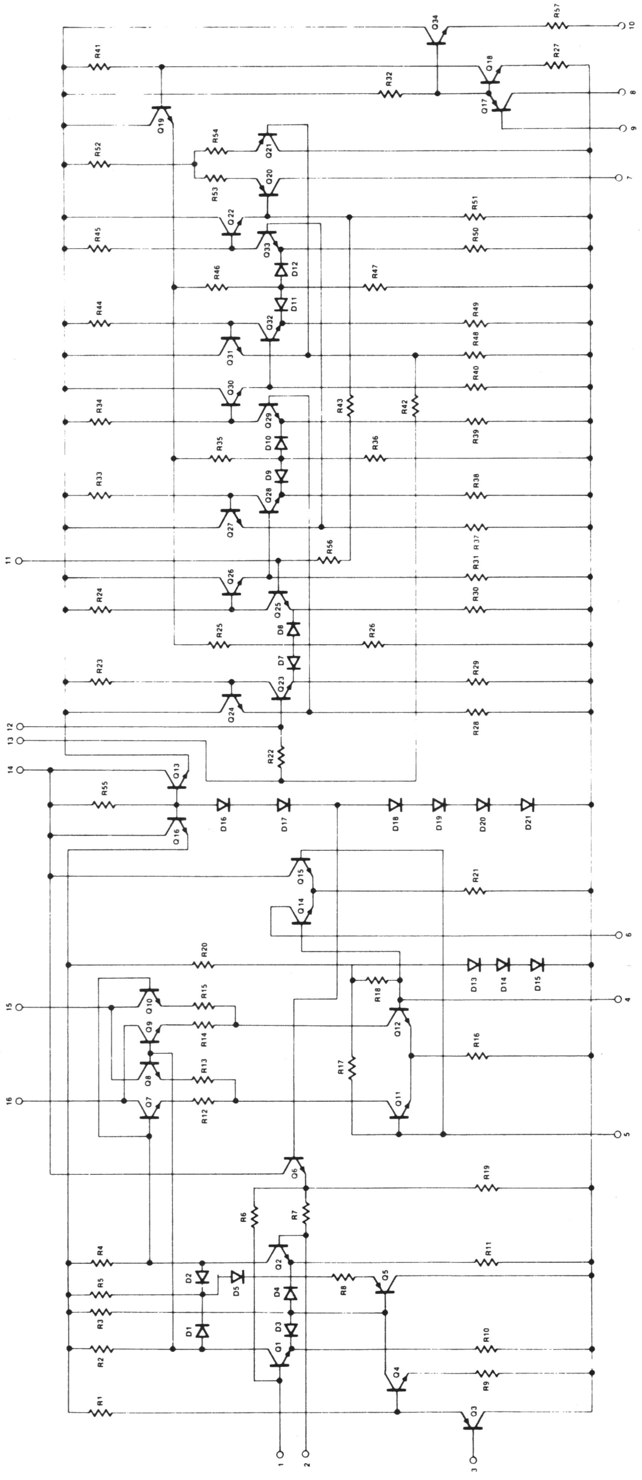
The IC offers at pin 10 a tuning meter voltage of 600 mV_{EMP} max. with a source impedance of approx. 400Ω.

FUNCTION

As pictured in the circuit diagram the TCA440 comprises two control loops independent of each other which control the RF stage and the IF stages. By AGCing the RF stage, excellent signal handling is obtained. A voltage of 2.6V_{pp} on the IC input can be handled with very low distortion. The push-pull mixer operates multiplicatively, thereby resulting in few harmonic mixing products and whistling points. The oscillator which is separated from the mixer is also apted excellently for short waves. From the AGC of the RF amplifier a voltage is derived for a tuning meter which can be connected directly to the meter. The symmetric composition of the circuit provides high stability against oscillation and, at the same time, an AGC range of more than 100dB. The bridge circuit of the mixer provides good isolation of the oscillator.

TCA 440-N

EQUIVALENT SCHEMATIC


1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q26
Q27
Q28
Q29
Q30
Q31
Q32
Q33
Q34
D1
D2
D3
D4
D5
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18
D19
D20
D21
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31
R32
R33
R34
R35
R36
R37
R38
R39
R40
R41
R42
R43
R44
R45
R46
R47
R48
R49
R50
R51
R52
R53
R54
R55
R56
R57

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 9V, T_A = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	TCA 440			UNIT
			Min	Typ	Max	
I_{CC}	Total current consumption at:	V_{CC} = 4.5V		7		mA
		V_{CC} = 9V		10.5		mA
		V_{CC} = 15V		12		mA

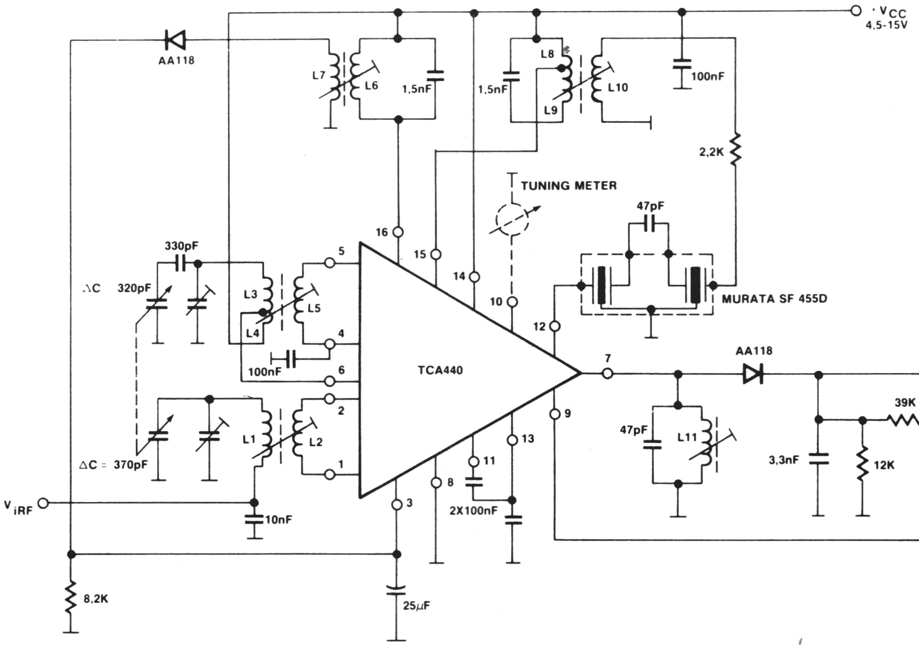
AC ELECTRICAL CHARACTERISTICS

V_{CC} = 9V, T_A = 25°C, f_{IRF} = 600kHz, fmod = 1kHx unless otherwise specified.

PARAMETER		TEST CONDITIONS	TCA 440			UNIT
			Min	Typ	Max	
ΔG_{RF}	RF level deviation for (m = 80%)	ΔV_{AF} = 6dB		65		dB
		ΔV_{AF} = 10dB		80		dB
V_{AFeff}	AF output voltage for V_{IRF} (symm. measured at 1-2)	m = 80% V_{IRF} = 20μV		140		mV
		V_{IRF} = 1mV		260		
		V_{IRF} = 500mV		350		
		m = 30% V_{IRF} = 20μV		50		mV
		V_{IRF} = 1mV		100		
		V_{IRF} = 500mV		130		
V_{IRF}	Input sensitivity (measured at 60Ω, f_{IRF} = 1MHz, m = 30%/0%, R_G = 540Ω)	At signal-to-noise distance				
		$\frac{S+N}{N}$ = 6dB		1		μV
		$\frac{S+N}{N}$ = 26dB		7		μV
		$\frac{S+N}{N}$ = 58dB		1		mV
RF unit						
f_{IRF}	Input frequency range			0 to 50		MHz
f_{IF}	Output frequency	f_{IF} = f_{OSC} = f_{IRF}		460		kHz
ΔG_V	Control range			38		dB
V_{IRFpp}	Input voltage	for 600kHz, m = 80%, for Overdrive, k_{AF} = 10%, Symmetrically measured at pins 1 & 2 (mean carrier value)		2.6		Vpp
V_{IRFeff}				.5		V
s_{IF}	IF suppression between 1-2 to 15			20		dB
Z_I	RF input impedance	Asymmetrical coupling at:				
		G_{RFmax}		2/5		kΩ/pF
		G_{RFmin}		2.2/1.5		kΩ/pF
		Symmetrical coupling at:				
		G_{RFmax}		4/5		kΩ/pF
		G_{RFmin}		4.5/1.5		kΩ/pF
Z_{gosc}	Mixer output impedance	Pins 15 or 16		250/4.5		kΩ/pF
IF unit						
f_{IIF}	Input frequency range			0 to 2		MHz
ΔG_V	Control range at 460kHz			62		dB
V_{IFeff}	Input voltage	Mean carrier value at G_{min} for Overdrive (k_{AF} = 10%), measured at Pin 12 (60Ω to ground, f_{IF} = 460kHz, m = 80%, f_{mod} = 1kHz)		200		mV
V_{AFeff}	AF output voltage	V_{IIF} at 60Ω (Pin 12) f_{mod} = 1kHz				
		V_{IF} = 30μV, m = 80%		50		mV
		V_{IF} = 3mV, m = 80%		200		mV
		V_{IF} = 3mV, m = 30%		70		mV
Z_I	IF input impedance	Asymmetrical coupling		3/3		kΩ/pF
Z_g	IF output impedance	Pin 7		200/8		kΩ/pF

TYPICAL APPLICATIONS

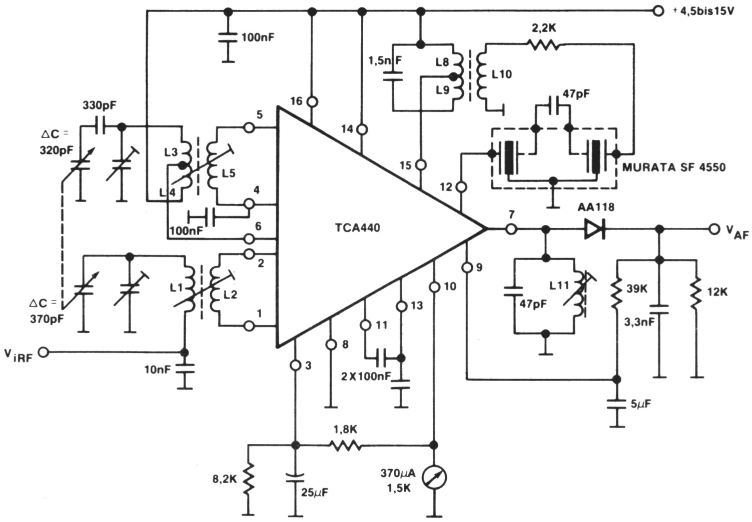
APPLICATION EXAMPLE FOR MW


+VCC 4,5-15V
AA118
L7
L6
1,5nF
1,5nF
L8
L9
L10
100nF
2,2K
TUNING METER
47pF
MURATA SF 455D
330pF
ΔC 320pF
L3
L4
L5
100nF
ΔC = 370pF
L1
L2
TCA440
16
15
14
10
12
5
4
6
2
1
3
8
11
13
9
7
2X100nF
AA118
VAF
47pF
L11
39K
3,3nF
12K
5μF
ViRF
10nF
8,2K
25μF

L1-L2 with V_{ogt} coil set D21-2375.1
L3-L1 with V_{ogt} coil set D41-2519

L1	105 turns	12 x 0.04 CuLS
L2	7 turns	0.10 CuL
L3	80 turns	12 x 0.04 CuLS
L4	35 turns	12 x 0.04 CuLS
L5	15 turns	0.10 CuL
L6	70 turns	12 x 0.04 CuLS
L7	35 turns	12 x 0.04 CuLS
L8	20 turns	12 x 0.04 CuLS
L9	50 turns	12 x 0.04 CuLS
L10	22 turns	12 x 0.04 CuLS
L11	400 turns	0.06 CuL

APPLICATION EXAMPLE FOR MW


+4,5bis15V
100nF
2,2K
1,5nF
L8
L9
L10
47pF
MURATA SF 4550
330pF
ΔC = 320pF
L3
L4
L5
100nF
ΔC = 370pF
L1
L2
TCA440
16
14
15
12
5
4
6
2
1
3
8
11
13
10
9
7
AA118
VAF
47pF
L11
39K
3,3nF
12K
5μF
ViRF
10nF
2X100nF
1,8K
8,2K
25μF
370μA 1,5K

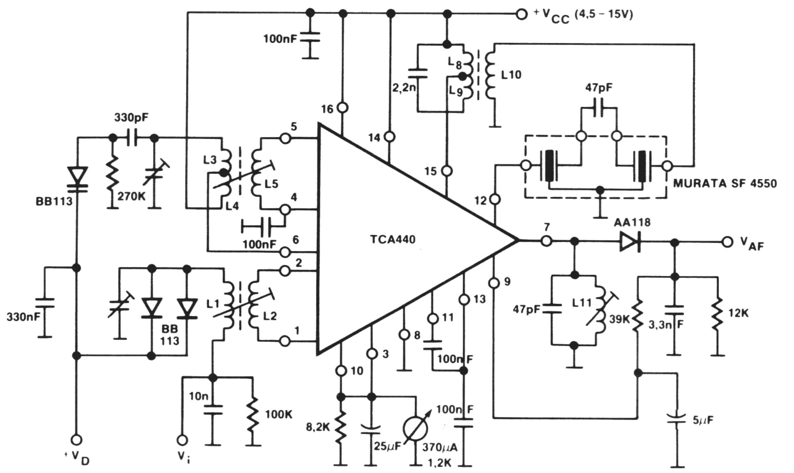
Prestage control is derived from IF control

L1	105 turns	12 x 0.04 CuLS
L2	7 turns	0.10 CuL
L3	80 turns	12 x 0.04 CuLS
L4	35 turns	12 x 0.04 CuLS
L5	15 turns	0.10 CuL
L8	20 turns	12 x 0.04 CuLS
L9	50 turns	12 x 0.04 CuLS
L10	22 turns	12 x 0.04 CuLS
L11	400 turns	0.04 CuL

L1-L2 with V_{ogt} coil set D21-23751
L3-L11 with V_{ogt} coil set D41-2519

TYPICAL APPLICATIONS (Cont'd)

APPLICATION EXAMPLE FOR AM USING VARICAP DIODES BB 113

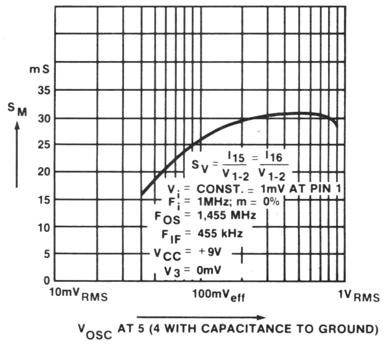

+VCC (4,5 - 15V)
100nF
2,2n
L8
L9
L10
47pF
330pF
16
14
15
5
4
6
2
1
L3
L5
L4
270K
BB113
100nF
MURATA SF 4550
12
7
AA118
V AF
TCA440
9
13
11
8
3
10
330nF
L1
L2
BB 113
47pF
L11
39K
3,3nF
12K
100nF
10n
100K
8,2K
25μF
370μA 1,2K
100nF
5μF
+V D
V i

L1	105 turns	12 x 0.04 CuLS
L2	7 turns	0.10 CuL
L3	80 turns	12 x 0.04 CuLS
L4	35 turns	12 x 0.04 CuLS
L5	15 turns	0.10 CuL
L8	20 turns	12 x 0.04 CuLS
L9	50 turns	12 x 0.04 CuLS
L10	22 turns	12 x 0.04 CuLS
L11	400 turns	0.06 CuL

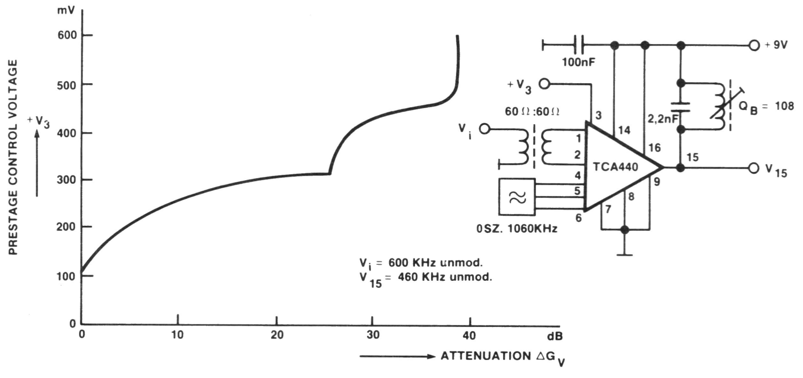
L1-L2 with Vogt coil set D21-23751
L3-L11 with Vogt coil set D41-2519

$V_D = 8.5V \rightarrow f_i = 800kHz$
$V_D = 30V \rightarrow f_i = 1620kHz$

CONVERSION CONDUCTANCE vs OSCILLATOR VOLTAGE



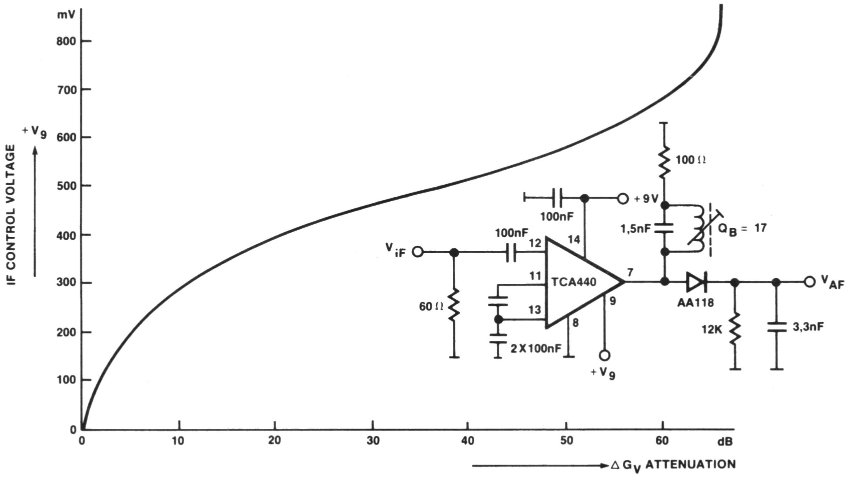
RF STAGE CONTROL



The input is not power matched and can be driven with a higher resistance, V_i is chosen so that a constant V_{15} is obtained (50mV$_{pp}$).

TYPICAL APPLICATIONS (Cont'd)

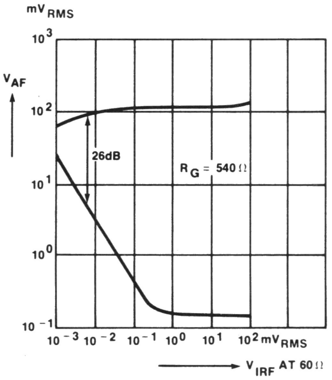
IF CONTROL



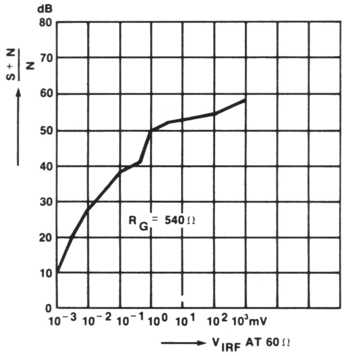
VIF (469kHz; m = 80%; fmod = 1kHz) is chosen so that always a constant VAF is obtained (200mVRMS)

TYPICAL PERFORMANCE CHARACTERISTICS

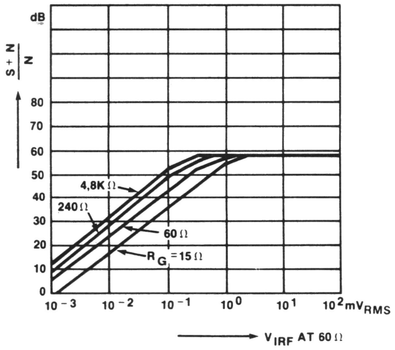
AF OUTPUT VOLTAGE AND NOISE FIGURE vs RF INPUT VOLTAGE (switching position 1)



SIGNAL TO NOISE DISTANCE vs RF INPUT VOLTAGE (switching position 2)

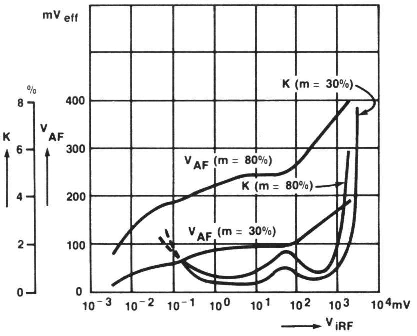


SIGNAL TO NOISE DISTANCE vs RF INPUT VOLTAGE (parameter is generator impedance) (switching position 1)

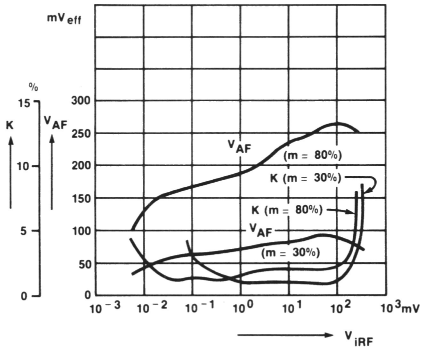


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

TEST FIGURES FOR APPLICATION EXAMPLE FOR MW HARMONIC DISTORTION AND AF OUTPUT VOLTAGE vs RF INPUT VOLTAGE MEASURED SYMMETRICALLY AT PINS 1 AND 2 f_i = 1MHz, f_{mod} = 1kHz, f_{IF} = 455kHz, V_{CC} = 9V



TEST FIGURES FOR APPLICATION EXAMPLE FOR AM USING BB 113 f_i = 1MHz, f_{mod} = 1kHz, f_{IF} = 455 kHz, V_{CC} = 9V, V_{IRF} measured symmetrically at pins 1 and 2

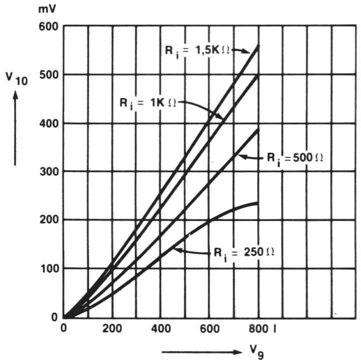


Example for moving coil instruments

R_i for full-scale deflection

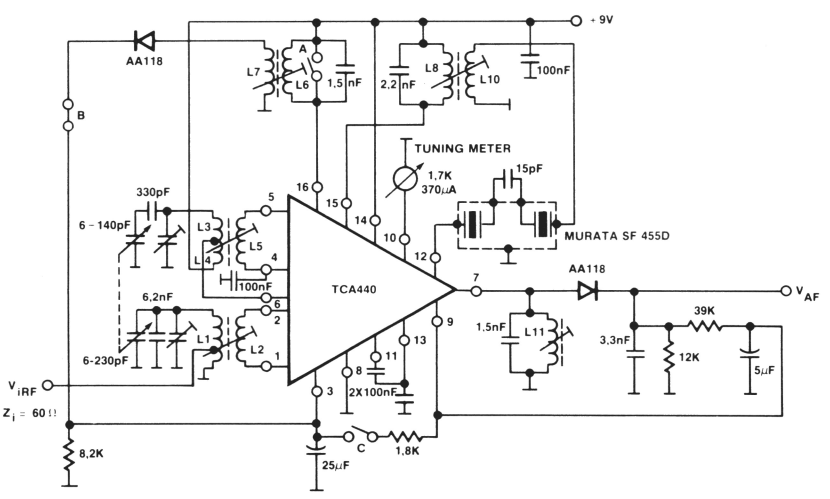
1.5kΩ	100μA
1.5kΩ	170μA
2kΩ	200μA
350Ω	500μA

TUNING METER VOLTAGE vs IF CONTROL VOLTAGE (parameter is impedance of tuning meter)



TEST CIRCUITS

TEST CIRCUIT FOR NOISE FIGURE


+9V
AA118
B
L7
A
L6
1,5 nF
2,2 nF
L8
L10
100nF
TUNING METER
1,7K
370μA
15pF
330pF
6 - 140pF
L3
L4
L5
100nF
6,2nF
6-230pF
L1
L2
16
15
14
10
12
5
4
6
2
1
TCA440
MURATA SF 455D
7
AA118
V AF
9
13
11
8
3
2X100nF
1,5nF
L11
3,3nF
39K
12K
5μF
V iRF
Z i = 60 Ω
8,2K
25μF
C
1,8K

L1-L2 M25 pot core
L3-L11 with Vogt coil set D41-2519

L1	2 + 6	turns	6 x 12 x 0.04 CuLS
L2	n		0.15 CuL
L3	90	turns	12 x 0.04 CuLS
L4	35	turns	12 x 0.04 CuLS
L5	15	turns	0.10 CuL
L6	70	turns	12 x 0.04 CuLS
L7	35	turns	12 x 0.04 CuLS
L8	60	turns	12 x 0.04 CuLS
L10	22	turns	12 x 0.04 CuLS
L11	68	turns	0.06 CuL

	switch		
A	B	C	
off	on	off	separate RF stage control
on	off	on	RF stage control voltage derived from IF control voltage

f_i = 1MHz; m = 30%

n(turns)	$R_{Generator}$(Ω)
1	15
2	60
4	240
6	540
9	1,2K
12	2,2K
18	4,8K

SECTION 12
TV CIRCUITS

Section 12—TV CIRCUITS

ULN2211	2-Watt TV/FM Sound Channel	277
TBA120S	8-Stage Amplifier with Balanced Demodulator	280
TBA1441	TV Video Amplifier with Demodulator	284
TDA2541	Video IF System	288

NOTE

* Any product listed in this section but not incorporated within the text may be obtained by writing Information Services at Signetics, 811 E. Arques, M/S 027, Sunnyvale, California 94086, or by calling (408) 746-1682.

2-WATT TV/FM SOUND CHANNEL — ULN2211

ULN2211-N

DESCRIPTION

The ULN2211 contains a limiting amplifier, an FM quadrature detector, an electronic gain control stage and a 2-watt audio output stage. It can be used to detect and amplify any FM modulated signal having a 0.1-20MHz carrier frequency.

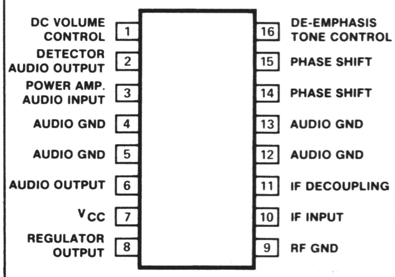
It is especially recommended as a complete TV sound channel requiring few external components and only one tuning adjustment for the 4.5MHz tank circuit. Provision is made for 6dB/octave de-emphasis and tone control.

FEATURES

- **2-watt output**
- **DC volume control attenuation, 70dB typ**
- **Limiter gain of 70dB**
- **Limiting threshold typically less than 200μV**
- **Automatic thermal shutdown**
- **Over-current limiting**
- **20dB ripple rejection**
- **Single supply operation (18-30V)**
- **No crossover distortion**

PIN CONFIGURATION

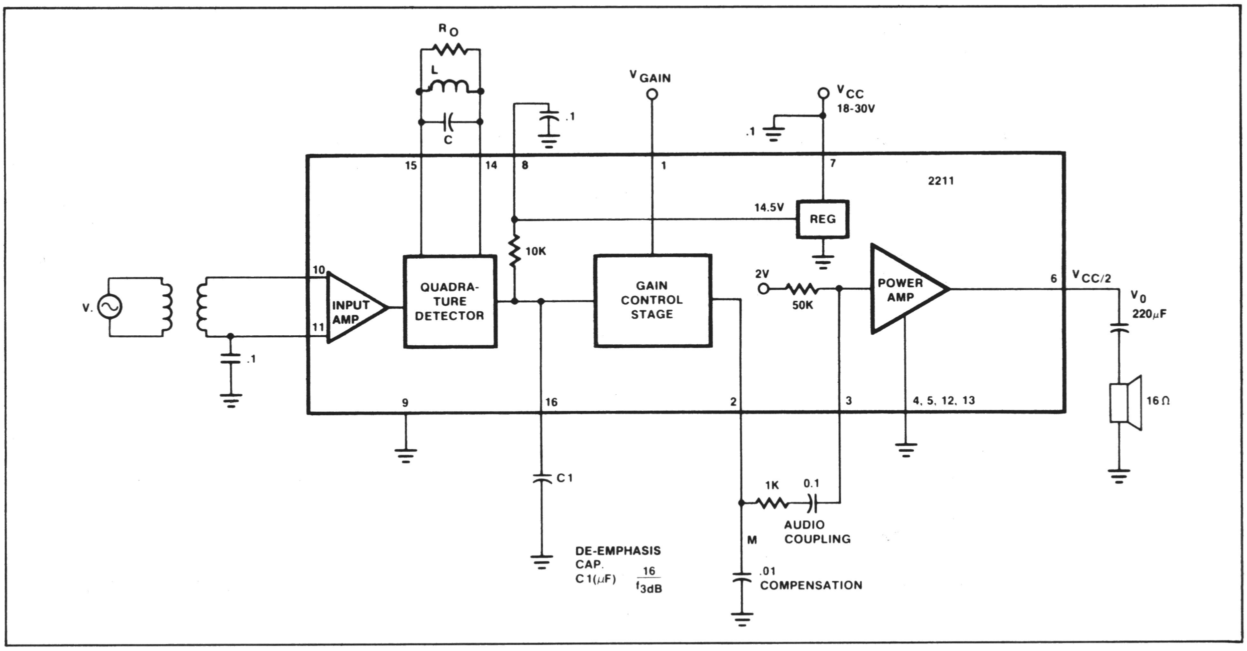
N PACKAGE


DC VOLUME CONTROL 1
DETECTOR AUDIO OUTPUT 2
POWER AMP. AUDIO INPUT 3
AUDIO GND 4
AUDIO GND 5
AUDIO OUTPUT 6
VCC 7
REGULATOR OUTPUT 8
16 DE-EMPHASIS TONE CONTROL
15 PHASE SHIFT
14 PHASE SHIFT
13 AUDIO GND
12 AUDIO GND
11 IF DECOUPLING
10 IF INPUT
9 RF GND

ORDER PART NO.
ULN2211N

NOTE: Internal power dissipation in watts.

BLOCK DIAGRAM


RO
L
C
.1
VGAIN
VCC 18-30V
.1
15
14
8
1
7
2211
14.5V
REG
10K
10
11
INPUT AMP
QUADRATURE DETECTOR
GAIN CONTROL STAGE
2V
50K
POWER AMP
6
VCC/2
VO
220μF
16Ω
V.
.1
9
16
2
3
4, 5, 12, 13
C1
1K
0.1
M
AUDIO COUPLING
DE-EMPHASIS CAP. C1(μF) 16/f3dB
.01 COMPENSATION

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage, V_{CC}	+30	V
Input voltage (pin 10)	+4.0	Vrms
Power consumption (internal)	See Figure 1	
Operating temperature	-25 to +70	°C
Storage temperature	-65 to +150	°C

AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = +24V$; $f_o = 4.5MHz$, $\Delta f = 25kHz$, $f_m = 400Hz$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	ULN2211			UNIT
			Min	Typ	Max	
V_{TH}	Recovered audio limiting threshold[1]	Adjust V_1 for $V_0 = 5.6V$ ($P_O = 2W$)		150	350	μV
AMR	AM rejection[2]	Adjust V_1 for 2W, $V_{IN} = 10mV$	30	55		dB
V_O	Recovered AF voltage (pin 16)	$V_{IN} = 10mV$, f = 25kHz	500	800		mVrms
THD_D	Detector output distortion	$V_{IN} = 10mV$, f = 25kHz		1.0	2.0	%
THD_O	Output distortion	$P_O = 2W$, $R_L = 16$		2	10	%
	Playthrough	$V_1 = 0$		10	15	mVrms
I_{MAX}	Current limit	$R_L = 0$		800		mA
V_N	Noise	$V_{IN} = 0$, $V_1 = +15V$		15	20	mVrms
A_V	Power AMP voltage gain[3]		25	27	29	dB
V_O/V_{CC}	Output tracking (V_6/V_7)	$V_{CC} = 18$ to 27V		0.5		V/V
Z_{IN}	Audio amp input impedance	f = 1kHz	40	50	60	kΩ

NOTES

1. Measured with output at -3dB, reference $V_{IN} = 10mV$, $\Delta f = 25kHz$
2. $AMR = 20 \log \frac{V_0 \text{ (FM, } \Delta f = 7.5kHz)}{V_0 \text{ (AM, 30\%)}}$
3. Set $V_0 = 1Vrms$. $A_V = 20 \log \frac{1}{(V3rms)}$

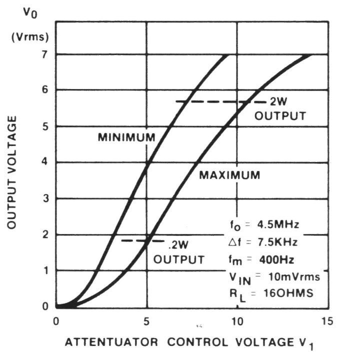
DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = +24V$ unless otherwise specified.

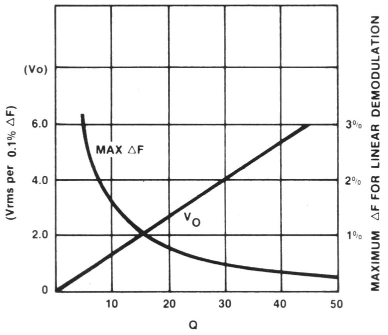
PARAMETER		TEST CONDITIONS	ULN2211			UNIT
			Min	Typ	Max	
I_{CC}	Standby current	$V_{IN} = 0$	25	45	60	mA
V_6	Terminal voltage		10.5	12.5	14.5	V
V_{10}				1.4		V
V_{11}				1.4		V
V_{14}, V_{15}				4.0		V
V_{16}				8.0		V
V_8			14	14.5	16	V
V_2				10		V
V_3				2.6		V

TYPICAL PERFORMANCE CHARACTERISTICS

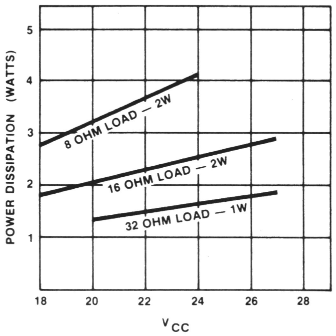
GAIN CONTROL CHARACTERISTIC



OUTPUT VOLTAGE AND LINEAR RANGE vs Q OF DETECTOR COIL

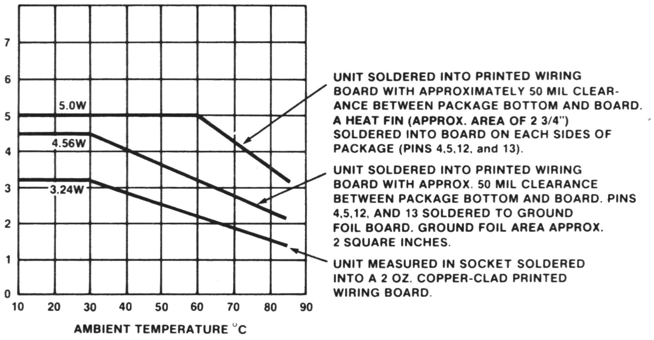


TYPICAL POWER DISSIPATION vs LOAD RESISTANCE AND V_{CC}



ULN2211-N

MAXIMUM ALLOWABLE POWER DISSIPATION



UNIT SOLDERED INTO PRINTED WIRING BOARD WITH APPROXIMATELY 50 MIL CLEARANCE BETWEEN PACKAGE BOTTOM AND BOARD. A HEAT FIN (APPROX. AREA OF 2 3/4") SOLDERED INTO BOARD ON EACH SIDES OF PACKAGE (PINS 4,5,12, and 13).

UNIT SOLDERED INTO PRINTED WIRING BOARD WITH APPROX. 50 MIL CLEARANCE BETWEEN PACKAGE BOTTOM AND BOARD. PINS 4,5,12, AND 13 SOLDERED TO GROUND FOIL BOARD. GROUND FOIL AREA APPROX. 2 SQUARE INCHES.

UNIT MEASURED IN SOCKET SOLDERED INTO A 2 OZ. COPPER-CLAD PRINTED WIRING BOARD.

Figure 1

TYPICAL APPLICATION

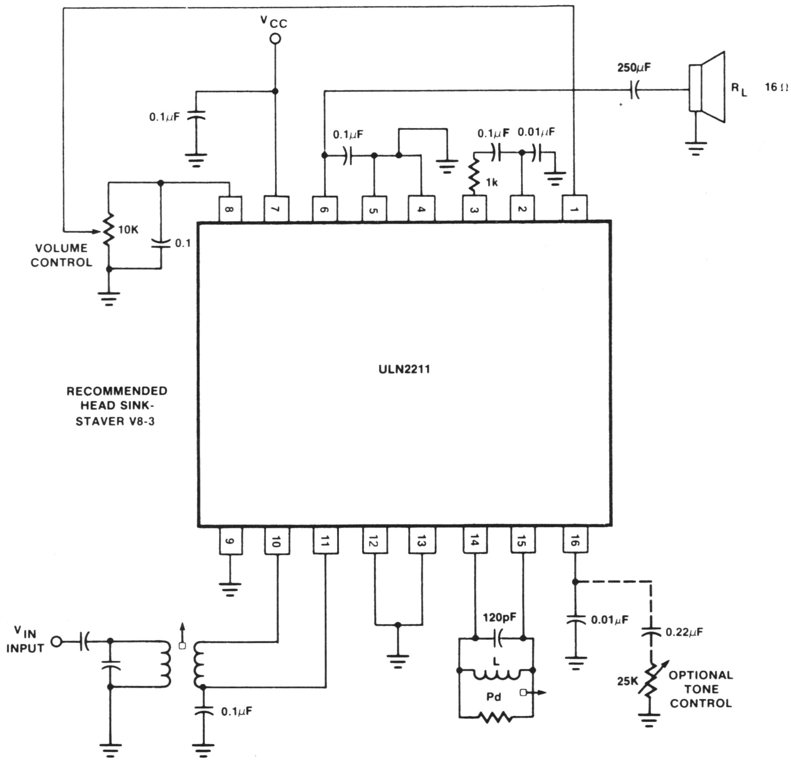

VCC
0.1μF
0.1μF
0.1μF
0.01μF
250μF
RL
16Ω
1k
8
7
6
5
4
3
2
1
10K
0.1
VOLUME CONTROL
ULN2211
RECOMMENDED HEAD SINK-STAVER V8-3
9
10
11
12
13
14
15
16
VIN INPUT
0.1μF
120pF
L
Pd
0.01μF
0.22μF
25K
OPTIONAL TONE CONTROL

Table 1

f₀	L	RD
4.5mHz 10./mHz	10-14μH 1-3μH	∞ 5K

Figure 2

8-STAGE AMPLIFIER WITH BALANCED DEMODULATOR TBA120S

TBA/120S-N

DESCRIPTION

An eight stage amplifier with balanced demodulator for amplifying, limiting and the demodulation of FM signals, specially designed for the sound-IF in TV and RF-IF amplifier in radios. An electronic Volume Control for the audio outputsignal is also provided.

Groups:

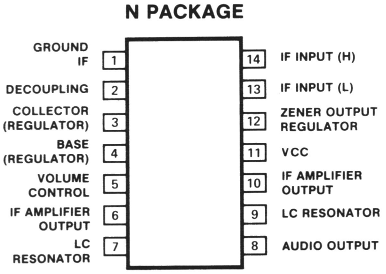
TBA 120 S is delivered in groups:

An attenuation of -30dB of the audio outputsignal requires a resistor from pin 5 to ground as indicated in the table.

Group	2	3	4	5
Value (kΩ)	1.9 to 2.2	2.1 to 2.5	2.4 to 2.9	2.8 to 3.3

For example, devices marked TBA120S-3 indicate group 3.

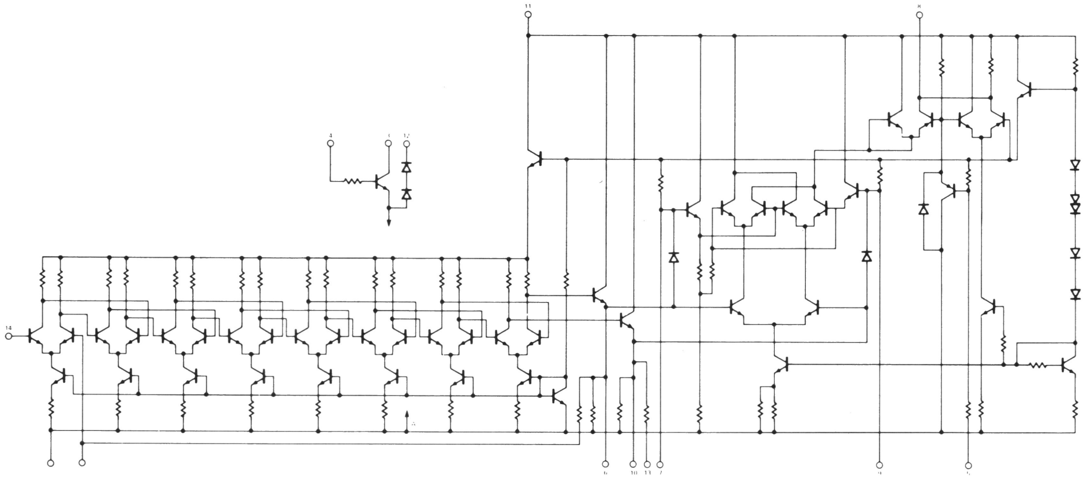
PIN CONFIGURATION


N PACKAGE
GROUND IF 1
DECOUPLING 2
COLLECTOR (REGULATOR) 3
BASE (REGULATOR) 4
VOLUME CONTROL 5
IF AMPLIFIER OUTPUT 6
LC RESONATOR 7
14 IF INPUT (H)
13 IF INPUT (L)
12 ZENER OUTPUT REGULATOR
11 VCC
10 IF AMPLIFIER OUTPUT
9 LC RESONATOR
8 AUDIO OUTPUT

ORDER PART NO.

TBA120SN (DIP), TBA120ASN (QUAD-IN-LINE)

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	18	V
Operating temperature range	-15 to +70	°C
Storage temperature	-40 to +125	°C
Power dissipation	400	mW
max 1 minute	500	mW
Supply current	15	mA
max 1 minute	20	mA
Current 13	1	mA
14	1	mA
Operating supply voltage	6 to 18	V
Frequency range	0 to 12	MHz

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 12V; T_{amb} = 25°C)

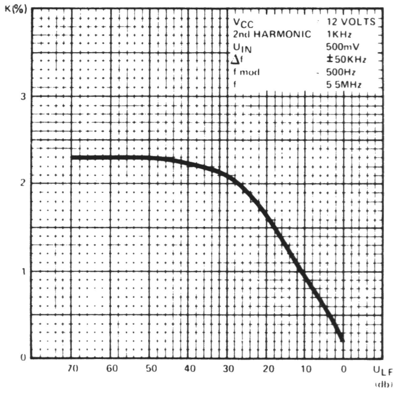
PARAMETER		TEST CONDITIONS	TBA120S			UNIT
			Min	Typ	Max	
I_{CC}	Total current requirement	$R_5 = \infty$	10	14	18	mA
		$R_5 = 0$	12	16	20	mA
V_8	dc-portion of the output signal	$V_1 = 0$		7.3		V
V_5	Voltage	-1dB down		2.4	2.6	V
		-70dB down		1.3		V

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 12V unless otherwise specified.

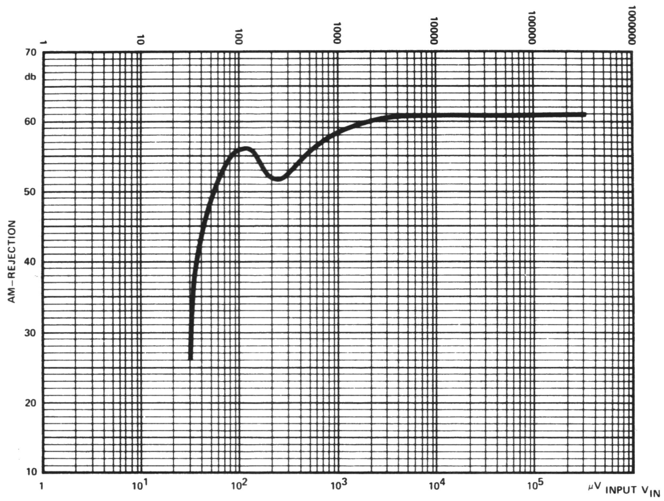
PARAMETER		TEST CONDITIONS	TBA120S			UNIT
			Min	Typ	Max	
G_V	IF-voltage gain V_6/V_{14}	f = 5.5MHz		68		dB
V_{QPP}	IF-output voltage at limiting; each output			250		mV
V_{AFrms}	AF-output voltage	f = 5.5MHz; $\Delta f = \pm 50$kHz; V_I = 10mV; f_{mod} = 1kHz; Q = 45; k = 4%		1.1		V
		f = 5.5MHz; $\Delta f = \pm 50$kHz; V_I = 10mV; f_{mod} = 1kHz; Q = 20; k = 1%		0.55		V
V_{lim}	Input voltage starting limiting	f = 5.5MHz; f = 50kHz; f_{mod} = 1kHz; Q = 45;		30	60	μV
Z_I	Input impedance	f = 5.5MHz	15/6	40/4.5		kΩ/pf
R_Q	Output resistance	Pin 8		2.6		kΩ
V_{AFmax} V_{AFmin}	Range of volume control			70		dB
a_{AM}	AM-suppression	f = 5.5MHz; f = +50Hz; V_I = 500μV; f_{mod} = 1kHz; m = 30%	45	55		dB
R_5	Potentiometer resistance	-1dB down		3.7	4.7	kΩ
		-70dB down	1.0	1.4		kΩ
CHARACTERISTICS OF THE AUXILIARY CIRCUIT						
V_{12}	Z-voltage	I_{12} = 5mA	11.2	12	13.2	V
R_Z	Z-resistance			30		Ω
$V_{CEO\ T43}$	Breakdown voltage	$I_4 = 0$; I_3 = 500μA	13			
h_{FE}	Current gain	I_3 = 1mA	30	120		V

TYPICAL PERFORMANCE CHARACTERISTICS

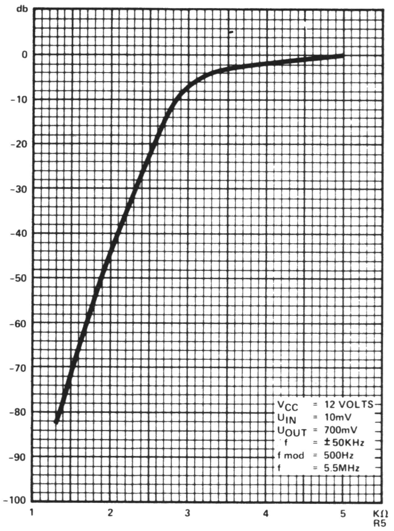
TYPICAL CURVE FROM PRODUCT SELECTION NR3.



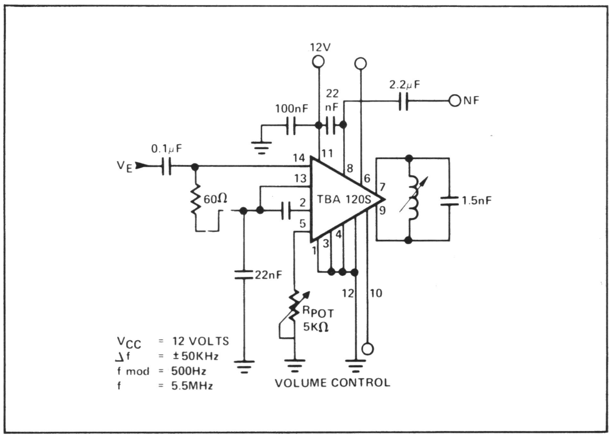
TYPICAL CURVE FROM PRODUCE-REFLECTION NR3.



VOLUME CONTROL SIGNETICS TBA120S



TEST CIRCUIT


12V
22
nF
2.2μF
NF
100nF
0.1μF
V_E
14
11
8
6
13
TBA 120S
7
60Ω
2
9
5
3
4
1
22nF
12
10
R_{POT}
5KΩ
VOLUME CONTROL
1.5nF
V_{CC} = 12 VOLTS
Δf = ±50KHz
f mod = 500Hz
f = 5.5MHz

TV VIDEO AMPLIFIER WITH DEMODULATOR — TBA1441

TBA1441-N

DESCRIPTION

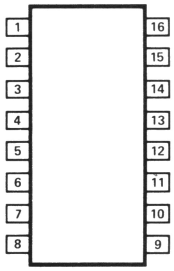
The TBA1441 (for npn tuner pre-stages) has been developed from the TBA440P/N. Improvements are as follows:

- Reduced residual IF at outputs 11 and 12
- Reduced residual IF at pin 13
- Considerably improved intermodulation distance
- Excellent tuning attitude even with low-ohmic tank circuit at demodulator

The IC's contain a high-amplifying controllable video IF amplifier, a controlled demodulator and two low-resistance video outputs with positive- and negative-going signals as well as the complete keyed control and delayed tuner control.

- Large control range with low noise and wide dynamic range
- High sensitivity
- Controlled demodulator, so minimum 1.07MHz disturbances
- Internal temperature stabilization
- The white levels of the video signals at the positive and negative video output are independent of the operating voltage
- The white and black levels can be adjusted separately

N PACKAGE



ORDER PART NO.
TBA1441N

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{13}	Supply voltage	15*	V
V_4	Voltages	5	V
V_5		20	V
V_{14}		5	V
R_{8-9}	Ohmic resistance between pins 8 and 9	≤ 20	Ω
R_{THSA}	Thermal resistance (system-air)	100	K/W
T_J	Junction temperature	150	°C
T_S	Storage temperature	-40 to +125	°C
V_{13}	Supply voltage range	10.5 to 15	V
T_A	Ambient temperature in operation	-25 to +60	°C

*NOTE
Briefly 16.5V

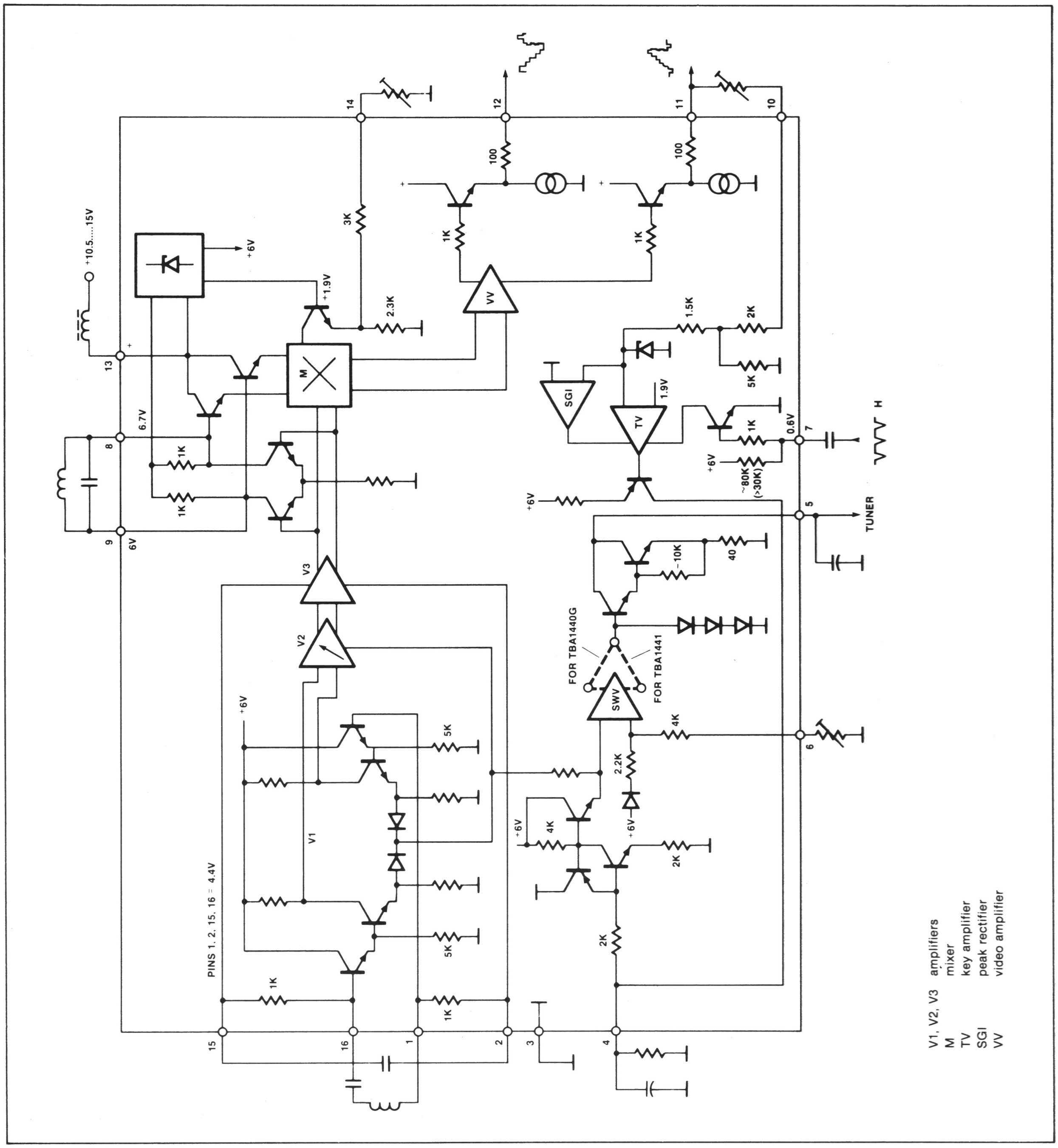
DC ELECTRICAL CHARACTERISTICS

$V_{13} = 13V$, $f_{IIF} = 38.9MHz$; $T_A = 25°C$; all data with reference to ground, unless otherwise specified.

PARAMETER		TEST CONDITIONS	TBA 1441			UNIT
			Min	Typ	Max	
I_{13}	Current consumption	$V_{13} = 15V$	34	47	60	mA
V_{11}	DC voltage at output 11	$V_{13} = 15V$; $V_1 = 0$				
		$R_{14-3} = \infty$		5.5		V
		$R_{14-3} = 0$		9.6		V
V_{12}	DC voltage at output 12	$V_{13} = 15V$; $V_1 = 0$				
		$R_{14-3} = \infty$		1.9		V
		$R_{14-3} = 0$		3.5		V
$V_{10} = V_{11}$	AGC threshold	V_{10} = sync pulse level for $R_{10-11} = 0$		1.9		V
V_{11sync}	Sync pulse level with async or without gating pulses	Peak level control		.5		V
V_4	IF control voltage	For max. gain	0		.5	V
		For min. gain	2.5		5	V
$-V_7$	Gating pulse voltage		2		5	V
I_{11}; I_{12}	Output current	To ground			5	mA
		TO $+V_{13}$			-1	mA

NOTES
1. According to test circuit; V_1 = effective sync pulse level at 60Ω.
2. Test level a_{cc} = -3dB
a_{sc} = -20dB referring to picture carrier.

EQUIVALENT SCHEMATIC


+10.5....15V
+6V
+1.9V
3K
2.3K
1K
1K
100
100
VV
M
14
12
11
10
13
8
9
6.7V
6V
1K
1K
1.5K
2K
5K
SGI
TV
1.9V
1K
0.6V
7
+6V
~80K (>30K)
H
+6V
5
TUNER
10K
40
FOR TBA1440G
FOR TBA1441
SWV
4K
6
2.2K
+6V
4K
+6V
2K
2K
V3
V2
V1
+6V
5K
5K
1K
1K
PINS 1, 2, 15, 16 = 4.4V
15
16
1
2
3
4
V1, V2, V3 amplifiers
M mixer
TV key amplifier
SGI peak rectifier
VV video amplifier

AC ELECTRICAL CHARACTERISTICS

(V_{13} = 13V; f_{IIF} = 38.9MHz; T_A = 25°C; all data with reference to ground, unless otherwise specified.

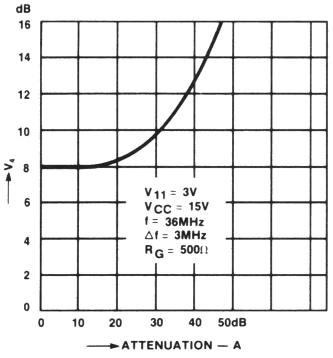
PARAMETER		TEST CONDITIONS	TBA1441			UNIT
			Min	Typ	Max	
$\Delta V_{11}/\Delta V_{13}$ $\Delta V_{12}/\Delta V_{13}$	White level deviation			100 20		mV/V mV/V
R_{14-3} R_{10-11}	Resistance for ΔV_{11} = 1V Resistance for sync pulse level deviation of 1V			8.5 2.4		kΩ kΩ
I_5	Control current for tuner prestage	$V_5 > 2V$ TBA1440G: 10dB after AGC TBA1441: 10dB previous to AGC	10	15		mA
V_{11}; V_{12}	Residual IF (basic frequency)			10		mV
Z_{1-16}	Input impedance	At max. gain At min. gain		1.8/2 1.9/0		kΩ/pF kΩ/pF
V_1 B_{video}	Input voltage[1] Video band width	$V_{11} = 3V_{PP}$ -3dB	70 6	100 7	300	μV MHz
ΔG_v a $Z_{q\ 8-9}$	AGC range Intermodulation with reference color carrier[2] Output impedance			55 45 2/2.5		dB dB kΩ/pF

NOTES

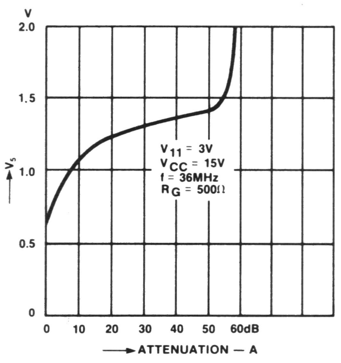
1. According to test circuit; V_1 = effective sync pulse level at 60Ω.
2. Test level a_{cc} = -3dB
   a_{sc} = -20dB referring to picture carrier.

TYPICAL PERFORMANCE CHARACTERISTICS

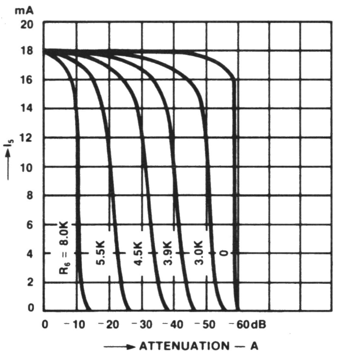
NOISE FIGURE vs ATTENUATION (MEASURED AD VIDEO FREQUENCY)
$-V_{fb}$ = 3V, V_{CC} = 15V, f = 36MHz, Δf = 3MHz, R_G = 500Ω



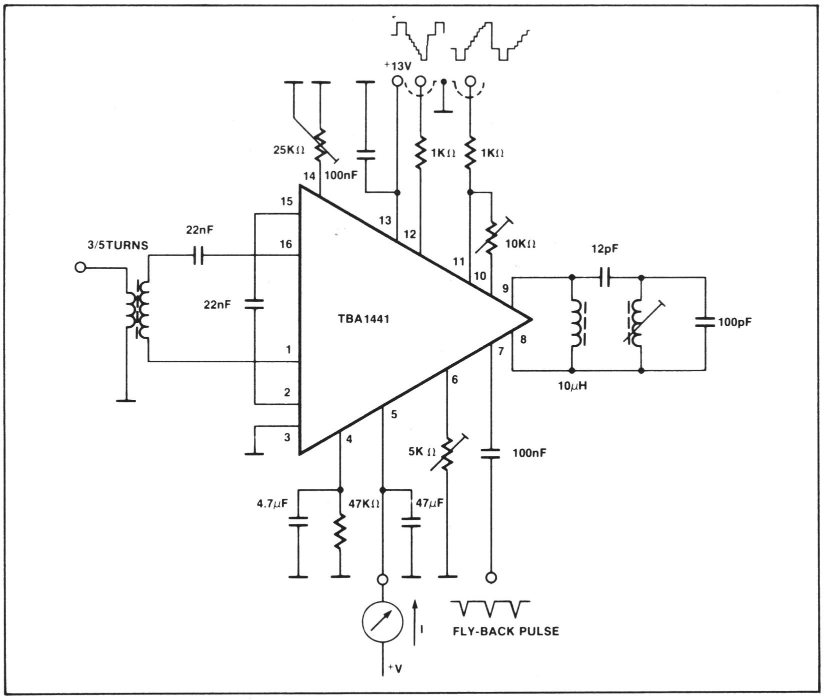
CONTROL VOLTAGE vs ATTENUATION
$-V_{fb}$ = 3V, V_{CC} = 15V, f = 36MHz, RG = 500Ω



TUNER CONTROL CURRENT vs ATTENUATION
R_G = PARAMETER
TBA1441



TEST CIRCUIT


+13V
25KΩ
14
100nF
1KΩ
1KΩ
15
13
12
10KΩ
11
10
9
12pF
3/5TURNS
22nF
16
22nF
TBA1441
100pF
1
8
7
10μH
2
6
5
3
4
5K Ω
100nF
4.7μF
47KΩ
47μF
I
FLY-BACK PULSE
+V

VIDEO IF SYSTEM — TDA 2541

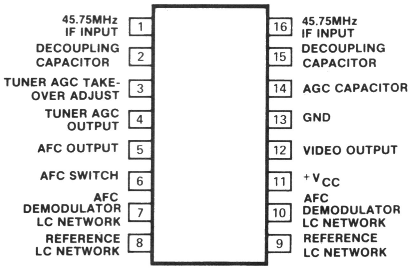
TDA2541-N

FEATURES

- Performs all video IF functions
- Provides 63dB IF AGC range
- Tuner AGC output
- Black and white noise inverting circuits
- AFC output
- High input sensitivity—100μV typical
- 53dB S/N ratio at 40dB gain control
- Minimal external components and adjustments required
- Switch disabling of video to allow direct video interface with VTR

PIN CONFIGURATION

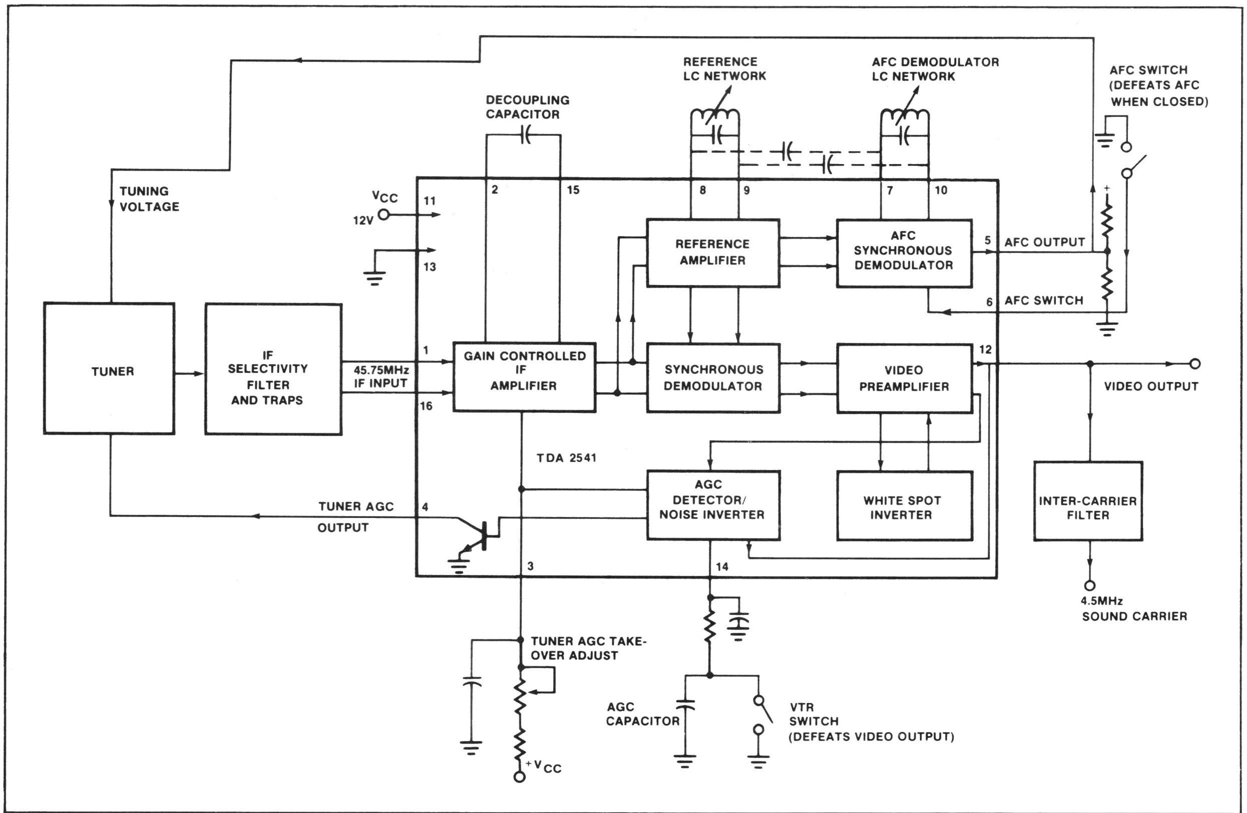
N PACKAGE



45.75MHz IF INPUT 1
DECOUPLING CAPACITOR 2
TUNER AGC TAKE-OVER ADJUST 3
TUNER AGC OUTPUT 4
AFC OUTPUT 5
AFC SWITCH 6
AFC DEMODULATOR LC NETWORK 7
REFERENCE LC NETWORK 8
16 45.75MHz IF INPUT
15 DECOUPLING CAPACITOR
14 AGC CAPACITOR
13 GND
12 VIDEO OUTPUT
11 +VCC
10 AFC DEMODULATOR LC NETWORK
9 REFERENCE LC NETWORK

ORDER PART NO.
TDA2541N

SIMPLIFIED BLOCK DIAGRAM



REFERENCE LC NETWORK
AFC DEMODULATOR LC NETWORK
AFC SWITCH (DEFEATS AFC WHEN CLOSED)
DECOUPLING CAPACITOR
TUNING VOLTAGE
VCC
12V
2
15
8
9
7
10
11
13
REFERENCE AMPLIFIER
AFC SYNCHRONOUS DEMODULATOR
5
AFC OUTPUT
6
AFC SWITCH
TUNER
IF SELECTIVITY FILTER AND TRAPS
45.75MHz IF INPUT
1
16
GAIN CONTROLLED IF AMPLIFIER
SYNCHRONOUS DEMODULATOR
VIDEO PREAMPLIFIER
12
VIDEO OUTPUT
TDA 2541
AGC DETECTOR/ NOISE INVERTER
WHITE SPOT INVERTER
INTER-CARRIER FILTER
TUNER AGC OUTPUT
4
3
14
4.5MHz SOUND CARRIER
TUNER AGC TAKE-OVER ADJUST
+VCC
AGC CAPACITOR
VTR SWITCH (DEFEATS VIDEO OUTPUT)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage V_{CC}	14	V
Supply current (V_{CC} = 14V)	75	mA
Power dissipation (V_{CC} = 14V)	1.0	W
Operating temperature	0 to +70	°C
Storage temperature	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = 12V$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	TDA 2541			UNIT
			Min	Typ	Max	
I_{CC}	Supply current		37		67	mA
$V_{th(AFC)}$	AFC switched off below			2.5		V
I_5	AFC symmetry	$V_i = 0$, $V_{14} = 0$	-40		+40	μA
$V_{th(VTR)}$	VTR switch switches off below			1.1		V
V_{WS}	White spot inverter threshold level			6.6		V
$V_{D(WS)}$	White spot inversion clamping level			4.6		V
V_N	Noise inverter threshold level			1.8		V
$V_{O(N)}$	Noise inversion clamping level			3.8		V
I_4	Tuner AGC output ON current		10			mA
$V_{4(SAT)}$	Tuner AGC output voltage	I_4 = 10mA			300	mV
I_4	Tuner AGC output OFF current				10	μA

AC ELECTRICAL CHARACTERISTICS

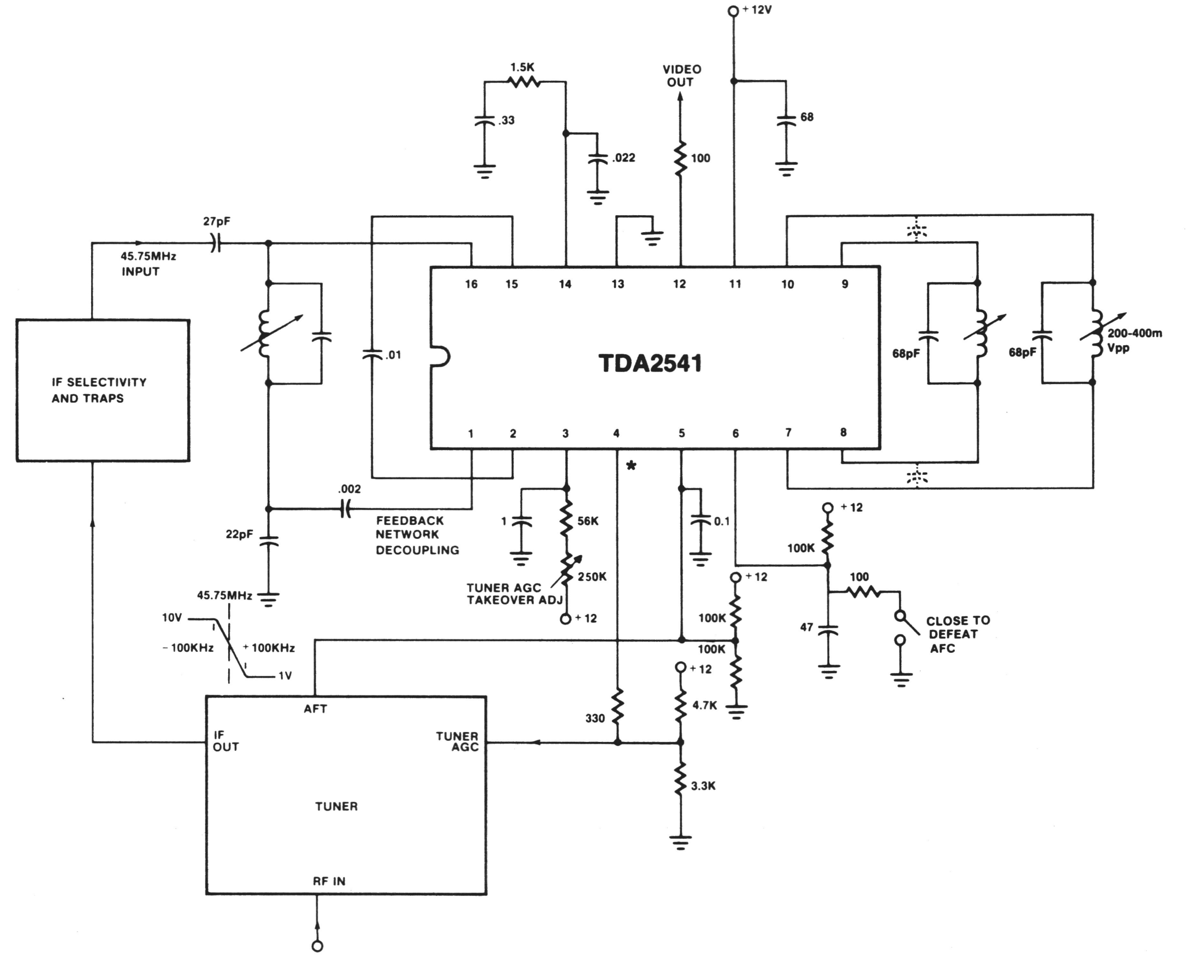
$T_A = 25°C$, $V_{CC} = 12V$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	TDA 2541			UNIT
			Min	Typ	Max	
V_i	IF input voltage for onset of AGC (f = 45.75MHz)		70	100	140	μV
$V_{O(Z)}$	Zero signal output level		5.7	6	6.3	V
$V_{O(TS)}$	Top sync level		2.9	3	3.2	V
V_5	AFC output voltage swing			10		V
ΔV_i	IF gain control range		50	63		dB
S/N	S/N at V_i = 10mV[1]			58		dB
B	3dB bandwidth of video amplifier			6		MHz
dG	Differential gain[2]			4	10	%
d0	Differential phase[2]			3°	10°	
	Intermodulation (1.1MHz)[3]	1.1MHz blue	46	60		dB
		1.1MHz yellow	46	50		dB
	Intermodulation (3.3MHz)[4]	3.3MHz	46	54		dB
	Carrier signal at video output			4	30	mV
	2nd harmonic of carrier at video output			20		mV
Δf	Change of frequency for 10V AFC swing			100	200	kHz

NOTES

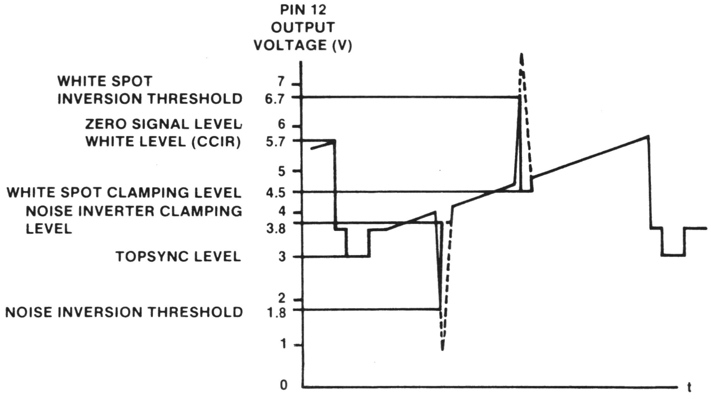
1. $S/N = \frac{V_O \text{ black to white}}{V \text{ noise r.m.s. } B = 5MHz}$
2. Measured with the VZM-2 test set-up of Wandel & Goltermann or equivalent. Measured between 10 and 75% of topsync level.
3. Intermodulation 1.1MHz $= 20 \log \left(\frac{V_O \text{ B-W}}{V_O \text{ p-p } 1.1MHz}\right)$ dB $= 20 \log \left(\frac{V_O \text{ } 4.4MHz}{V_O \text{ } 1.1MHz}\right) + 3.6dB$
4. Intermodulation 3.3MHz $= 20 \log \left(\frac{V_O \text{ } 4.4MHz}{V_O \text{ } 3.3MHz}\right)$ dB

TYPICAL APPLICATION


+12V
1.5K
.33
.022
VIDEO OUT
100
68
27pF
45.75MHz INPUT
IF SELECTIVITY AND TRAPS
.01
16
15
14
13
12
11
10
9
TDA2541
1
2
3
4
5
6
7
8
68pF
68pF
200-400m Vpp
.002
FEEDBACK NETWORK DECOUPLING
22pF
45.75MHz
10V
−100KHz
+100KHz
1V
1
56K
250K
TUNER AGC TAKEOVER ADJ
+12
*
0.1
+12
100K
100
47
CLOSE TO DEFEAT AFC
+12
100K
100K
+12
4.7K
330
3.3K
AFT
IF OUT
TUNER AGC
TUNER
RF IN

*Open NPN collector 10mA maximum

TDA2541 VIDEO OUTPUT



SECTION 13
GENERAL CONSUMER

Section 13—GENERAL CONSUMER

NE544 Servo Amplifier 295
NE644 Servo Amplifier 295

NOTE
*Any product listed in this section but not incorporated within the text may be obtained by writing Information Services at Signetics, 811 E. Arques, M/S 027, Sunnyvale, California 94086, or by calling (408) 746-1682.

SERVO AMPLIFIER

NE544/644

NE544/644-N,W

DESCRIPTION

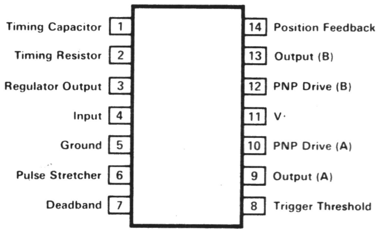
The NE544 is a servo amplifier and pulse-width demodulator with internal motor drive transistors. It is designed for remote control applications in digital proportional systems but can be used in many other closed loop position control applications. It incorporates a linear one shot for improved positional accuracy and outputs for external pnp motor drive transistors.

FEATURES

- **500mA load current capability**
- **Bidirectional bridge output with single power supply**
- **Low standby power drain**
- **Adjustable deadband and trigger thresholds**
- **High linearity, 0.5% maximum error**
- **Output drive for external PNP transistors (optional)**
- **Wide supply voltage range**

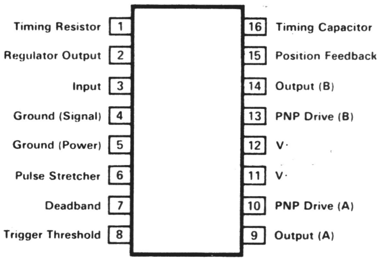
PIN CONFIGURATIONS

N PACKAGE


Timing Capacitor 1
Timing Resistor 2
Regulator Output 3
Input 4
Ground 5
Pulse Stretcher 6
Deadband 7
14 Position Feedback
13 Output (B)
12 PNP Drive (B)
11 V+
10 PNP Drive (A)
9 Output (A)
8 Trigger Threshold

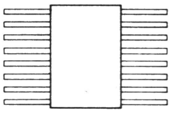
Order part no. NE544N

N PACKAGE


Timing Resistor 1
Regulator Output 2
Input 3
Ground (Signal) 4
Ground (Power) 5
Pulse Stretcher 6
Deadband 7
Trigger Threshold 8
16 Timing Capacitor
15 Position Feedback
14 Output (B)
13 PNP Drive (B)
12 V+
11 V+
10 PNP Drive (A)
9 Output (A)

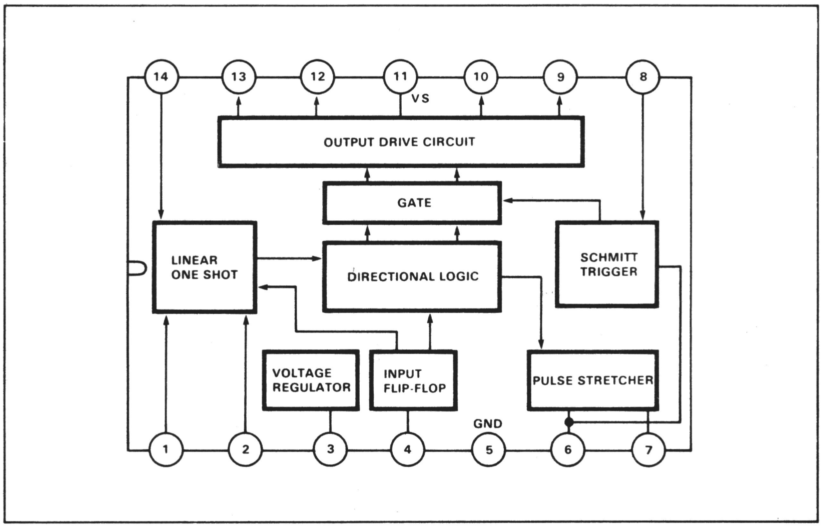
Order part no. NE644N

W PACKAGE*



*Pinout same as 644N package
Order part no. NE644W

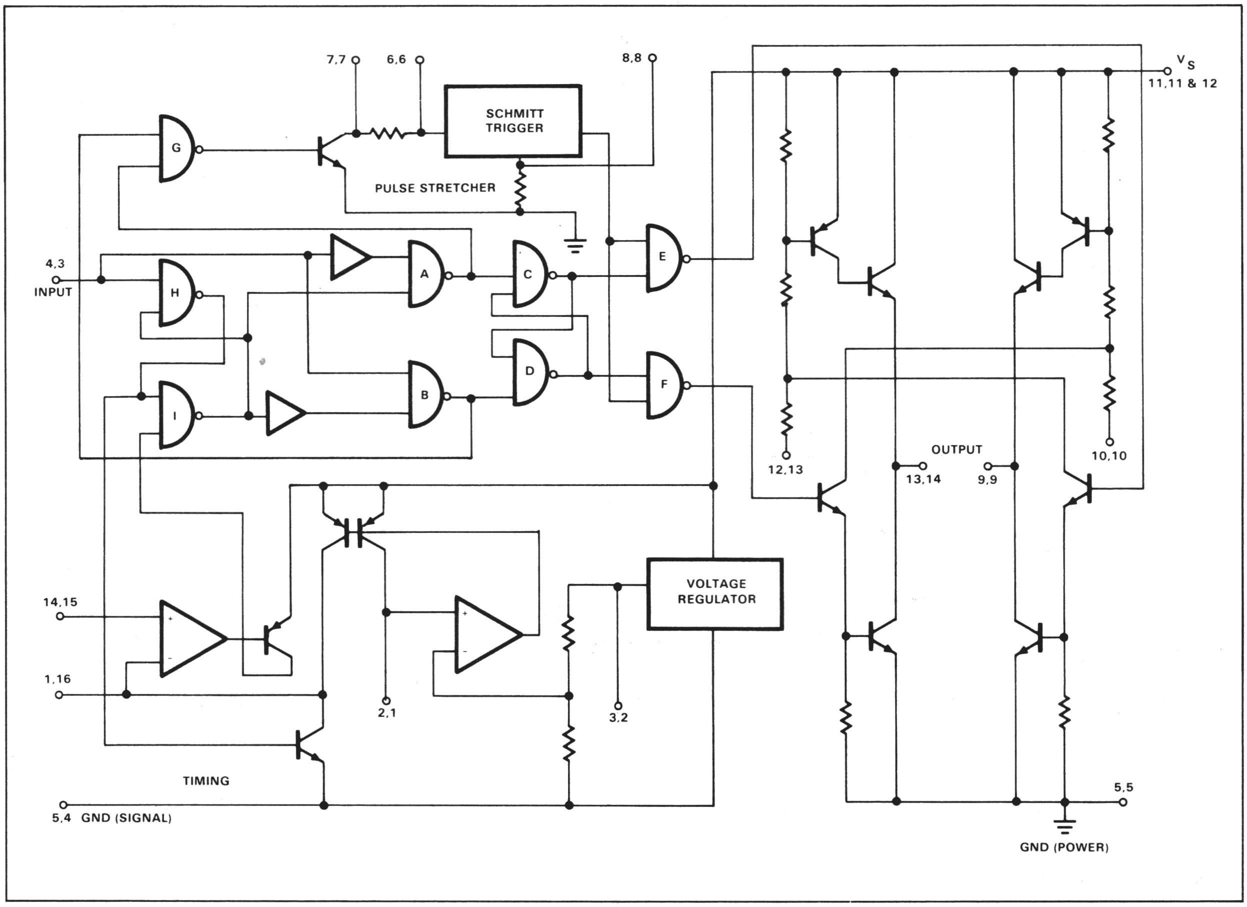
BLOCK DIAGRAM


14
13
12
11
VS
10
9
8
OUTPUT DRIVE CIRCUIT
GATE
LINEAR ONE SHOT
DIRECTIONAL LOGIC
SCHMITT TRIGGER
VOLTAGE REGULATOR
INPUT FLIP-FLOP
PULSE STRETCHER
GND
1
2
3
4
5
6
7

ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise specified.

PARAMETER		RATING	UNIT
$V+$	Supply voltage	6.0	V
I_O	Output current	500	mA
T_A	Operating temperature	-20 to +75	°C
T_{stg}	Storage temperature	-65 to +150	°C

EQUIVALENT CIRCUIT SCHEMATIC

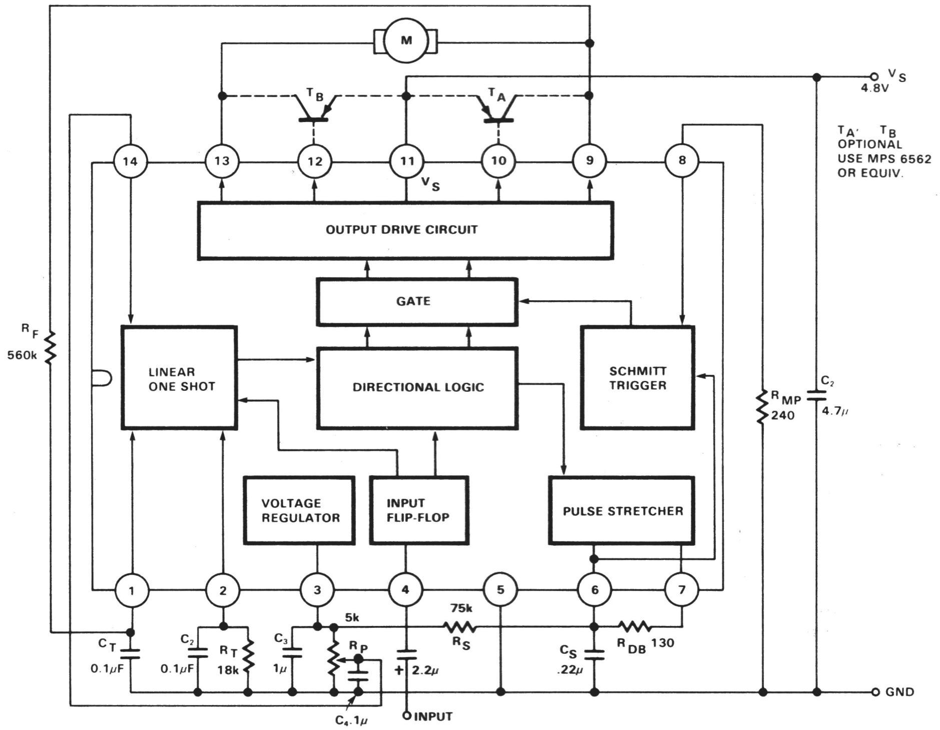

7,7
6,6
8,8
SCHMITT TRIGGER
PULSE STRETCHER
G
H
I
A
B
C
D
E
F
4,3
INPUT
14,15
1,16
2,1
3,2
VOLTAGE REGULATOR
TIMING
5,4 GND (SIGNAL)
V_S
11,11 & 12
12,13
OUTPUT
13,14
9,9
10,10
5,5
GND (POWER)

DC ELECTRICAL CHARACTERISTICS

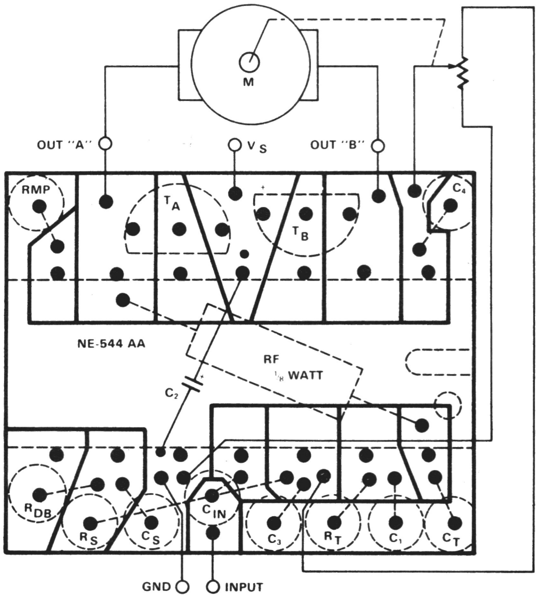
$T_A = 25°C$, $V_S = 4.8V$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		3.2	4.8	6	V
I_{CC}	Supply current	Quiescent	4.2	5.5	7.3	mA
V_{TH}	Input threshold					V
	On			1.5		
	Off			1.4		
Z_{IN}	Input resistance			18		kΩ
	Output voltage					V
V_{OL}	Low	Pin 9 or 13, I_L = 400mA		0.3		
V_{OH}	High			3.9		
V_R	Reference voltage		2.4	2.5	2.7	V
PSRR	Power supply rejection	$3.5V \leq V_S \leq 6V$		.01		%/V
	Minimum dead band	RDB = 0		1		μs
	One shot temperature coefficient			.01		%/°C
	Standby power			27		mW
	PNP drive current	Pin 10 and 12		20		mA

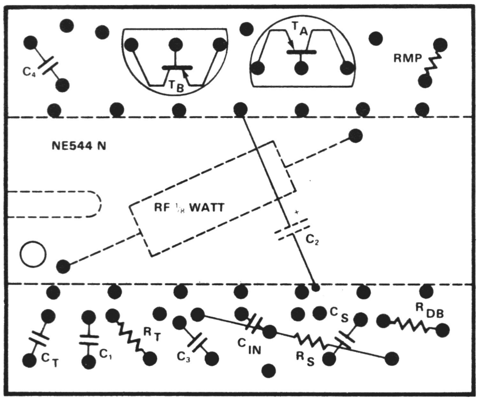
TYPICAL CONNECTION OF NE544N FOR LINEAR ONE SHOT TIMING


M
TB
TA
VS
4.8V
TA, TB OPTIONAL USE MPS 6562 OR EQUIV.
14
13
12
11
10
9
8
VS
OUTPUT DRIVE CIRCUIT
GATE
RF
560k
LINEAR ONE SHOT
DIRECTIONAL LOGIC
SCHMITT TRIGGER
RMP
240
C2
4.7μ
VOLTAGE REGULATOR
INPUT FLIP-FLOP
PULSE STRETCHER
1
2
3
4
5
6
7
5k
75k
RS
CT
0.1μF
C2
0.1μF
RT
18k
C3
1μ
RP
C4 .1μ
2.2μ
INPUT
CS
.22μ
RDB 130
GND

PC BOARD—N PACKAGE

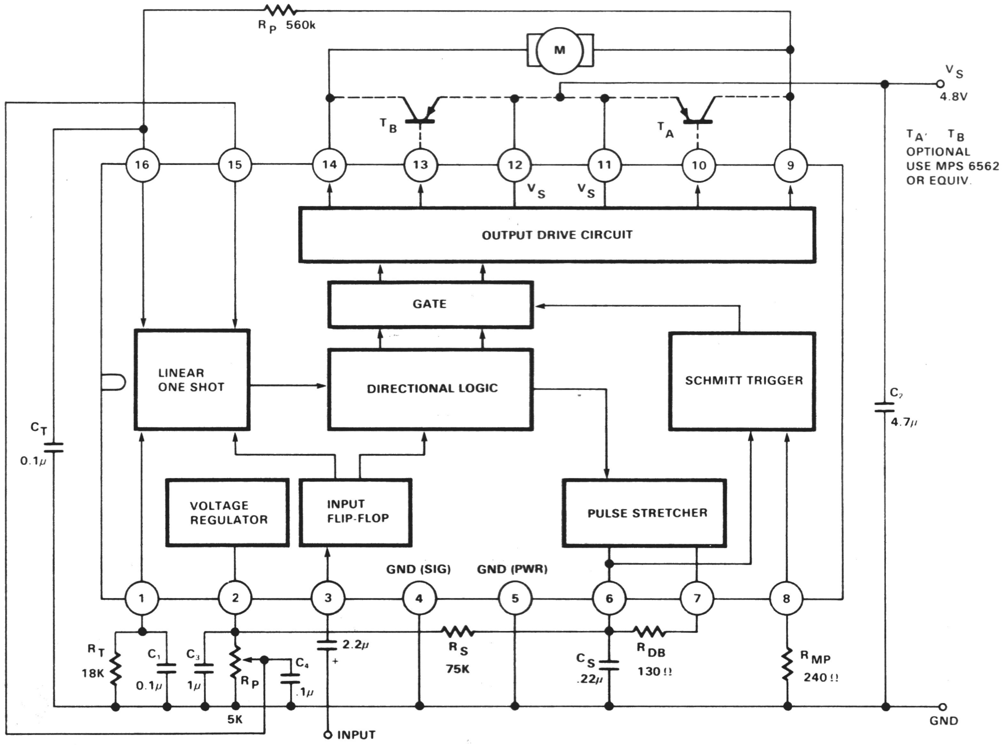

M
OUT "A"
V S
OUT "B"
RMP
C4
TA
TB
NE-544 AA
RF
1/8 WATT
C2
RDB
RS
CS
CIN
C3
RT
C1
CT
GND
INPUT

Typical PC Board Layout
Bottom View—4X


C4
TB
TA
RMP
NE544 N
RF 1/8 WATT
C2
CT
C1
RT
C3
CIN
CS
RS
RDB

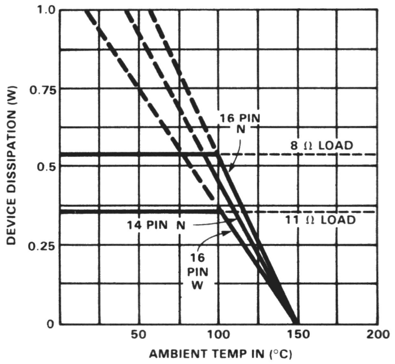
Parts Layout
Top View

TYPICAL CONNECTION OF NE644W AND NE644N FOR LINEAR ONE SHOT TIMING

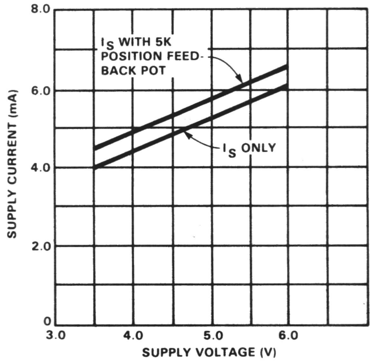

R_P 560k
M
V_S
4.8V
T_B
T_A
T_A, T_B
OPTIONAL
USE MPS 6562
OR EQUIV.
16
15
14
13
12
11
10
9
V_S
V_S
OUTPUT DRIVE CIRCUIT
GATE
LINEAR ONE SHOT
DIRECTIONAL LOGIC
SCHMITT TRIGGER
C_T
0.1μ
C_7
4.7μ
VOLTAGE REGULATOR
INPUT FLIP-FLOP
PULSE STRETCHER
GND (SIG)
GND (PWR)
1
2
3
4
5
6
7
8
R_T
18K
C_1
0.1μ
C_3
1μ
R_P
5K
C_4
.1μ
2.2μ
+
INPUT
R_S
75K
C_S
.22μ
R_{DB}
130Ω
R_{MP}
240Ω
GND

TYPICAL PERFORMANCE CHARACTERISTICS

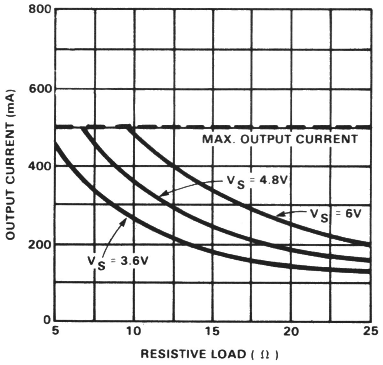
MAXIMUM DISSIPATION vs AMBIENT TEMPERATURE



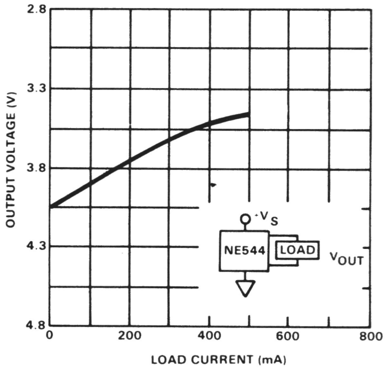
SUPPLY CURRENT vs SUPPLY VOLTAGE



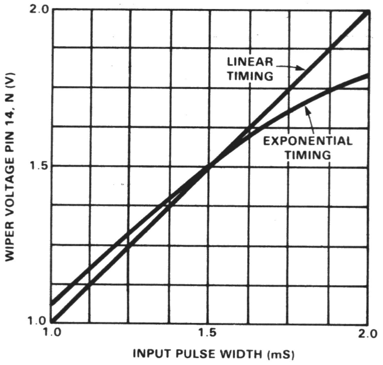
OUTPUT CURRENT vs LOAD RESISTANCE



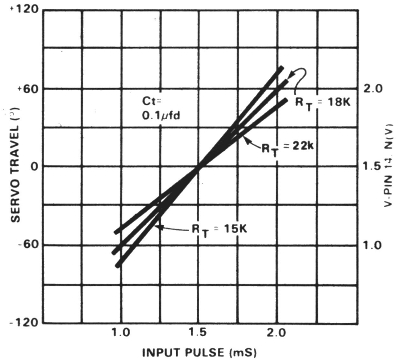
OUTPUT VOLTAGE vs LOAD CURRENT



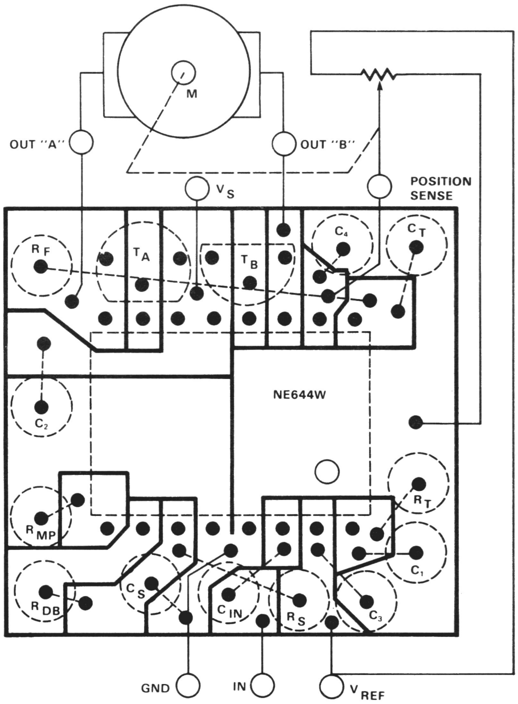
INPUT PULSE WIDTH vs FEEDBACK POT OUTPUT



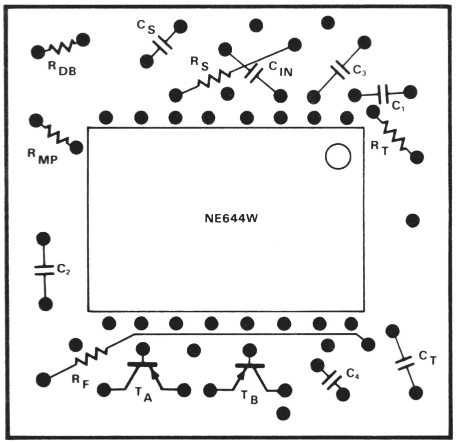
INPUT PULSE vs SERVO TRAVEL



PC BOARD—W PACKAGE


M
OUT "A"
OUT "B"
V_S
POSITION SENSE
R_F
T_A
T_B
C_4
C_T
C_2
NE644W
R_T
R_{MP}
C_1
R_{DB}
C_S
C_{IN}
R_S
C_3
GND
IN
V_{REF}

PC Board Layout
Bottom View—4X


R_{DB}
C_S
R_S
C_{IN}
C_3
C_1
R_{MP}
R_T
NE644W
C_2
R_F
T_A
T_B
C_4
C_T

Parts Layout
Top View

SECTION 14
PHASE LOCKED LOOPS

Section 14—PHASE LOCKED LOOPS

NE564	Phase Locked Loop	309
NE/SE565	Phase Locked Loop	316
NE/SE566	Function Generator	321
NE/SE567	Tone Decoder/Phase Locked Loop	324

NOTE

*Any product listed in this section but not incorporated within the text may be obtained by writing Information Services at Signetics, 811 E. Arques, M/S 027, Sunnyvale, California 94086, or by calling (408) 746-1682.

PHASE LOCKED LOOPS DEFINITIONS

T_A

Ambient temperature range. Range of the surrounding environment of the operating device.

T_J

Junction Temperature. The maximum temperature of the device. 150°C is standard for silicon devices.

T_{STG}

Storage temperature range. Temperature range that the device can be stored in a non-operating condition.

T_{SOLD}

Soldering Temperature. The temperature which can be applied to the lead frame of the device for short periods of time (normally specified for a duration of 10 sec).

Truth Tables

0 is logic level low
1 is logic level high
X - don't care condition - has no effect under circuit conditions listed.

Absolute Maximum Rating

Operating safe zones exceeding these limits could cause permanent damage to the device and are not meant to imply that devices can operate at these limits.

Power Dissipation

The power that the device can safely handle at 25°C. The dissipation must be derated as indicated for the individual package type.

Package Type Designation

See full package designations in Appendix.

V_{CC} $(-V_{CC})$

Supply Voltage. The range of power supply voltage over which the device will operate safely.

FREE-RUNNING FREQUENCY (f_o', ω_o').

Also called the *center frequency*, this is the frequency at which the loop VCO operates when not locked to an input signal. The "prime" superscripts are used to distinguish the free-running frequency from f_o' and ω_o' which are used for the general oscillator frequency. (Many references use f_o' and ω_o' for both the free-running and general oscillator frequency and leave the proper choice for the reader to infer from the context). The appropriate units for f_o' and ω_o' are Hz and radians per second respectively.

LOCK RANGE ($2f_L$, $2\omega_L$).*

The range of frequencies over which the loop will remain in lock. Normally the lock range is centered at the free-running frequency unless there is some nonlinearity in the system which limits the frequency deviation on one side of f_o'. The deviations from f_o' are referred to as the *Tracking Range* or *Hold-in Range.* (See figure 1.6). The tracking range is therefore one-half of the lock range.

CAPTURE RANGE ($2f_c$, $2\omega_c$).**

Although the loop will remain in lock throughout its lock range, it may not be able to acquire lock at the tracking range extremes because of the selectivity afforded by the low-pass filter. The capture range also is centered at f_o' with the equal deviations called the *Lock-in* or *Pull-in Ranges.* The capture range can never exceed the lock range.

LOCK-UP TIME (t_L).***

The transient time required for a free-running loop to lock. This time depends principally upon the bandwidth selectivity designed into the loop with the low-pass filter. The lock-up time is inversely proportional to the selectivity bandwidth. Also, lock-up time exhibits a statistical spreading due to random initial phase relationships between the input and oscillator phases.

PHASE COMPARATOR CONVERSION GAIN (K_d).

The conversion constant relating the phase comparators output voltage to the phase difference between input and VCO signals when the loop is locked. At low input signal levels, K_d is also a function of signal amplitude. K_d has units of volts per radian (V/rad).

VCO CONVERSION GAIN (K_o).

The conversion constant relating the oscillators frequency shift from f_o' to the applied input voltage. K_o has units of radians per second per volt (rad/sec/volt). K_o is a linear function of ω_o' and must be obtained using a formula or graph provided or experimentally measured at the desired ω_o'.

LOOP GAIN (K_v).

The product of K_d, K_o, and the low-pass filters gain at dc. K_d is evaluated at the appropriate input signal level and K_o at the appropriate ω_o'. K_v has units of $(\text{sec})^{-1}$.

CLOSED LOOP GAIN (CLG).

The output signal frequency and phase can be determined from a product of the CLG and the input signal where the CLG is given by

$$\text{CLG} = \frac{K_v}{1 + K_v} \qquad \text{(Equation 1.4)}$$

NATURAL FREQUENCY (ω_n).

The characteristic frequency of the loop, determined mathematically by the final pole positions in the complex plane or determined experimentally as the modulation frequency for which an underdamped loop gives the maximum frequency deviation from f_o' and at which the phase error swing is the greatest.

DAMPING FACTOR (ζ).

The standard damping constant of a second order feedback system. For the PLL, ζ refers to the ability of the loop to respond quickly to an input frequency step without excessive overshoot.

LOOP NOISE BANDWIDTH (B_L).

A loop property relating ω_n and τ which describes the effective bandwidth of the received signal. Noise and signal components outside this bandwidth are greatly attenuated.

* Also called Synchronization Range.
** Also called Acquisition Range.
*** Also called Acquisition Time.

NOTE
Refer to Section 10 of the 1979 Analog Applications Manual for an in-depth explanation of Phase Locked Loops and their applications.

SE/NE564-N,I

DESCRIPTION

The NE564 is a versatile, high frequency Phase Locked Loop designed for operation up to 50MHz. As shown in the block diagram, the NE564 consists of a VCO, limiter, phase comparator, and post detection processor.

APPLICATIONS

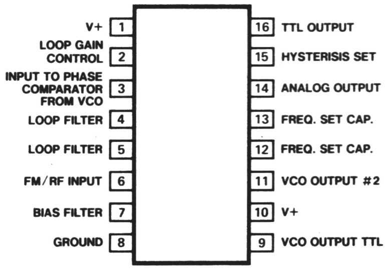
- **High speed modems**
- **FSK receivers and transmitters**
- **Frequency synthesizers**
- **Signal generators**

FEATURES

- **Operation with single 5V supply**
- **TTL compatible inputs and outputs**
- **Operation to 50MHz**
- **External loop gain control**
- **Reduced carrier feedthrough**
- **No elaborate filtering needed in FSK applications**
- **Can be used as a modulator**
- **Variable loop gain (Externally Controlled)**

PIN CONFIGURATION

I,N PACKAGE

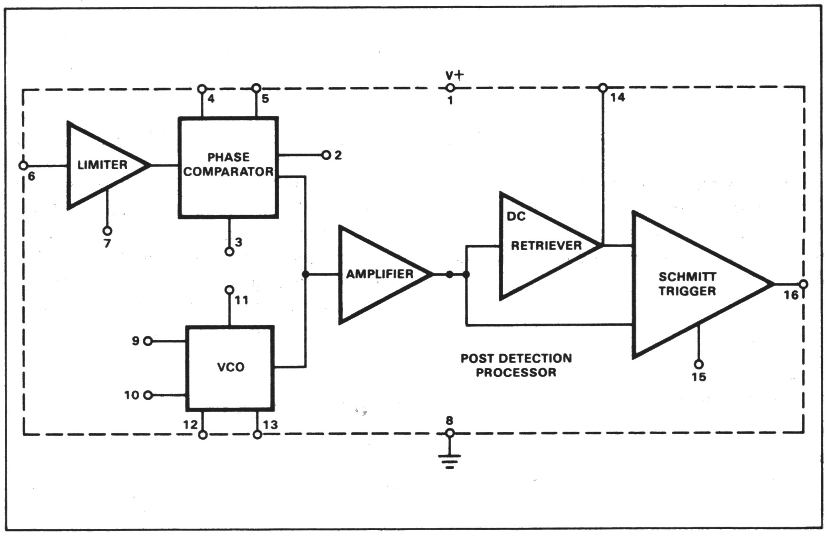

V+ 1
LOOP GAIN CONTROL 2
INPUT TO PHASE COMPARATOR FROM VCO 3
LOOP FILTER 4
LOOP FILTER 5
FM/RF INPUT 6
BIAS FILTER 7
GROUND 8
16 TTL OUTPUT
15 HYSTERISIS SET
14 ANALOG OUTPUT
13 FREQ. SET CAP.
12 FREQ. SET CAP.
11 VCO OUTPUT #2
10 V+
9 VCO OUTPUT TTL

ORDER PART NO.
SE/NE564

ABSOLUTE MAXIMUM RATINGS

PARAMETER			RATING	UNIT
V+	Supply voltage			V
	Pin 1		14	
	Pin 10		6	
P_D	Power dissipation		400	mW
T_A	Operating temperature	NE	0 to 70	°C
	Operating temperature	SE	−55 to +125	
t_{stg}	Storage temperature		−65 to 150	°C

BLOCK DIAGRAM


V+
1
4
5
14
LIMITER
PHASE COMPARATOR
2
6
7
3
AMPLIFIER
DC RETRIEVER
SCHMITT TRIGGER
16
11
9
VCO
10
12
13
8
15
POST DETECTION PROCESSOR

FUNCTIONAL DESCRIPTION

The NE564 is a monolithic phase locked loop with a post detection processor. The use of Schottky clamped transistors and optimized device geometries extends the frequency of operation to greater than 50MHz. In addition to the classical PLL applications, the NE564 can be used as a modulator with a controllable frequency deviation.

The output voltage of the PLL can be written as shown in the following equation:

$$V_O = \frac{(f_{in} - f_o)}{K_{vco}} \qquad \text{Equation 1}$$

K_{VCO} = conversion gain of the VCO (see figure 7)
f_{in} = frequency of the input signal
f_o = free running frequency of the VCO

The process of recovering FSK signals involves the conversion of the PLL output into logic compatible signals. For high data rates, a considerable amount of carrier will be present at the output of the PLL due to the wideband nature of the loop filter. To avoid the use of complicated filters, a comparator with hysterisis or Schmitt trigger is required. With the conversion gain of the VCO fixed, the output voltage as given by Equation 1 varies according to the frequency deviation of f_{in} from f_O. Since this differs from system to system, it is necessary that the hysterisis of the Schmitt trigger be capable of being changed, so that it can be optimized for a particular system. This is

ELECTRICAL CHARACTERISTICS

$V+ = 5V$, $T_A = 25°C$, $fo = 5MHz$, $I_B = -200\mu A$ unless otherwise specified.
Test Circuit: Figure 1

PARAMETER	TEST CONDITIONS	SE564			NE564			UNIT
		Min	Typ	Max	Min	Typ	Max	
Maximum VCO frequency		50	65		45	60		MHz
Lock range	Input ≥ 200mVrms, $T_A = 25°C$	60	90		60	90		% of fo
	$= 125°C$	30	50					
	$= -55°C$	120	150					
	$= 0°C$				100	120		
	$= 70°C$				50	70		
Capture range	Input ≥ 200mVrms, R2 = 27Ω	25	35		25	35		% of fo
	= 100Ω	35	50		35	50		
VCO frequency drift with temperature	fo = 5MHz, $T_A = -55°C$ to 125°C		400	1000				PPM/°C
	= 0°C to 70°C					400	1250	
	fo = 500kHz, $T_A = -55°C$ to 125°C		250	500				
	= 0°C to 70°C					400	850	
VCO frequency change with supply voltage	V+ = 4.5V to 5.5V		3	6		3	6	% of fo
Demodulated output voltage	Modulation frequency: 1kHz, fo = 5MHz							
	Input deviation: 10%, T = 25°C	120	140		120	140		mVrms
	: 1%, T = 25°C	12	14		12	14		mVrms
	T = 0°C				11	13		mVrms
	= −55°C	9	12					mVrms
	= 70°C				13	15		mVrms
	= 125°C	14	16					mVrms
Linearity	Deviation: 1% to 8%		1	3		1	3	%
Signal to noise ratio			40			40		dB
AM rejection			35			35		dB
Supply current	V+ = 5V		35	50		35	50	mA
Leakage current	Pin 9		1	10		1	10	µA
Output current	Pin 9			6			6	mA
Supply voltage	Pin 1	4.5		12	4.5		12	V
	Pin 10	4.5		5.5	4.5		5.5	V

accomplished in the 564 by varying the voltage at pin 15 which results in a change of the hysteresis of the Schmitt trigger.

For FSK signals, an important factor to be considered is the drift in the free running frequency of the VCO itself. If this changes due to temperature, according to Equation 1 it will lead to a change in the dc levels of the PLL output, and consequently to errors in the digital output signal. This is especially true for narrow band signals where the deviation in f_{in} itself may be less than the change in f_o due to temperature. This effect can be eliminated if the dc or average value of the signal is retrieved and used as the reference to the comparator. In this manner, variations in the dc levels of the PLL output do not affect the FSK output.

VCO Section

Due to its inherent high frequency performance, an emitter coupled oscillator is used in the VCO. In the circuit, shown in the equivalent schematic, transistors Q_{21} and Q_{23} with current sources $Q_{25}-Q_{26}$ form the basic oscillator. The free running frequency of the oscillator is shown in the following equation:

$$f_o = \frac{1}{16 R_c C_1} \qquad \text{Equation 2}$$

$R_c = R_{19} = R_{20} = 100\Omega$ (INTERNAL)
C_1 = external frequency setting capacitor

Variation of V_d (phase detector output voltage) changes the frequency of the oscillator. As indicated by Equation 2, the frequency of the oscillator has a negative temperature coefficient due to the positive temperature coefficient of the monolithic resistor. To compensate for this, a current I_R with negative temperature coefficient is introduced to achieve a low frequency drift with temperature.

Phase Comparator Section

The phase comparator consists of a double balanced modulator with a limiter amplifier to improve AM rejection. Schottky clamped vertical PNPs are used to obtain TTL level inputs. The loop gain can be varied by changing the current in Q_4 and Q_{15} which effectively changes the gain of the differential amplifiers. This can be accomplished by introducing a current at pin 2.

Post Detection Processor Section

The post detection processor consists of a unity gain transconductance amplifier and comparator. The amplifier can be used as a dc retriever for demodulation of FSK signals, and as a post detection filter for linear FM demodulation. The comparator has adjustable hysteresis so that phase jitter in the output signal can be eliminated.

As shown in the equivalent schematic, the dc retriever is formed by the transductance amplifier $Q_{42}-Q_{43}$ together with an external capacitor which is connected at the amplifier output (pin 14). This forms an integrator whose output voltage is shown in the following equation:

$$V_O = \frac{g_m}{C_2} V_{in}dt \qquad \text{Equation 3}$$

g_m = transconductance of the amplifier
C_2 = capacitor at the output (pin 14)
V_{in} = signal voltage at amplifier input

With proper selection of C_2, the integrator time constant can be varied so that the output voltage is the dc or average value of the input signal for use in FSK, or as a post detection filter in linear demodulation.

The comparator with hysterisis is made up of $Q_{49}-Q_{50}$ with positive feedback being provided by $Q_{47}-Q_{48}$. The hysterisis is varied by changing the current in Q_{52} with a resulting variation in the loop gain of the comparator. This method of hysterisis control, which is a dc control, provides symmetric variation around the nominal value.

Design Formula

The free running frequency of the VCO is shown by the following equation:

$$f_O = \frac{1}{16R_CC_1} \text{ in Hz} \qquad \text{Equation 4}$$

$R_C = 100\Omega$
C_1 = external cap in farads

The loop filter diagram shown is explained by the following equation:

$$F(s) = \frac{1}{1 + sRC_3} \qquad \text{Equation 5}$$

$R = R_{12} = R_{13} = 1.3k\Omega$ (INTERNAL)

By adding capacitors to pins 4 and 5, two poles are added to the loop transfer function at $\omega = \frac{1}{RC_3}$.

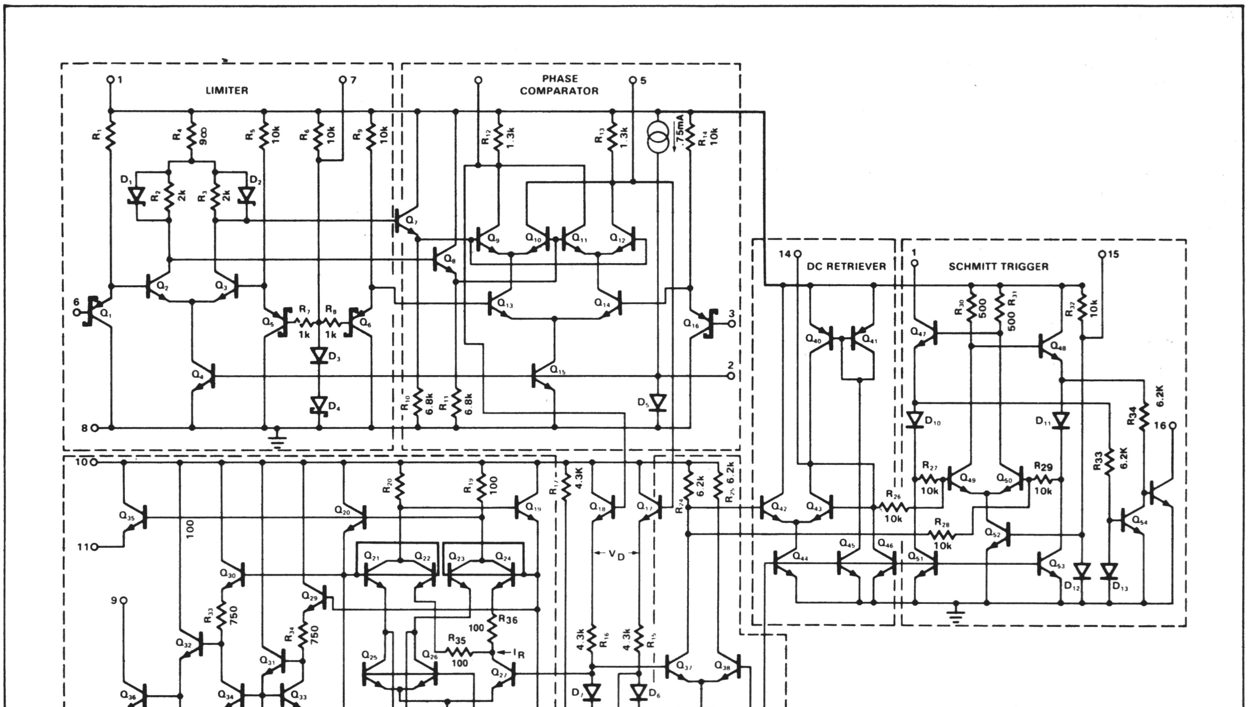
FM DEMODULATOR

The NE564 can be used as an FM demodulator. The connections for operation at 5V and 12V are shown in figures 2 and 3 respectively. The input signal is ac coupled with the output signal being extracted at pin 14. Loop filtering is provided by the capacitors at pins 4 and 5 with additional filtering being provided by the capacitor at pin 14. Since the conversion gain of the VCO is not very high, to obtain sufficient demodulated output signal the frequency deviation in the input signal should be fairly high (1% or higher).

MODULATION TECHNIQUES

The NE564 phase locked loop can be modulated at either the loop filter ports (pins 4 and 5) or the input port (pin 6) as shown in figure 4. The approximate modulation frequency can be determined from the frequency conversion gain curve shown in figure 5. This curve will be appropriate for signals injected into pins 4 and 5 as shown in figure 4.

EQUIVALENT SCHEMATIC


LIMITER
PHASE COMPARATOR
DC RETRIEVER
SCHMITT TRIGGER
VCO
AMPLIFIER
1
7
5
6
8
3
2
14
15
16
10
11
9
12
13
R1
R4 900
R5 10k
R6 10k
R9 10k
R2 2k
R3 2k
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
R7 1k
R8 1k
R12 1.3k
R13 1.3k
.75mA
R14 10k
R10 6.8k
R11 6.8k
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q26
Q27
Q28
Q29
Q30
Q31
Q32
Q33
Q34
Q35
Q36
Q37
Q38
Q39
Q40
Q41
Q42
Q43
Q44
Q45
Q46
Q47
Q48
Q49
Q50
Q51
Q52
Q53
Q54
R30 500
R31 500
R32 10k
R34 6.2K
R33 6.2K
R27 10k
R29 10k
R26 10k
R28 10k
R20
R19 100
R17 4.3K
R24 6.2k
R25 6.2k
100
R33 750
R34 750
R36 100
R35 100
IR
R16 4.3k
R15 4.3k
VD
R23 680
R22 10k
R21 2k
R18

FSK Demodulation

The 564 PLL is particularly attractive for FSK demodulation since it contains an internal voltage comparator and VCO which have TTL compatible inputs and outputs, and it can operate from a single 5 volt power supply. Demodulated dc voltages associated with the mark and space frequencies are recovered with a single external capacitor in a dc retriever without utilizing extensive filtering networks. An internal comparator, acting as a Schmitt trigger with an adjustable hysteresis, shapes the demodulated voltages into compatible TTL output levels. The high frequency design of the 564 enables it to demodulate FSK at high data rates in excess of 1.0M baud.

Figure 6 shows a high-frequency FSK decoder designed for input frequency deviations of ± 1.0MHz centered around a free-running frequency of 10.8MHz. The value of the timing capacitance required was estimated from figure 8 to be approximately 40pF. A trimmer capacitor was added to fine tune f_O' to 10.8MHz.

Figure 9 indicates that the ± 1.0MHz frequency deviations will be within the lock range for input signal levels greater than approximately 50mV with zero pin 2 bias current. While strictly this figure is appropriate only for 5MHz, it can be used as a guide for lock range estimates at other f_O' frequencies.

The hysteresis was adjusted experimentally via the 10kΩ potentiometer and 2kΩ bias arrangement to give the waveshape shown in figure 7 for 20K, 500K, 2M baud rates with square wave FSK modulation. Note the magnitude and phase relationships of the phase comparators output voltages with respect to each other and to the FSK output. The high frequency sum components of the input and VCO frequency also are visible as noise on the phase comparators outputs.

SE/NE 564 TEST CIRCUIT

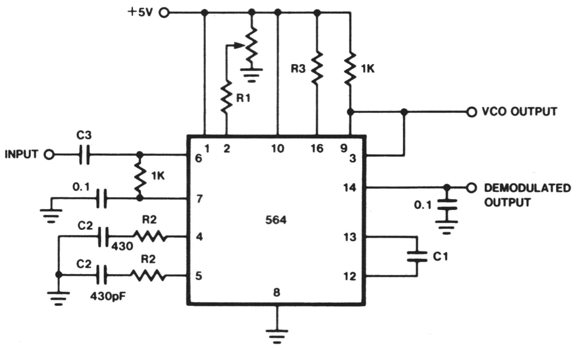

+5V
R1
R3
1K
VCO OUTPUT
INPUT
C3
1K
0.1
C2
430
R2
C2
430pF
R2
1
2
10
16
9
6
3
7
4
5
14
13
12
8
564
DEMODULATED OUTPUT
0.1
C1

Figure 1

FM DEMODULATOR AT 5V

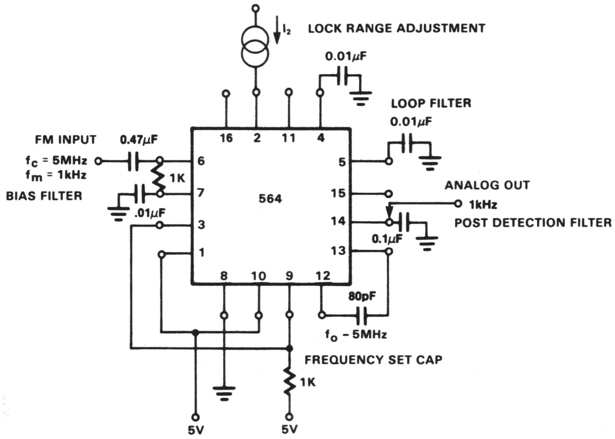

I₂
LOCK RANGE ADJUSTMENT
0.01µF
LOOP FILTER
0.01µF
FM INPUT
0.47µF
fc = 5MHz
fm = 1kHz
1K
BIAS FILTER
.01µF
16
2
11
4
6
7
3
1
5
15
14
13
8
10
9
12
564
ANALOG OUT
1kHz
POST DETECTION FILTER
0.1µF
80pF
fo - 5MHz
FREQUENCY SET CAP
1K
5V
5V

Figure 2

FM DEMODULATOR AT 12V

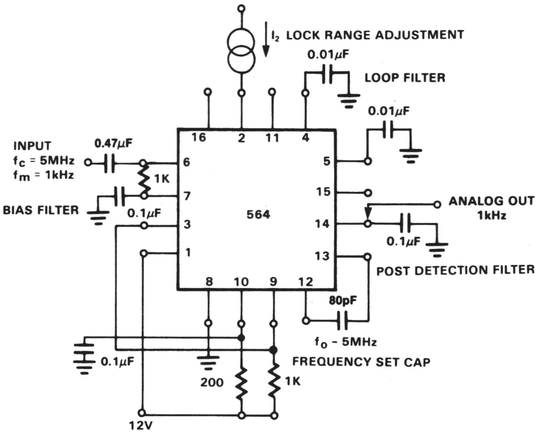

I₂ LOCK RANGE ADJUSTMENT
0.01μF
LOOP FILTER
0.01μF
INPUT
fc = 5MHz
fm = 1kHz
0.47μF
1K
BIAS FILTER
0.1μF
564
16
2
11
4
6
7
3
1
5
15
14
13
8
10
9
12
ANALOG OUT
1kHz
0.1μF
POST DETECTION FILTER
80pF
fo - 5MHz
FREQUENCY SET CAP
0.1μF
200
1K
12V

Figure 3

MODULATOR

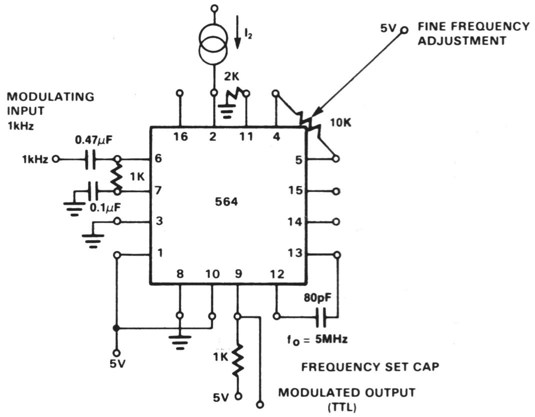
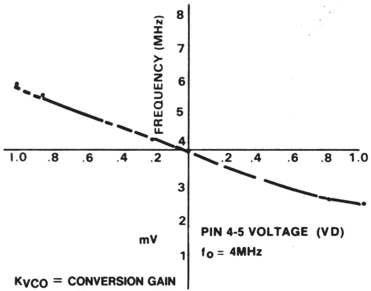

I₂
2K
5V
FINE FREQUENCY
ADJUSTMENT
10K
MODULATING
INPUT
1kHz
0.47μF
1kHz
1K
0.1μF
564
16
2
11
4
6
7
3
1
5
15
14
13
8
10
9
12
80pF
fo = 5MHz
5V
1K
5V
FREQUENCY SET CAP
MODULATED OUTPUT
(TTL)

Figure 4

VCO CONVERSION GAIN



K_{VCO} = CONVERSION GAIN

$$K_{VCO} = \frac{\Delta f}{\Delta V_D} \simeq -1.8 \frac{\text{MHz}}{\text{V}}$$

FOR K_O OF PLL MODEL

$$K_O = \frac{(\Delta f/fo)}{\text{VOLT}} = \frac{-(1.8\text{MHz}/4\text{MHz})}{1\text{VOLT}}$$

$$= \frac{-0.45\ \text{RADIANS}}{\text{VOLT}}$$

$$= -4.5 \times 10^{-4}\ \text{RADIANS/mV}$$

Figure 5

10.8MHz FSK DECODER USING THE 564

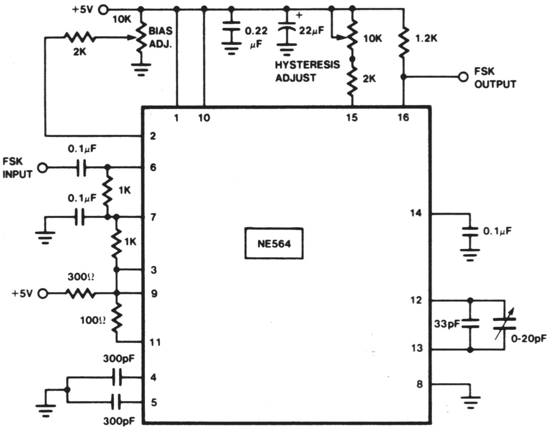
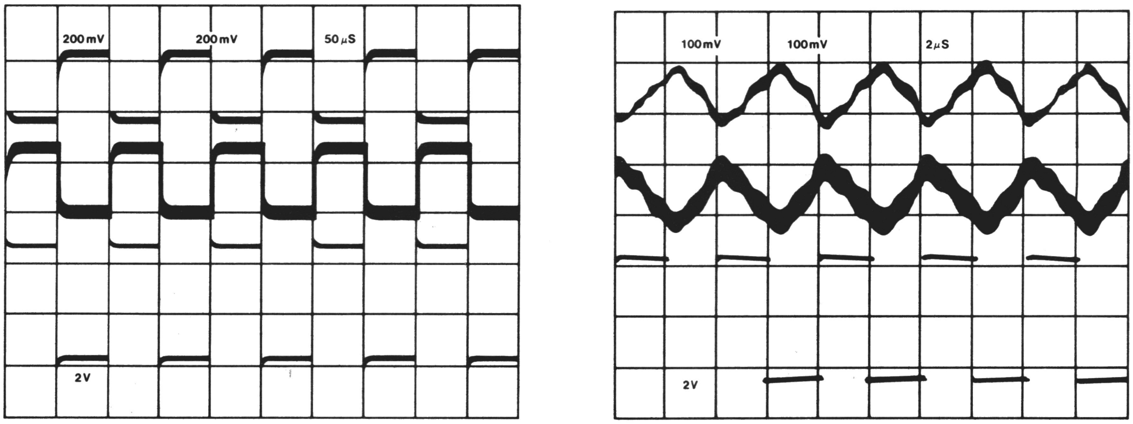

+5V
10K
BIAS
ADJ.
2K
0.22
μF
22μF
+
10K
HYSTERESIS
ADJUST
2K
1.2K
FSK
OUTPUT
1
10
15
16
2
FSK
INPUT
0.1μF
6
1K
0.1μF
7
1K
3
300Ω
+5V
9
100Ω
11
300pF
4
5
300pF
NE564
14
0.1μF
12
33pF
0-20pF
13
8

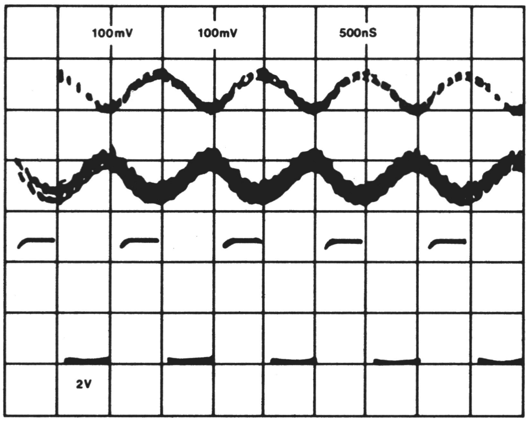
Figure 6

PHASE COMPARATOR (PINS 4 AND 5) AND FSK (PIN 16) OUTPUTS FOR DATA RATES OF



(a) 20K BAUD

(b) 500K BAUD



NOTE
Top trace-pin 4
Center trace-pin 5
Bottom trace-pin 16

(c) 2.0M BAUD

Figure 7

TYPICAL PERFORMANCE CHARACTERISTICS

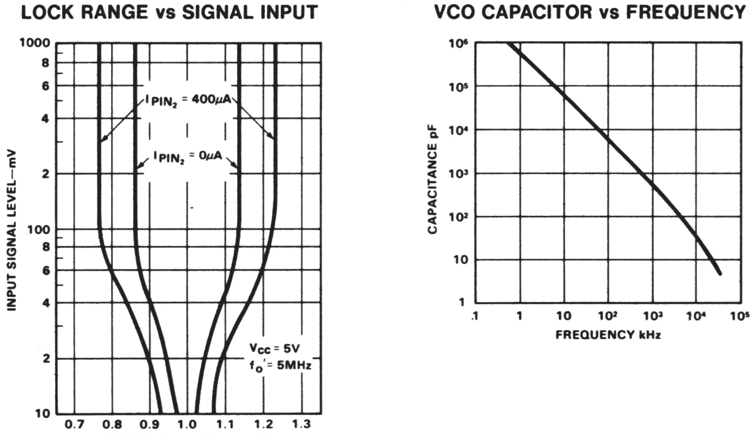
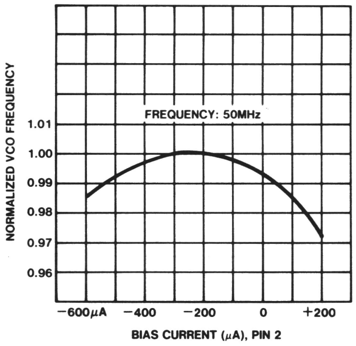
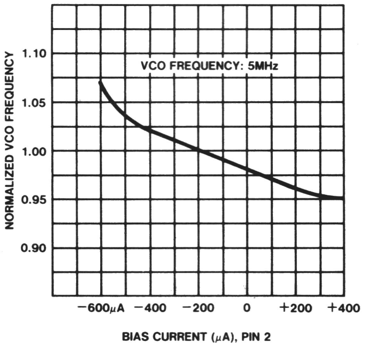


Figure 8

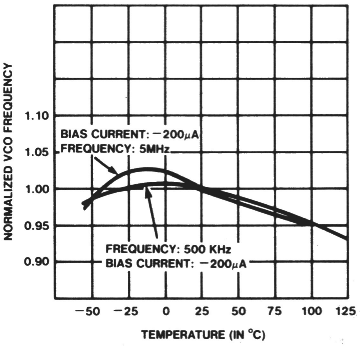
TYPICAL NORMALIZED VCO FREQUENCY AS A FUNCTION OF PIN 2 BIAS CURRENT



TYPICAL NORMALIZED VCO FREQUENCY AS A FUNCTION OF PIN 2 BIAS CURRENT



NORMALIZED VCO FREQUENCY AS A FUNCTION OF TEMPERATURE



NOTE

Refer to section 10 of Signetics Analog Applications Manual for more detailed information.

NE/SE565-F,K,N

DESCRIPTION

The SE/NE565 Phase-Locked Loop (PLL) is a self-contained, adaptable filter and demodulator for the frequency range from 0.001Hz to 500kHz. The circuit comprises a voltage-controlled oscillator of exceptional stability and linearity, a phase comparator, an amplifier and a low-pass filter as shown in the block diagram. The center frequency of the PLL is determined by the free-running frequency of the VCO; this frequency can be adjusted externally with a resistor or a capacitor. The low-pass filter, which determines the capture characteristics of the loop, is formed by an internal resistor and an external capacitor.

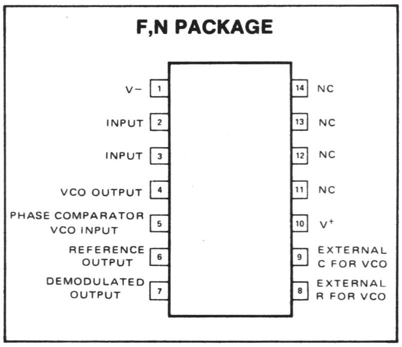
FEATURES

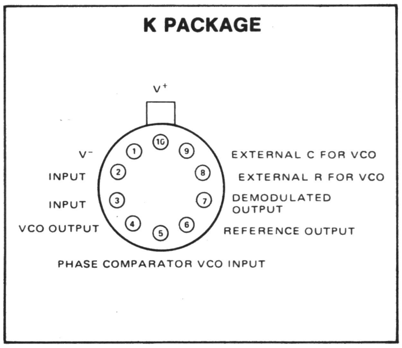
- **Highly stable center frequency (200ppm/°C typ.)**
- **Wide operating voltage range (±6 to ±12 volts)**
- **Highly linear demodulated output (0.2% typ.)**
- **Center frequency programming by means of a resistor or capacitor, voltage or current**
- **TTL and DTL compatible square-wave output; loop can be opened to insert digital frequency divider**
- **Highly linear triangle wave output**
- **Reference output for connection of comparator in frequency discriminator**
- **Bandwidth adjustable from < ±1% to > ±60%**
- **Frequency adjustable over 10 to 1 range with same capacitor**

APPLICATIONS

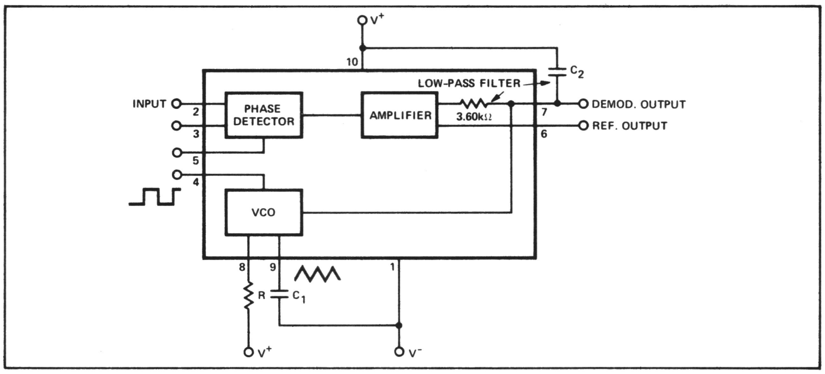
- **Frequency shift keying**
- **Modems**
- **Telemetry receivers**
- **Tone decoders**
- **SCA receivers**
- **Wideband FM discriminators**
- **Data synchronizers**
- **Tracking filters**
- **Signal restoration**
- **Frequency multiplication & division**

PIN CONFIGURATIONS

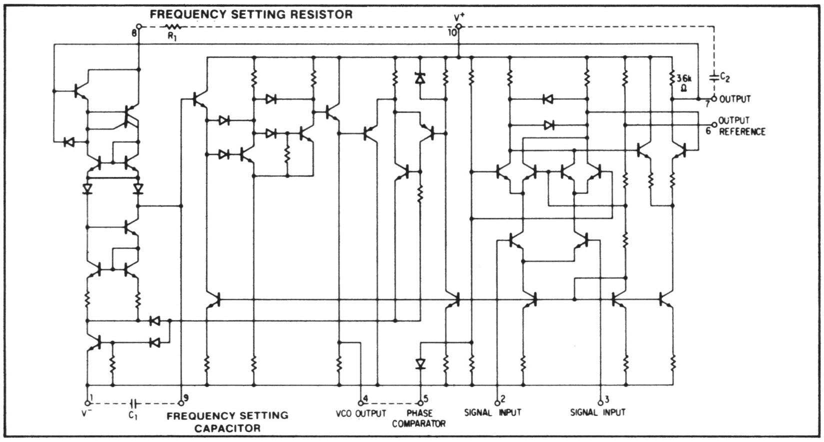

F,N PACKAGE
V− 1
INPUT 2
INPUT 3
VCO OUTPUT 4
PHASE COMPARATOR VCO INPUT 5
REFERENCE OUTPUT 6
DEMODULATED OUTPUT 7
14 NC
13 NC
12 NC
11 NC
10 V+
9 EXTERNAL C FOR VCO
8 EXTERNAL R FOR VCO


K PACKAGE
V+
V−
INPUT
INPUT
VCO OUTPUT
EXTERNAL C FOR VCO
EXTERNAL R FOR VCO
DEMODULATED OUTPUT
REFERENCE OUTPUT
PHASE COMPARATOR VCO INPUT
1
2
3
4
5
6
7
8
9
10

BLOCK DIAGRAM


V+
10
C2
LOW-PASS FILTER
INPUT
2
3
5
4
PHASE DETECTOR
AMPLIFIER
3.60kΩ
7
6
DEMOD. OUTPUT
REF. OUTPUT
VCO
8
9
1
R
C1
V+
V−

EQUIVALENT SCHEMATIC


FREQUENCY SETTING RESISTOR
8
R1
V+
10
C2
3.6k Ω
7 OUTPUT
6 OUTPUT REFERENCE
1
V−
C1
9
FREQUENCY SETTING CAPACITOR
4
VCO OUTPUT
5
PHASE COMPARATOR
2
SIGNAL INPUT
3
SIGNAL INPUT

ABSOLUTE MAXIMUM RATINGS

$T_A = 25°C$ unless otherwise specified.

PARAMETER	RATING	UNIT
Maximum operating voltage	26	V
Input voltage	3	Vp-p
Storage temperature	-65 to +150	°C
Operating temperature range		
NE565	0 to +70	°C
SE565	-55 to +125	°C
Power dissipation	300	mW

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = \pm 6V$ unless otherwise specified.

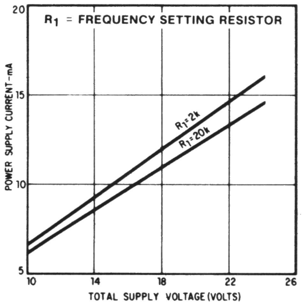
PARAMETER	TEST CONDITIONS	SE565			NE565			UNIT
		Min	Typ	Max	Min	Typ	Max	
SUPPLY REQUIREMENTS								
Supply voltage		12		±12	±6		±12	V
Supply current			8	12.5		8	12.5	mA
INPUT CHARACTERISTICS								
Input impedance[1]		7	10		5	10		kΩ
Input level required for tracking	$f_o = 50kHz$, ±10% frequency deviation	10	1		10	1		mVrms
VCO CHARACTERISTICS								
Center frequency								
Maximum value	$C_1 = 2.7pF$	300	500			500		kHz
Distribution[2]	Distribution taken about $f_o = 50kHz$, $R_1 = 5.0k\Omega$, $C_1 = 1200pF$	-10	0	+10	-30	0	+30	%
Drift with temperature	$f_o = 50kHz$		200			300		ppm/°C
Drift with supply voltage	$f_o = 50kHz$, $V_{CC} = \pm 6$ to ± 7 volts		0.1	1.0		0.2	1.5	%/V
Triangle wave								
Output voltage level		1.9	0		1.9	0		V
Amplitude			2.4	3		2.4	3	Vp-p
Linearity			0.2			0.5		%
Square wave								
Logical "1" output voltage	$f_o = 50kHz$	+4.9	+5.2		+4.9	+5.2		V
Logical "0" output voltage	$f_o = 50kHz$		-0.2	+0.2		-0.2	+0.2	V
Duty cycle	$f_o = 50kHz$	45	50	55	40	50	60	%
Rise time			20	100		20		ns
Fall time			50	200		50		ns
Output current (sink)		0.6	1		0.6	1		mA
Output current (source)		5	10		5	10		mA
DEMODULATED OUTPUT CHARACTERISTICS								
Output voltage level	Measured at pin 7	4.25	4.5	4.75	4.0	4.5	5.0	V
Maximum voltage swing[3]			2			2		Vp-p
Output voltage swing	±10% frequency deviation	250	300		200	300		mVp-p
Total harmonic distortion			0.2	0.75		0.4	1.5	%
Output impedance[4]			3.6			3.6		kΩ
Offset voltage (V6-V7)			30	100		50	200	mV
Offset voltage vs temperature (drift)			50			100		µV/°C
AM rejection		30	40			40		dB

NOTES

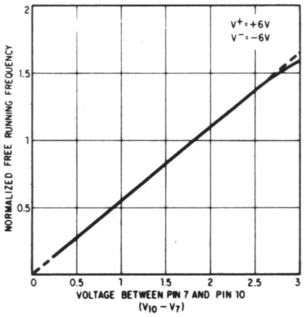
1. Both input terminals (pins 2 and 3) must receive identical dc bias. This bias may range from 0 volts to -4 volts.
2. The external resistance for frequency adjustment (R1) must have a value between 2kΩ and 20kΩ.
3. Output voltage swings negative as input frequency increases.
4. Output not buffered.

TYPICAL PERFORMANCE CHARACTERISTICS

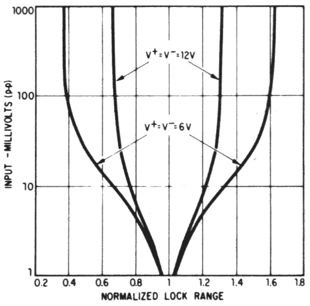
POWER SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



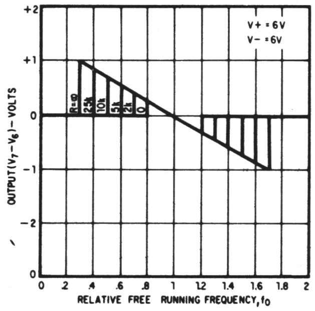
VCO CONVERSION GAIN



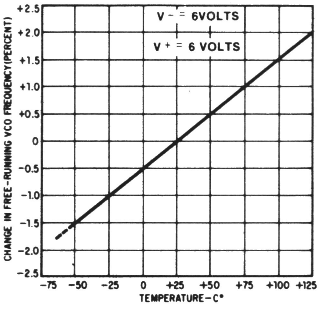
LOCK RANGE AS A FUNCTION OF INPUT VOLTAGE



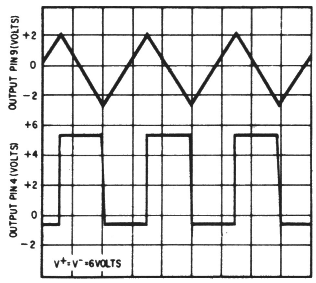
LOCK RANGE AS A FUNCTION OF GAIN SETTING RESISTANCE (PIN 6-7)



CHANGE IN FREE-RNNING VCO FREQUENCY AS A FUNCTION OF TEMPERATURE



VCO OUTPUT WAVEFORM



DESIGN FORMULAS
(See Figure 1)

Free-running frequency of VCO: $f_o \approx \frac{1.2}{4R_1C_1}$ in Hz

Lock-range: $f_L = \pm\frac{8f_o}{V_{CC}}$ in Hz

Capture-range: $f_C \approx \pm\frac{1}{2\pi}\sqrt{\frac{2\pi f_L}{\tau}}$

where $\tau = (3.6\text{X}10^3)\ \text{X}\ C_2$

TYPICAL APPLICATIONS
FM Demodulation

The 565 Phase Locked Loop is a general purpose circuit designed for highly linear FM demodulation. During lock, the average dc level of the phase comparator output signal is directly proportional to the frequency of the input signal. As the input frequency shifts, it is this output signal which causes the VCO to shift its frequency to match that of the input. Consequently, the linearity of the phase comparator output with frequency is determined by the voltage-to-frequency transfer function of the VCO.

Because of its unique and highly linear VCO, the 565 PLL can lock to and track an input signal over a very wide bandwidth (typically ±60%) with very high linearity (typically, within 0.5%).

A typical connection diagram is shown in Figure 1. The VCO free-running frequency is given approximately by

$f_o = \frac{1.2}{4R_1C_1}$ and should be adjusted to be at the center of the input signal frequency range. C1 can be any value, but R1 should be within the range of 2000 to 20,000 ohms with an optimum value on the order of 4000 ohms. The source can be direct coupled if the dc resistances seen from pins 2 and 3 are equal and there is no dc voltage difference between the pins. A short between pins 4 and 5 connects the VCO to the phase comparator. Pin 6 provides a dc reference voltage that is close to the dc potential of the demodulated output (pin 7). Thus, if a resistance is connected between pins 6 and 7, the gain of the output stage can be reduced with little change in the dc voltage level at the output. This allows the lock range to be decreased with little change in the free-running frequency. In this manner the lock range can be decreased from ±60% of f_o to approximately ±20% of f_o (at ±6V).

A small capacitor (typically 0.001μF) should be connected between pins 7 and 8 to eliminate possible oscillation in the control current source.

A single-pole loop filter is formed by the capacitor C2, connected between pin 7 and the positive supply, and an internal resistance of approximately 3600 ohms.

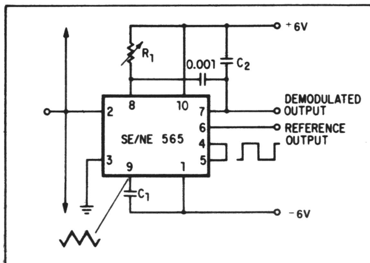


Figure 1

Frequency Shift Keying (FSK)

FSK refers to data transmission by means of a carrier which is shifted between two preset frequencies. This frequency shift is usually accomplished by driving a VCO with the binary data signal so that the two resulting frequencies correspond to the "0" and "1" states (commonly called space and mark) of the binary data signal.

A simple scheme using the 565 to receive FSK signals of 1070Hz and 1270Hz is shown in Figure 2. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding dc shift at the output.

The loop filter capacitor C2 is chosen smaller than usual to eliminate overshoot on the output pulse, and a three-stage RC ladder filter is used to remove the carrier component from the output. The band edge of the ladder filter is chosen to be approximately half way between the maximum keying rate (in this case 300 baud or 150Hz) and twice the input frequency (approximately 2200Hz). The output signal can now be made logic compatible by connecting a voltage comparator between the output and pin 6 of the loop. The free-running frequency is adjusted with R1 so as to result in a slightly-positive voltage at the output with f_{IN} = 1070Hz.

The input connection is typical for cases where a dc voltage is present at the source and therefore a direct connection is not desirable. Both input terminals are returned to ground with identical resistors (in this case, the values are chosen to effect a 600-ohm input impedance).

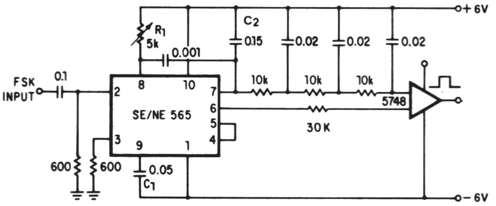


Figure 2

Frequency Multiplication

There are two methods by which frequency multiplication can be achieved using the 565:

1. Locking to a harmonic of the input signal.
2. Inclusion of a digital frequency divider or counter in the loop between the VCO and phase comparator.

The first method is the simplest, and can be achieved by setting the free-running frequency of the VCO to a multiple of the input frequency. A limitation of this scheme is that the lock range decreases as successively higher and weaker harmonics are used for locking. If the input frequency is to be constant with little tracking required, the loop can generally be locked to any one of the first 5 harmonics. For higher orders of multiplication, or for cases where a large lock range is desired, the second scheme is more desirable. An example of this might be a case where the input signal varies over a wide frequency range and a large multiple of the input frequency is required.

A block diagram of the second scheme is shown in Figure 3. Here the loop is broken between the VCO and the phase comparator, and a frequency divider is inserted. The fundamental of the divided VCO frequency is locked to the input frequency in this case, so that the VCO is actually running at a multiple of the input frequency. The amount of multiplication is determined by the frequency divider. A typical connection scheme is shown in Figure 4. To set up the circuit, the frequency limits of the input signal must be determined. The free-running frequency of the VCO is then adjusted by means of R1 and C1 (as discussed under FM demodulation) so that the output frequency of the divider is midway between the input frequency limits. The filter capacitor, C2, should be large enough to eliminate variations in the demodulated output voltage (at pin 7), in order to stabilize the VCO frequency. The output can now be taken as the VCO squarewave output, and its fundamental will be the desired multiple of the input frequency (f_{IN}) as long as the loop is in lock.

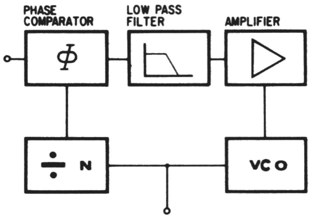


Figure 3

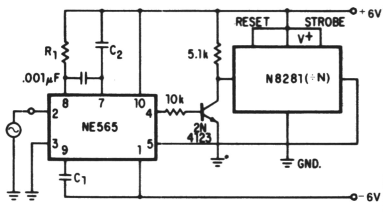


Figure 4

SCA (Background Music) Decoder

Some FM stations are authorized by the FCC to broadcast uninterrupted background music for commerical use. To do this a frequency modulated subcarrier of 67kHz is used. The frequency is chosen so as not to interfere with the normal stereo or monaural program; in addition, the level of the subcarrier is only 10% of the amplitude of the combined signal.

The SCA signal can be filtered out and demodulated with the NE565 Phase Locked Loop without the use of any resonant circuits. A connection diagram is shown in Figure 5. This circuit also serves as an example of operation from a single power supply.

A resistive voltage divider is used to establish a bias voltage for the input (pins 2 and 3). The demodulated (multiplex) FM signal is fed to the input through a two-stage high-pass filter, both to effect capacitive coupling and to attenuate the strong signal of the regular channel. A total signal amplitude, between 80mV and 300mV, is required at the input. Its source should have an impedance of less than 10,000 ohms.

The Phase Locked Loop is tuned to 67kHz with a 5000 ohm potentiometer; only approximate tuning is required, since the loop will seek the signal.

The demodulated output (pin 7) passes through a three-stage low-pass filter to provide de-emphasis and attenuate the high-frequency noise which often accompanies SCA transmission. Note that no capacitor is provided directly at pin 7; thus, the circuit is operating as a first-order loop. The demodulated output signal is in the order of 50mV and the frequency response extends to 7kHz.

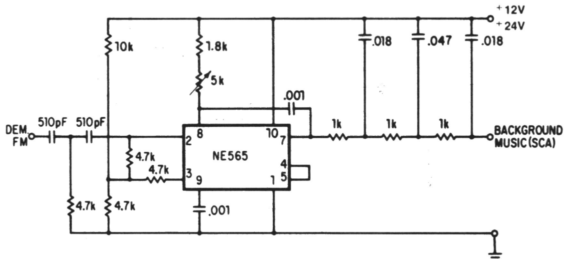

+12V
+24V
10k
1.8k
5k
.018
.047
.018
.001
DEM. FM
510pF
510pF
8
10
7
2
NE565
4.7k
4.7k
3
9
4
5
1
1k
1k
1k
BACKGROUND MUSIC (SCA)
4.7k
4.7k
.001

Figure 5

FUNCTION GENERATOR NE/SE566

NE/SE566-F,N,T

DESCRIPTION

The SE/NE 566 Function Generator is a voltage controlled oscillator of exceptional linearity with buffered square wave and triangle wave outputs. The frequency of oscillation is determined by an external resistor and capacitor and the voltage applied to the control terminal. The oscillator can be programmed over a ten to one frequency range by proper selection of an external resistance and modulated over a ten to one range by the control voltage, with exceptional linearity.

FEATURES

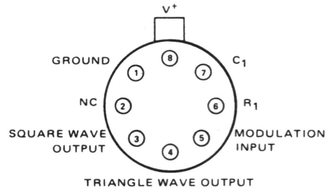
- **Wide range of operating voltage (up to 24 volts)**
- **High linearity of modulation**
- **Highly stable center frequency (200 ppm/°C typical)**
- **Highly linear triangle wave output**
- **Frequency programming by means of a resistor or capacitor, voltage or current**
- **Frequency adjustable over 10 to 1 range with same capacitor**

APPLICATIONS

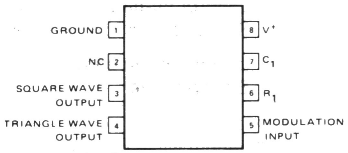
- **Tone generators**
- **Frequency shift keying**
- **FM modulators**
- **Clock generators**
- **Signal generators**
- **Function generators**

PIN CONFIGURATIONS

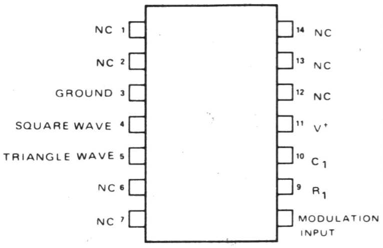
T PACKAGE


V+
GROUND
C1
NC
R1
SQUARE WAVE OUTPUT
MODULATION INPUT
TRIANGLE WAVE OUTPUT
1
2
3
4
5
6
7
8

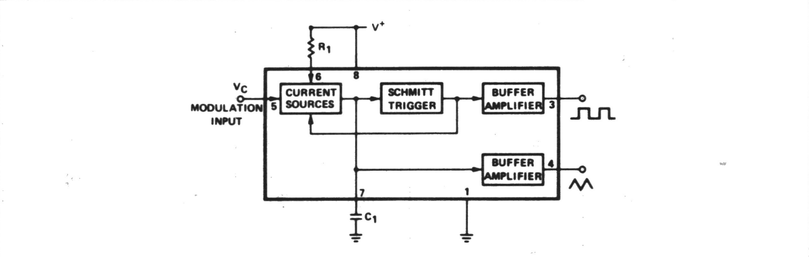
N PACKAGE


GROUND 1
NC 2
SQUARE WAVE OUTPUT 3
TRIANGLE WAVE OUTPUT 4
8 V+
7 C1
6 R1
5 MODULATION INPUT

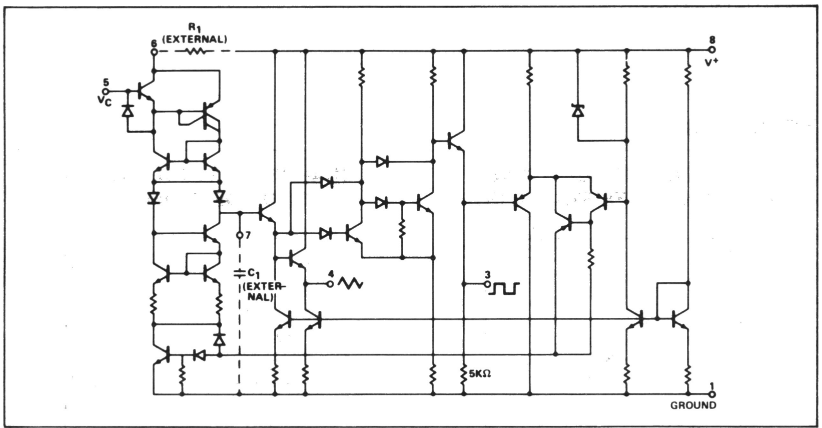
F PACKAGE


NC 1
NC 2
GROUND 3
SQUARE WAVE 4
TRIANGLE WAVE 5
NC 6
NC 7
14 NC
13 NC
12 NC
11 V+
10 C1
9 R1
MODULATION INPUT

BLOCK DIAGRAM


V+
R1
6
8
VC
MODULATION INPUT
5
CURRENT SOURCES
SCHMITT TRIGGER
BUFFER AMPLIFIER
3
BUFFER AMPLIFIER
4
7
1
C1

EQUIVALENT SCHEMATIC


R1 (EXTERNAL)
6
5
VC
8
V+
7
C1 (EXTERNAL)
4
3
5KΩ
1
GROUND

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Maximum operating voltage	26	V
Input voltage	3	V_{P-P}
Storage temperature	-65 to +150	°C
Operating temperature range		
NE566	0 to +70	°C
SE566	-55 to +125	°C
Power dissipation	300	mW

NE/SE566-F,N,T

ELECTRICAL CHARACTERISTICS

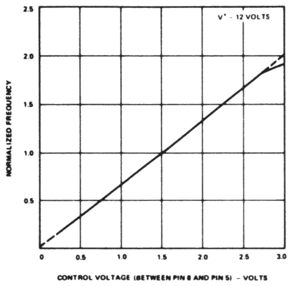
$T_A = 25°C$; $V_{CC} = 12V$ unless otherwise specified.

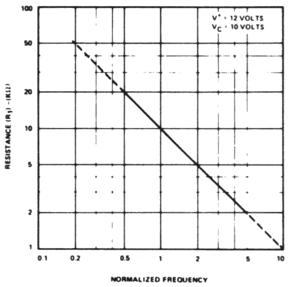
PARAMETER	SE566			NE566			UNIT
	Min	Typ	Max	Min	Typ	Max	
GENERAL							
Operating temperature range	-55		125	0		70	°C
Operating supply voltage			24			24	V
Operating supply current		7	12.5		7	12.5	mA
VCO[1]							
Maximum operating frequency		1			1		MHz
Frequency drift with temperature		200			300		ppm/°C
Frequency drift with supply voltage		1			2		%/V
Control terminal input impedance[2]		1			1		MΩ
FM distortion (±10% deviation)		0.2	0.75		0.4	1.5	%
Maximum sweep rate		1			1		MHz
Sweep range		10:1			10:1		
OUTPUT							
Triangle wave output							
Impedance		50			50		Ω
Voltage	1.9	2.4		1.9	2.4		Vpp
Linearity		0.2			0.5		%
Square wave input							
Impedance		50			50		Ω
Voltage	5	5.4		5	5.4		Vpp
Duty Cycle	45	50	55	40	50	60	%
Rise time		20			20		ns
Fall Time		50			50		ns

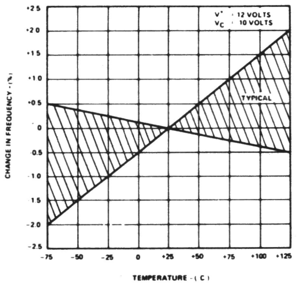
NOTES

1. The external resistance for frequency adjustment (R_1) must have a value between 2kΩ and 20KΩ.
2. The bias voltage (V_C) applied to the control terminal (pin 5) should be in the range $3/4V^+ \le V_C \le V^+$.

TYPICAL PERFORMANCE CHARACTERISTICS

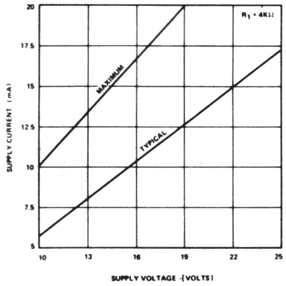

NORMALIZED FREQUENCY AS A FUNCTION OF CONTROL VOLTAGE


NORMALIZED FREQUENCY AS A FUNCTION OF RESISTANCE (R1)

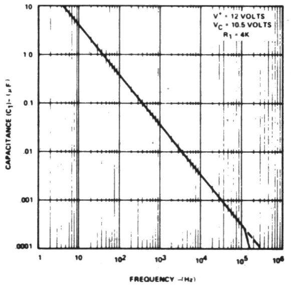

CHANGE IN FREQUENCY AS A FUNCTION OF TEMPERATURE

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

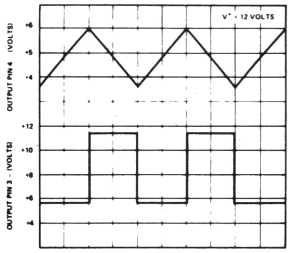
POWER SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



FREQUENCY AS A FUNCTION OF CAPACITANCE (C1)



VCO OUTPUT WAVEFORMS



OPERATING INSTRUCTIONS

The SE/NE 566 Function Generator is a general purpose voltage controlled oscillator designed for highly linear frequency modulation. The circuit provides simultaneous square wave and triangle wave outputs at frequencies up to 1MHz. A typical connection diagram is shown in Figure 1. The control terminal (pin 5) must be biased externally with a voltage (V_C) in the range

$$3/4\, V^+ \leq V_C \leq V^+$$

where V_{CC} is the total supply voltage. In Figure 1, the control voltage is set by the voltage divider formed with R_2 and R_3. The modulating signal is then ac coupled with the capacitor C_2. The modulating signal can be direct coupled as well, if the appropriate dc bias voltage is applied to the control terminal. The frequency is given approximately by

$$f_O \simeq \frac{2[(V^+) - (V_C)]}{R_1 C_1 V^+}$$

and R_1 should be in the range $2k\Omega < R_1 < 20k\Omega$.

A small capacitor (typically 0.001μf) should be connected between pins 5 and 6 to eliminate possible oscillation in the control current source.

If the VCO is to be used to drive standard logic circuitry, it may be desirable to use a dual supply of ±5 volts as shown in Figure 2. In this case the square wave output has the proper dc levels for logic circuitry. RTL can be driven directly from pin 3. For DTL or T^2L gates, which require a current sink of more than 1mA, it is usually necessary to connect a 5kΩ resistor between pin 3 and negative supply. This increases the current sinking capability to 2mA. The third type of interface shown uses a saturated transistor between the 566 and the logic circuitry. This scheme is used primarily for T^2L circuitry which requires a fast fall time (<50ns) and a large current sinking capability.

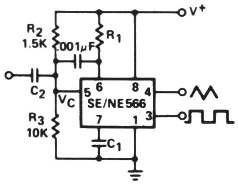


FIGURE 1

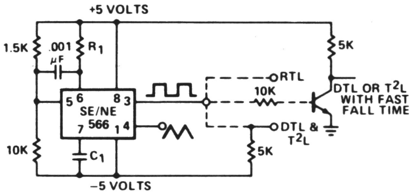


FIGURE 2

TONE DECODER/PHASE LOCKED LOOP — NE/SE567

NE/SE567-F,N,T

DESCRIPTION

The SE/NE567 tone and frequency decoder is a highly stable phase-locked loop with synchronous AM lock detection and power output circuitry. Its primary function is to drive a load whenever a sustained frequency within its detection band is present at the self-biased input. The bandwidth center frequency, and output delay are independently determined by means of four external components.

FEATURES

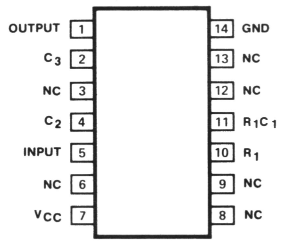
- **Wide frequency range (.01Hz to 500kHz)**
- **High stability of center frequency**
- **Independently controllable bandwidth (up to 14 percent)**
- **High out-band signal and noise rejection**
- **Logic-compatible output with 100mA current sinking capability**
- **Inherent immunity to false signals**
- **Frequency adjustment over a 20 to 1 range with an external resistor**
- **Military processing available**

APPLICATIONS

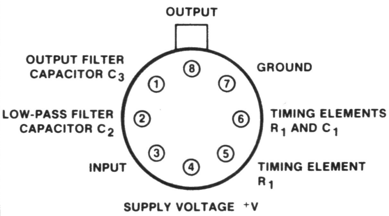
- **Touch Tone® decoding**
- **Carrier current remote controls**
- **Ultrasonic controls (remote TV, etc.)**
- **Communications paging**
- **Frequency monitoring and control**
- **Wireless intercom**
- **Precision oscillator**

PIN CONFIGURATIONS

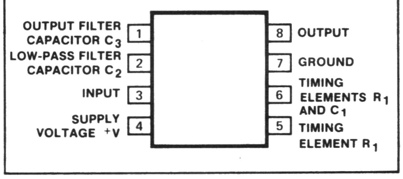
F PACKAGE


OUTPUT 1
C3 2
NC 3
C2 4
INPUT 5
NC 6
VCC 7
14 GND
13 NC
12 NC
11 R1C1
10 R1
9 NC
8 NC

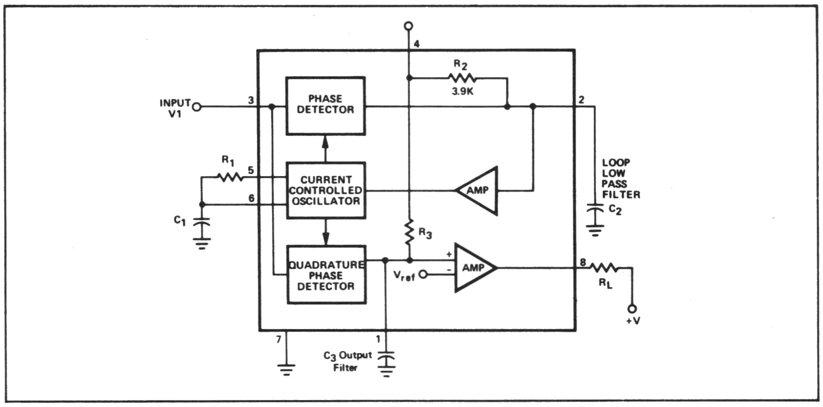
T PACKAGE


OUTPUT
OUTPUT FILTER CAPACITOR C3
GROUND
LOW-PASS FILTER CAPACITOR C2
TIMING ELEMENTS R1 AND C1
INPUT
TIMING ELEMENT R1
SUPPLY VOLTAGE +V
1
2
3
4
5
6
7
8

N PACKAGE


OUTPUT FILTER CAPACITOR C3 1
LOW-PASS FILTER CAPACITOR C2 2
INPUT 3
SUPPLY VOLTAGE +V 4
8 OUTPUT
7 GROUND
6 TIMING ELEMENTS R1 AND C1
5 TIMING ELEMENT R1

BLOCK DIAGRAM

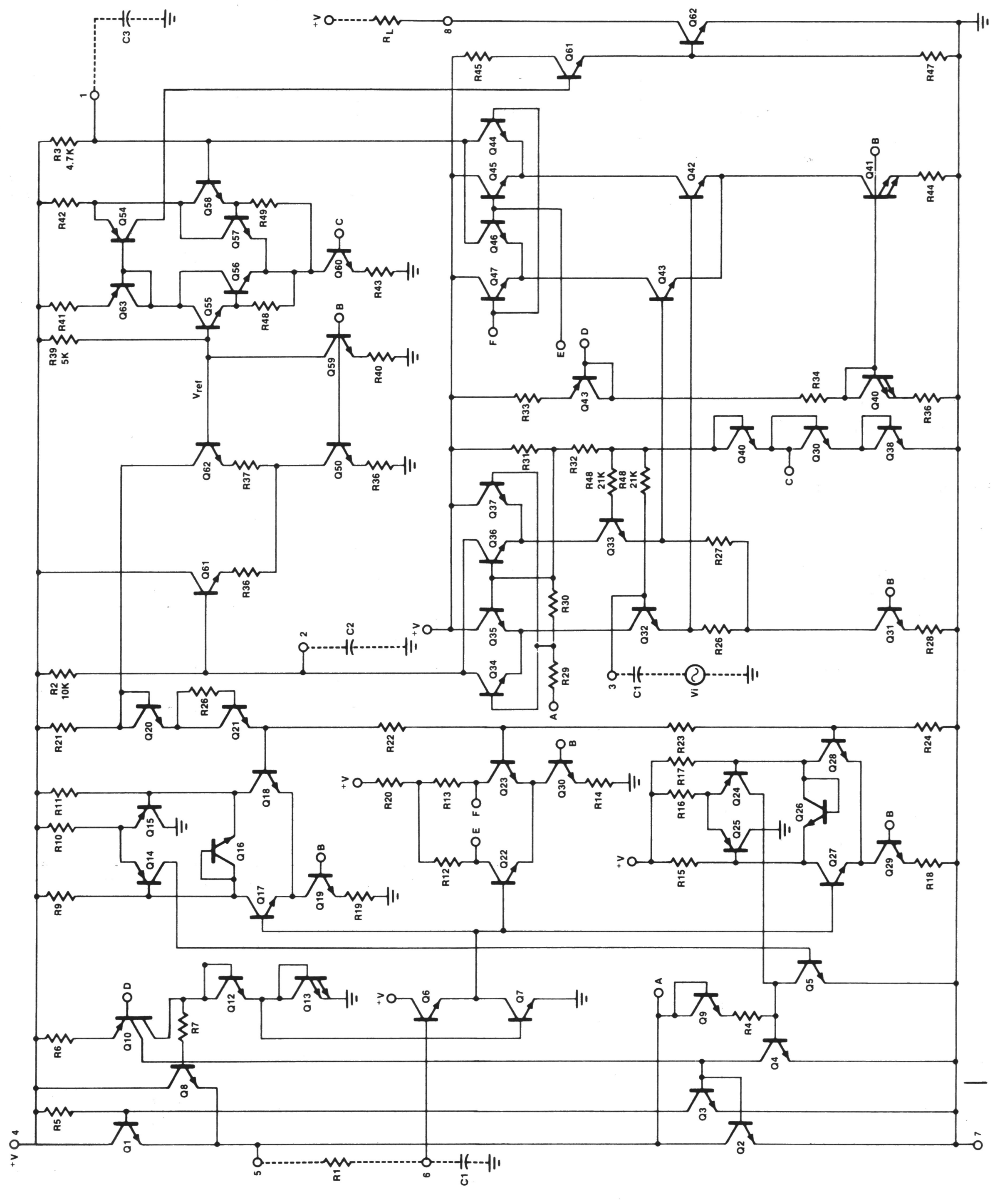

INPUT V1
3
PHASE DETECTOR
4
R2
3.9K
2
LOOP LOW PASS FILTER
C2
R1
5
6
C1
CURRENT CONTROLLED OSCILLATOR
AMP
R3
QUADRATURE PHASE DETECTOR
Vref
+
-
AMP
8
RL
+V
7
1
C3 Output Filter

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Operating temperature		
NE567	0 to +70	°C
SE567	-55 to +125	°C
Operating voltage	10	V
Positive voltage at input	0.5 + Vs	V
Negative voltage at input	-10	Vdc
Output voltage (collector of output transistor)	15	Vdc
Storage temperature	-65 to +150	°C
Power dissipation	300	mW

NE/SE567-F,N,T

EQUIVALENT SCHEMATIC


C3
1
+V
R_L
8
Q62
R45
Q61
R47
R3 4.7K
Q44
Q45
Q46
Q47
B
Q41
R44
Q42
Q43
R42
Q54
Q58
Q57
R49
C
Q60
R43
Q63
Q56
Q55
R48
R41
B
Q59
R40
R39 5K
V_{ref}
F
E
D
R33
Q43
R34
Q40
R36
Q40
C
Q30
Q38
Q62
R37
Q50
R36
R31
R32
R48 21K
R48 21K
Q37
Q36
Q33
R27
Q61
R36
R30
2
C2
+V
Q35
Q34
R29
A
Q32
R26
B
Q31
R28
3
C1
Vi
R2 10K
R21
Q20
R26
Q21
R22
R23
R24
Q28
R17
R16
Q24
Q25
Q26
+V
R15
Q27
B
Q29
R18
+V
R20
R13
F
Q23
B
Q30
R14
E
R12
Q22
R11
Q15
R10
Q14
Q16
Q18
R9
Q17
B
Q19
R19
D
Q10
R6
R7
Q12
Q13
+V
Q6
Q7
A
Q9
R4
Q5
Q4
Q8
R5
Q1
Q3
Q2
+V 4
5
R1
6
C1
7

NE/SE567-F,N,T

DC ELECTRICAL CHARACTERISTICS (V+ = 5.0V; T_A = 25°C unless otherwise specified.)

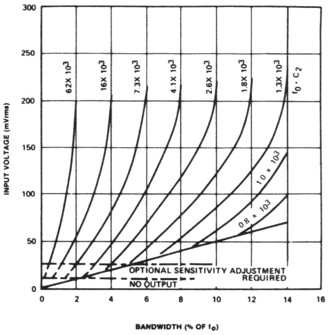
PARAMETER	TEST CONDITIONS	SE567			NE567			UNIT
		Min	Typ	Max	Min	Typ	Max	
CENTER FREQUENCY[1]								
Highest center frequency (f_o)		100	500		100	500		kHz
Center frequency stability[2]	-55 to +125°C		35±140			35±140		ppm/°C
	0 to +70°C		35±60			35±60		ppm/°C
Center frequency shift with supply voltage	f_o = 100kHz		0.5	1		0.7	2	%/V
DETECTION BANDWIDTH								
Largest detection bandwidth	f_o = 100kHz	12	14	16	10	14	18	% of f_o
Largest detection bandwidth skew			1	2		2	3	% of f_o
Largest detection bandwidth—variation with temperature	V_i = 300mVrms		±0.1			±0.1		%/°C
Largest detection bandwidth—variation with supply voltage	V_i = 300mVrms		±2			±2		%/V
INPUT								
Input resistance			20			20		kΩ
Smallest detectable input voltage (V_i)	I_L = 100mA, $f_i = f_o$		20	25		20	25	mVrms
Largest no-output input voltage	I_L = 100mA, $f_i = f_o$	10	15		10	15		mVrms
Greatest simultaneous outband signal to inband signal ratio			+6			+6		dB
Minimum input signal to wideband noise ratio	B_n = 140kHz		-6			-6		dB
OUTPUT								
Fastest on-off cycling rate			f_o/20			f_o/20		
"1" output leakage current			0.01	25		0.01	25	μA
"0" output voltage	I_L = 30mA		0.2	0.4		0.2	0.4	V
	I_L = 100mA		0.6	1.0		0.6	1.0	V
Output fall time[3]	R_L = 50Ω		30			30		ns
Output rise time[3]	R_L = 50Ω		150			150		ns
GENERAL								
Operating voltage range		4.75		9.0	4.75		9.0	V
Supply current quiescent			6	8		7	10	mA
Supply current—activated	R_L = 20kΩ		11	13		12	15	mA
Quiescent power dissipation			30			35		mW

NOTES

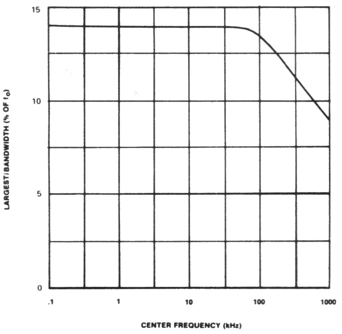
1. Frequency determining resistor R_1 should be between 1 and 20kΩ.
2. Applicable over 4.75 to 5.75 volts. See graphs for more detailed information.
3. Pin 8 to Pin 1 feedback R_L network selected to eliminate pulsing during turn-on and turn-off.

TYPICAL PERFORMANCE CHARACTERISTICS

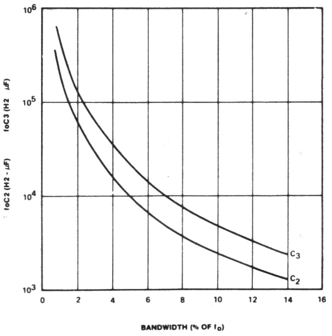
BANDWIDTH vs INPUT SIGNAL AMPLITUDE



LARGEST DETECTION BANDWIDTH vs OPERATING FREQUENCY

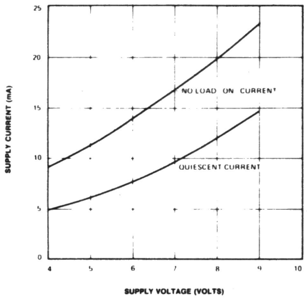


DETECTION BANDWIDTH AS A FUNCTION OF C_2 and C_3

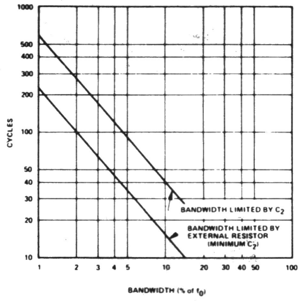


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

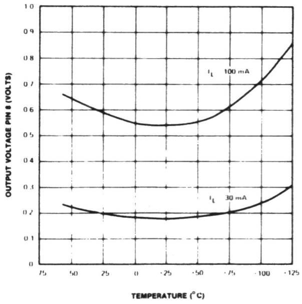
TYPICAL SUPPLY CURRENT vs SUPPLY VOLTAGE



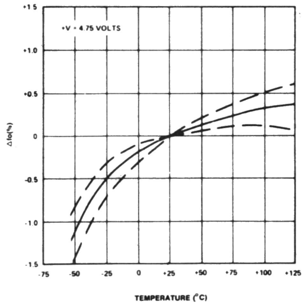
GREATEST NUMBER OF CYCLES BEFORE OUTPUT



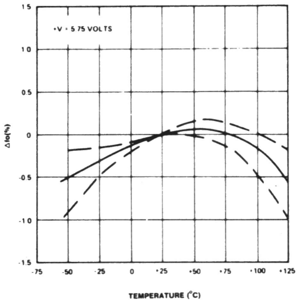
TYPICAL OUTPUT VOLTAGE vs TEMPERATURE



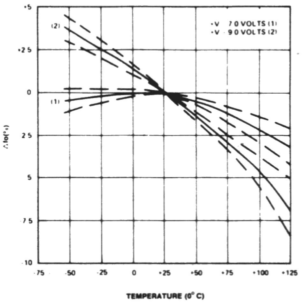
TYPICAL FREQUENCY DRIFT WITH TEMPERATURE (MEAN AND S.D.)



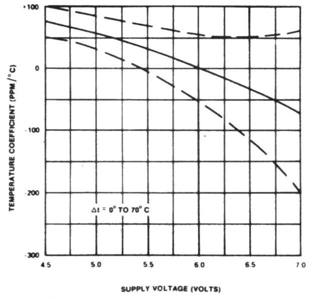
TYPICAL FREQUENCY DRIFT WITH TEMPERATURE (MEAN AND S.D.)



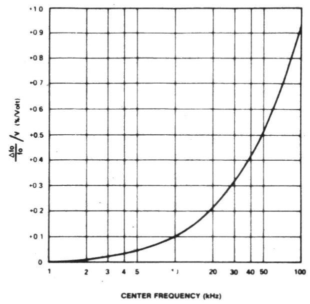
TYPICAL FREQUENCY DRIFT WITH TEMPERATURE (MEAN AND S.D.)



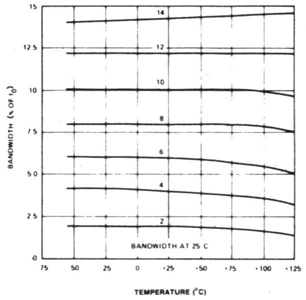
CENTER FREQUENCY TEMPERATURE COEFFICIENT (MEAN AND S.D.)



CENTER FREQUENCY SHIFT WITH SUPPLY VOLTAGE CHANGE vs OPERATING FREQUENCY



TYPICAL BANDWIDTH VARIATION WITH TEMPERATURE



DESIGN FORMULAS

$$f_0 \simeq \frac{1.1}{R_1C_1}$$

$$BW \simeq 1070\sqrt{\frac{V_I}{f_0C_2}} \text{ in \% of } f_0, V_I \leq 200\text{mVrms}$$

Where

V_I = Input Voltage (Vrms)
C_2 = Low-Pass Filter Capacitor (μF)

PHASE LOCKED LOOP TERMINOLOGY CENTER FREQUENCY (fo)

The free-running frequency of the current controlled oscillator (CCO) in the absence of an input signal.

Detection Bandwidth (BW)

The frequency range, centered about f_0, within which an input signal above the threshold voltage (typically 20mVrms) will cause a logical zero state on the output. The detection bandwidth corresponds to the loop capture range.

Lock Range

The largest frequency range within which an input signal above the threshold voltage will hold a logical zero state on the output.

Detection Band Skew

A measure of how well the detection band is centered about the center frequency, f_0. The skew is defined as $(f_{max} + f_{min} - 2f_0)/2f_0$ where fmax and fmin are the frequencies corresponding to the edges of the detection band. The skew can be reduced to zero if necessary by means of an optional centering adjustment.

OPERATING INSTRUCTIONS

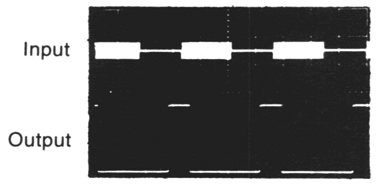
Figure 1 shows a typical connection diagram for the 567. For most applications, the following three-step procedure will be sufficient for choosing the external components R_1, C_1, C_2 and C_3.

1. Select R_1 and C_1 for the desired center frequency. For best temperature stability, R_1 should be between 2K and 20K ohm, and the combined temperature coefficient of the R_1C_1 product should have sufficient stability over the projected temperature range to meet the necessary requirements.

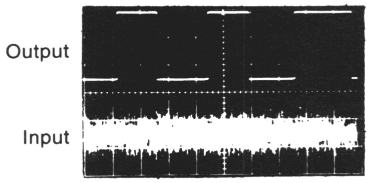
2. Select the low pass capacitor, C_2, by referring to the Bandwidth versus Input Signal Amplitude graph. If the input amplitude variation is known, the appropriate value of f_0C_2 necessary to give the desired bandwidth may be found. Conversely, an area of operation may be selected on this graph and the input level and C_2 may be adjusted accordingly. For example, constant bandwidth operation requires that input amplitude be above 200mVrms. The bandwidth, as noted on the graph, is then controlled solely by the f_0C_2 product (f_0 (Hz), C_2 (μ fd)).

3. The value of C_3 is generally non-critical. C_3 sets the band edge of a low pass filter which attenuates frequencies outside the detection band to elminate spurious outputs. If C_3 is too small, frequencies just outside the detection band will switch the output stage on and off at the beat frequency, or the output may pulse on and off during the turn-on transient. If C_3 is too large, turn-on and turn-off of the output stage will be delayed until the voltage on C_3 passes the threshold voltage. (Such delay may be desirable to avoid spurious outputs due to translent frequencies.) A typical minimum value for C_3 is $2C_2$.

TYPICAL RESPONSE



Response to 100mVrms tone burst.
R_L = 100 ohms.



Response to same input tone burst with wideband noise.
$\frac{S}{N}$ = -6db R_L = 100 ohms
Noise Bandwidth = 140Hz

AVAILABLE OUTPUTS (Figure 2)

The primary output is the uncommitted output transistor collector, pin 8. When an in-band input signal is present, this transistor saturates; its collector voltage being less than 1.0 volt (typically 0.6V) at full output current (100mA). The voltage at pin 2 is the phase detector output which is a linear function of frequency over the range of 0.95 to 1.05 f_0 with a slope of about 20mV per percent of frequency deviation. The average voltage at pin 1 is, during lock, a function of the inband input amplitude in accordance with the transfer characteristic given. Pin 5 is the controlled oscillator square wave output of magnitude $(+V - 2V_{be}) \approx (+V - 1.4V)$ having a dc average of +V/2. A 1kΩ load may be driven from pin 5. Pin 6 is an exponential triangle of 1 volt peak-to-peak with an average dc level of +V/2. Only high impedance loads may be connected to pin 6 without affecting the CCO duty cycle or temperature stability.

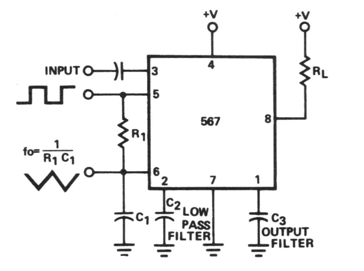


Figure 1

OPERATING PRECAUTIONS

A brief review of the following precautions will help the user achieve the high level of performance of which the 567 is capable.

1. Operation in the high input level mode (above 200mV) will free the user from bandwidth variations due to changes in the in-band signal amplitude. The input stage is now limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the in-band signal is suppressed. Also, the limiting action will create in-band components from sub-harmonic signals, so the 567 becomes sensitive to signals at $f_0/3$, $f_0/5$, etc.

2. The 567 will lock onto signals near $(2n + 1) f_0$, and will give an output for signals near $(4n + 1) f_0$ where n = 0, 1, 2, etc. Thus, signals at $5f_0$ and $9f_0$ can cause an unwanted output. If such signals are anticipated, they should be attenuated before reaching the 567 input.

3. Maximum immunity from noise and out-band signals is afforded in the low input level (below 200mVrms) and reduced bandwidth operating mode. However, decreased loop damping causes the worse-case lock-up time to increase, as shown by the Greatest Number of Cycles Before Output vs Bandwidth graph.

4. Due to the high switching speeds (20ns) associated with 567 operation, care should be taken in lead routing. Lead lengths should be kept to a minimum. The power supply should be adequately bypassed close to the 567 with a 0.01μF or greater capacitor; grounding paths should be carefully chosen to avoid ground loops and

unwanted voltage variations. Another factor which must be considered is the effect of load energization on the power supply. For example, an incandescent lamp typically draws 10 times rated current at turn-on. This can cause supply voltage fluctuations which could, for example, shift the detection band of narrow-band systems sufficiently to cause momentary loss of lock. The result is a low-frequency oscillation into and out of lock. Such effects can be prevented by supplying heavy load currents from a separate supply or increasing the supply filter capacitor.

SPEED OF OPERATION

Minimum lock-up time is related to the natural frequency of the loop. The lower it is, the longer becomes the turn-on transient. Thus, maximum operating speed is obtained when C_2 is at a minimum. When the signal is first applied, the phase may be such as to initially drive the controlled oscillator away form the incoming frequency rather than toward it. Under this condition, which is of course unpredictable, the lock-up transient is at its worst and the theoretical minimum lock-up time is not achievable. We must simply wait for the transient to die out.

The following expressions give the values of C_2 and C_3 which allow highest operating speeds for various band center frequencies. The minimum rate at which digital information may be detected without information loss due to the turn-on transient or output chatter is about 10 cycles per bit, corresponding to an information transfer rate of $f_o/10$ baud.

$$C_2 = \frac{130}{f_o}\ \mu F$$

$$C_3 = \frac{260}{f_o}\ \mu F$$

In cases where turn-off time can be sacrificed to achieve fast turn-on, the optional sensitivity adjustment circuit can be used to move the quiescent C_3 voltage lower (closer to the threshold voltage). However, sensitivity to beat frequencies, noise and extraneous signals will be increased.

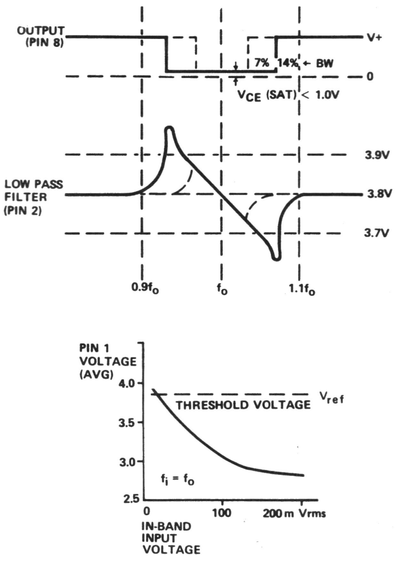


Figure 2

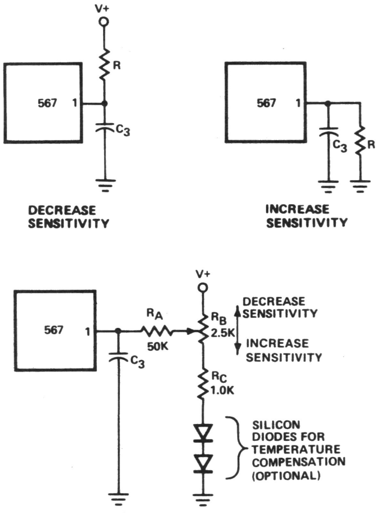


Figure 3

OPTIONAL CONTROLS (Figure 3)

The 567 has been designed so that, for most applications, no external adjustments are required. Certain applications, however, will be greatly facilitated if full advantage is taken of the added control possibilities available through the use of additional external components. In the diagrams given, typical values are suggested where applicable. For best results the resistors used, except where noted, should have the same temperature coefficient. Ideally, silicon diodes would be low-resistivity types, such as forward-biased transistor base-emmiter junctions. However, ordinary low-voltage diodes should be adequate for most applications.

SENSITIVITY ADJUSTMENT

(Figure 3)

When operated as a very narrow band detector (less than 8 percent), both C_2 and C_3 are made quite large in order to improve noise and outband signal rejection. This will inevitably slow the response time. If, however, the output stage is biased closer to the threshold level, the turn-on time can be improved. This is accomplished by drawing additional current to terminal 1. Under this condition, the 567 will also give an output for lower-level signals (10mV or lower).

By adding current to terminal 1, the output stage is biased further away from the threshold voltage. This is most useful when, to obtain maximum operating speed, C_2 and C_3 are made very small. Normally, frequencies just outside the detection band could cause false outputs under this condition. By desensitizing the output stage, the outband beat notes do not feed through to the output stage. Since the input level must be somewhat greater when the output stage is made less sensitive, rejection of third harmonics or in-band harmonics (of lower frequency signals) is also improved.

CHATTER PREVENTION (Figure 4)

Chatter occurs in the output stage when C_3 is relatively small, so that the lock transient and the AC components at the quadrature phase detector (lock detector) output cause the output stage to move through its threshold more than once. Many loads, for example lamps and relays, will not respond to the chatter. However, logic may recognize the chatter as a series of outputs. By feeding the output stage output back to its input (pin 1) the chatter can be eliminated. Three schemes for doing this are given in Figure 4. All operate by feeding the first output step (either on or off) back to the input, pushing the input past the threshold until the transient conditions are over. It is only necessary to assure that the feedback time constant is not so large as to prevent operation at the highest anticipated speed. Although chatter can always be eliminated by making C_3 large, the feedback circuit will enable faster operation of the 567 by allowing C_3 to be kept small. Note that if the feedback time constant is made quite large, a short burst at the input frequency can be stretched into a long output pulse. This may be useful to drive, for example, stepping relays.

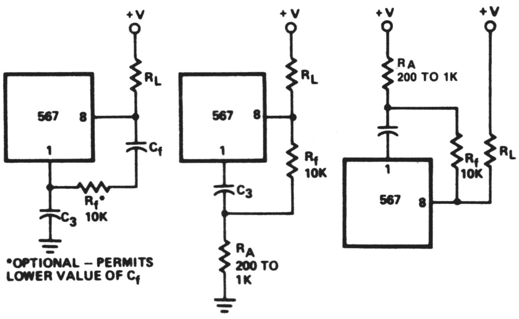


Figure 4

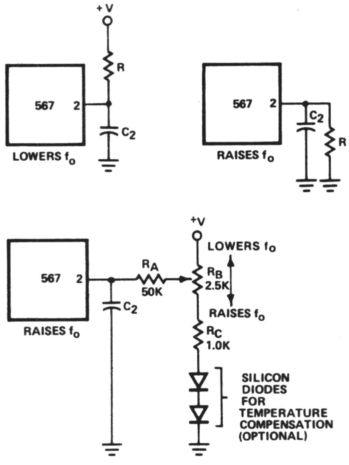


Figure 5

DETECTION BAND CENTERING (OR SKEW) ADJUSTMENT

(Figure 5)

When it is desired to alter the location of the detection band (corresponding to the loop capture range) within the lock range, the circuits shown above can be used. By moving the detection band to one edge of the range, for example, input signal variations will expand the detection band in only one direction. This may prove useful when a strong but undesirable signal is expected on one side or the other of the center frequency. Since R_B also alters the duty cycle slightly, this method may be used to obtain a precise duty cycle when the 567 is used as an oscillator.

ALTERNATE METHOD OF BANDWIDTH REDUCTION

(Figure 6)

Although a large value of C_2 will reduce the bandwidth, it also reduces the loop damping so as to slow the circuit response time. This may be undesirable. Bandwidth can be reduced by reducing the loop gain. This scheme will improve damping and permit faster operation under narrow-band conditions. Note that the reduced impedance level at terminal 2 will require that a larger value of C_2 be used for a given filter cutoff frequency. If more than three 567s are to be used, the network of R_B and R_C can be eliminated and the R_A resistors connected together. A capacitor between this junction and ground may be required to shunt high frequency components.

OUTPUT LATCHING (Figure 7)

To latch the output on after a signal is received, it is necessary to provide a feedback resistor around the output stage (between pins 8 and 1). Pin 1 is pulled up to unlatch the output stage.

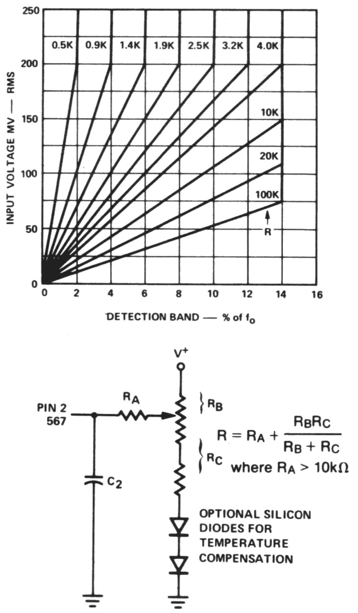
REDUCTION OF C1 VALUE

(Figure 8)

For precision very low-frequency applications, where the value of C_1 becomes large, an overall cost savings may be achieved by inserting a voltage follower between the R_1 C_1 junction and pin 6, so as to allow a higher value of R_1 and a lower value of C_1 for a given frequency.

PROGRAMMING

To change the center frequency, the value of R_1 can be changed with a mechanical or solid state switch, or additional C_1 capacitors may be added by grounding them through saturating npn transistors.


250
200
150
100
50
0
INPUT VOLTAGE MV — RMS
0.5K
0.9K
1.4K
1.9K
2.5K
3.2K
4.0K
10K
20K
100K
R
0
2
4
6
8
10
12
14
16
DETECTION BAND — % of f_o
V+
PIN 2 567
R_A
R_B
R_C
C_2
$R = R_A + \frac{R_B R_C}{R_B + R_C}$
where $R_A > 10k\Omega$
OPTIONAL SILICON DIODES FOR TEMPERATURE COMPENSATION

$$\frac{130}{f_o}\left(\frac{10K + R}{R}\right) < C_2 < \frac{1300}{f_o}\left(\frac{10K + R}{R}\right)$$

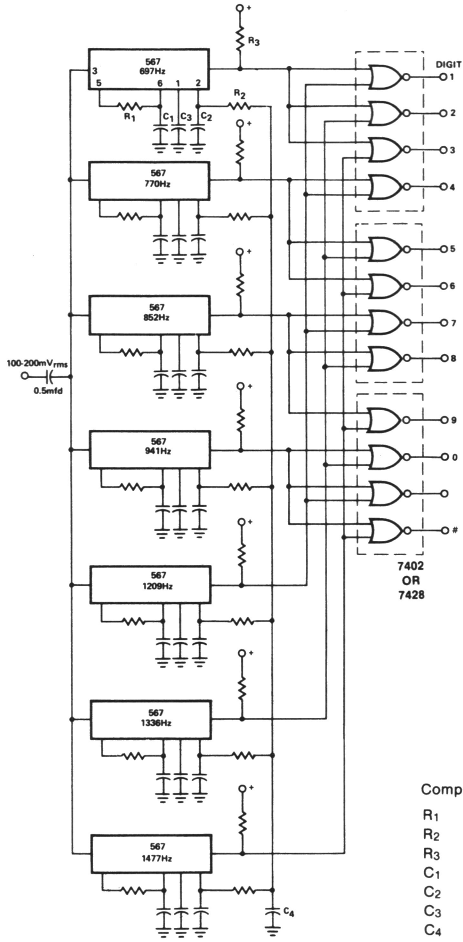
NOTE

Adjust control for symmetry of detection band edges about f_o.

Figure 6

TYPICAL APPLICATIONS

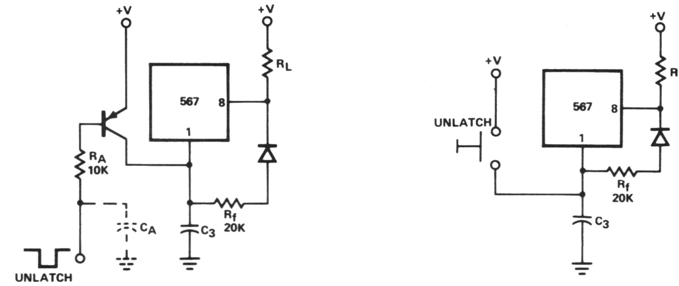
TOUCH-TONE® DECODER


+
R_3
567 697Hz
3
5
6
1
2
R_1
C_1
C_3
C_2
R_2
567 770Hz
567 852Hz
567 941Hz
567 1209Hz
567 1336Hz
567 1477Hz
100-200mV rms
0.5mfd
C_4
DIGIT
1
2
3
4
5
6
7
8
9
0
#
7402 OR 7428

Component values (Typical)

R_1	6.8 to 15K ohm
R_2	4.7K ohm
R_3	20K ohm
C_1	0.10mfd
C_2	1.0mfd 5V
C_3	2.2mfd 6V
C_4	250 μF 6V

OUTPUT LATCHING


+V
+V
567
8
1
R_L
R_A 10K
C_A
C_3
R_f 20K
UNLATCH
+V
+V
UNLATCH
567
8
1
R_L
R_f 20K
C_3

C_A prevents latch-up when power supply is turned on.

Figure 7

PRECISION VLF

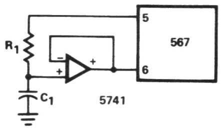
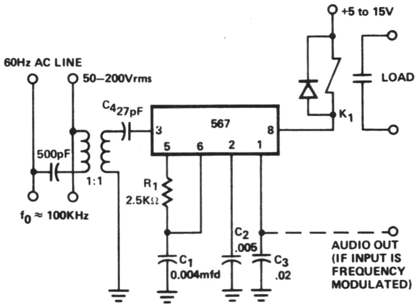

R_1
C_1
5741
5
6
567

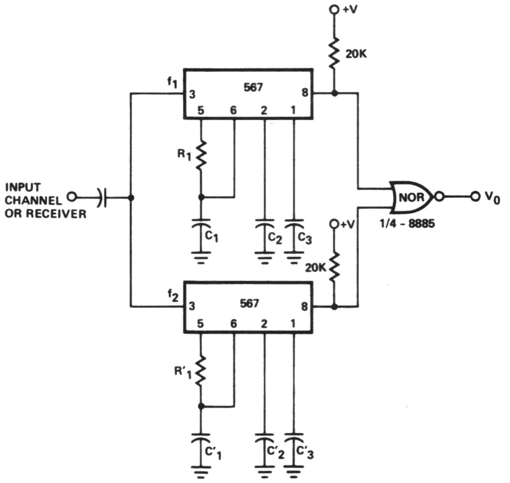
Figure 8

TYPICAL APPLICATIONS (Cont'd)

CARRIER-CURRENT REMOTE CONTROL OR INTERCOM

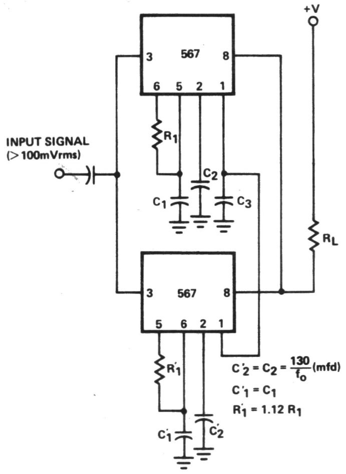

+5 to 15V
60Hz AC LINE
50–200Vrms
C_4 27pF
567
3
8
5
6
2
1
K_1
LOAD
500pF
1:1
$f_0 \approx$ 100KHz
R_1
2.5KΩ
C_1
0.004mfd
C_2
.005
C_3
.02
AUDIO OUT
(IF INPUT IS
FREQUENCY
MODULATED)

DUAL-TONE DECODER

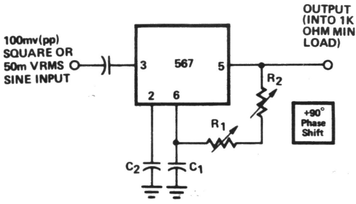

+V
20K
f_1
567
3
8
5
6
2
1
R_1
INPUT
CHANNEL
OR RECEIVER
C_1
C_2
C_3
+V
20K
NOR
1/4 - 8885
V_0
f_2
567
R'_1
C'_1
C'_2
C'_3

1. Resistor and capacitor values chosen for desired frequencies and bandwidth.
2. If C_3 is made large so as to delay turn-on of the top 567, decoding of sequential (f_1 f_2) tones is possible.

24% BANDWIDTH TONE DECODER


+V
567
3
8
6
5
2
1
R_1
INPUT SIGNAL
(>100mVrms)
C_1
C_2
C_3
R_L
567
R'_1
C'_1
C'_2
$C'_2 = C_2 = \frac{130}{f_0}$(mfd)
$C'_1 = C_1$
$R'_1 = 1.12\ R_1$

0° to 180° PHASE SHIFTER

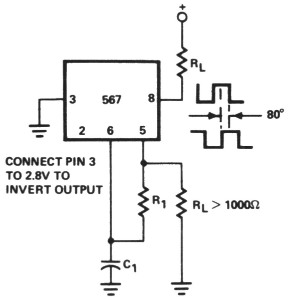

100mv(pp)
SQUARE OR
50m VRMS
SINE INPUT
567
3
5
2
6
OUTPUT
(INTO 1K
OHM MIN.
LOAD)
R_2
R_1
+90°
Phase
Shift
C_2
C_1

$R_2 \approx R_1/5$

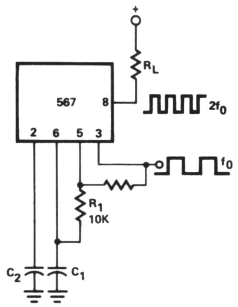
Adjust R_1 so that $\phi = 90°$ with control midway

TYPICAL APPLICATIONS (Cont'd)

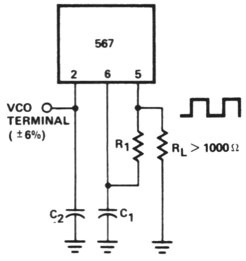
OSCILLATOR WITH QUADRATURE OUTPUT


+
R_L
3
567
8
2
6
5
80°
CONNECT PIN 3 TO 2.8V TO INVERT OUTPUT
R_1
R_L > 1000Ω
C_1

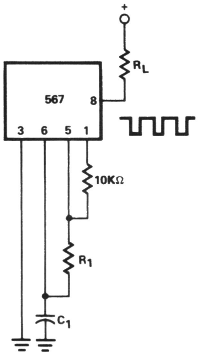
OSCILLATOR WITH DOUBLE FREQUENCY OUTPUT


+
R_L
567
8
2
6
5
3
$2f_0$
f_0
R_1
10K
C_2
C_1

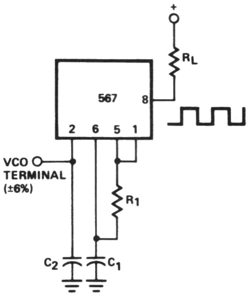
PRECISION OSCILLATOR WITH 20ns SWITCHING


567
2
6
5
VCO TERMINAL (±6%)
R_1
R_L > 1000Ω
C_2
C_1

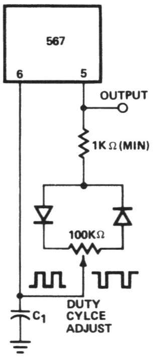
PULSE GENERATOR WITH 25% DUTY CYCLE


+
R_L
567
8
3
6
5
1
10KΩ
R_1
C_1

PRECISION OSCILLATOR TO SWITCH 100ma LOADS


+
R_L
567
8
2
6
5
1
VCO TERMINAL (±6%)
R_1
C_2
C_1

PULSE GENERATOR


567
6
5
OUTPUT
1KΩ (MIN)
100KΩ
C_1
DUTY CYLCE ADJUST

NOTE

Application information available on request.

SECTION 15
D-MOS FETS

Section 15—D-MOS FETS

SD203	Single Gate N-Channel Enhancement	339
SD205 (DMP4025DB)	Single Gate N-Channel Enhancement	344
SD210	Switch N-Channel Enhancement	348
SD211	Switch N-Channel Enhancement	348
SD212	Switch N-Channel Enhancement	348
SD213	Switch N-Channel Enhancement	348
SD214	Switch N-Channel Enhancement	348
SD215	Switch N-Channel Enhancement	348
SD217 (DMS4025DE)	Switch N-Channel Enhancement	353
SD220H	Power FET Single Gate N-Channel Enhancement	357
SD222DC	Power FET Single Gate N-Channel Enhancement	361
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SD303	Dual Gate N-Channel Enhancement	369
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SD6000	Dual Gate FETS N-Channel Enhancement	383
SD5000	Quad Analog Switch Arrays, Multiplexers and Driver	390
SD5001	Quad Analog Switch Arrays, Multiplexers and Driver	390
SD5002	Quad Analog Switch Arrays, Multiplexers and Driver	390
SD5200	Quad Analog Switch Arrays, Multiplexers and Driver	390
SD5301	8X2 Analog/Digital Switching Arrays	399
SD5302	8X2 Analog/Digital Switching Arrays	399

NOTE

*Any product listed in this section but not incorporated within the text may be obtained by writing Information Services at Signetics, 811 E. Arques, M/S 027, Sunnyvale, California 94086, or by calling (408) 746-1682.

D-MOS FET - SINGLE GATE N-CHANNEL ENHANCEMENT SD203

SD203-DC

DESCRIPTION

The Signetics D-MOS SD203 is a silicon, insulated gate, field effect transistor of the N-channel enhancement mode type. It is fabricated by the Signetics double-diffused process which gives superior high frequency performance up to 2GHz. A zener diode is connected between the gate and substrate of the SD201 and 203 that bypasses any voltage transient lying outside the range of -0.3V to +25.0V. Thus the gate of the 203 is protected against damage in all normal handling and operating situations.

The device is a general purpose transistor especially suited for amplifier designs in the UHF range (500MHz to 2GHz). It has extremely high transconductance, very low input capacitance and extremely low feedback capacitance. The SD203 combines high gain with low levels of noise, intermodulation distortion, and feedback capacitance. These parameters make it ideally suited for critical amplifier applications. This device is hermetically sealed in a modified 4-lead TO-72 package.

GENERAL FEATURES

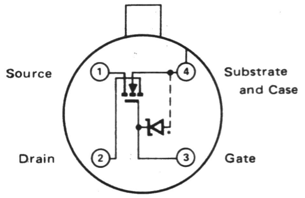
- **Ion-implanted for greater control and reliability**
- **Wide dynamic range**
- **Positive bias only**

SD203 FEATURES

- **High gain through UHF range: 10dB at 1.5GHz**
- **Low noise through UHF range: 3.5dB at 1.0GHz**
- **Low input capacitance: 3.0pF**
- **Low feedback capacitance: 0.20pF**
- **High drain-to-source voltage: +25V**
- **High forward transconductance: 20mmhos**

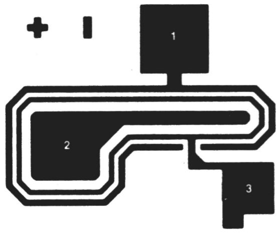
PIN CONFIGURATION

DC PACKAGE
(Top View)



ORDER PART NO.
SD203DC

SD203
SINGLE GATE RF DEVICE



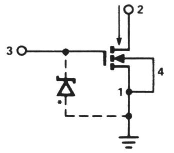
PAD NO.	PAD FUNCTION
1	SOURCE
2	DRAIN
3	GATE/DIODE

Die Size 19 X 22

ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise specified.

PARAMETER		RATING	UNIT
V_{DS}	Drain-to-source voltage		
	SD203	+20	V
V_{DB}	Drain-to-substrate voltage		
	SD203	+20	V
V_{GB}	DC gate-to-substrate voltage		
	SD203	-0.3, +10	V
I_D	Drain current	50	mA
T_{STG}	Temperature range		
	Storage	-65 to +175	°C
T_A	Operating	-55 to +125	°C
P_T	Transistor dissipation		
	At +25°C case temperature (Derate linearly to +125°C case temperature at the rate of 8.0mW/°C.)	1.2	W
	At +25°C free-air temperature (Derate linearly to +125°C free-air temperature at the rate of 2.0mW/°C.)	300	mW

COMMON SOURCE BIAS SCHEME



$+V_{DS} = 0 \rightarrow +20$ Volts
$+V_{GS} = 0 \rightarrow +4$ Volts
$+I_{DS} = 0 \rightarrow +20mA$

SD203-DC

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SD203			UNIT
			Min	Typ	Max	
BV_{DS}	Drain-to-source breakdown voltage	$V_{GS} = 0V$, $I_D < 1\mu A$	20	25		V
I_{GSS}	Gate leakage current	$V_{GS} = \pm 10V$, $V_{DS} = 0V$				nA
		$V_{GS} = +10V$, $V_{DS} = 0V$		0.001	1.0	μA
$I_D(OFF)$	Drain-to-source current	$V_{DS} = +15V$, $V_{GS} = 0V$		0.001	1.0	μA
I_{DSS}	Zero bias drain current	$V_{DS} = +15V$, $V_{GS} = 0V$		0.001	1.0	μA
V_T	Threshold voltage	$V_{DS} = V_{GS} = V_T$, $I_D = 1\mu A$	0.1	1.0	2.0	V
$r_{DS}(ON)$	Drain-to-source ON resistance	$V_{GS} = +5V$, $I_D = 1.0mA$		35	50	Ω

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

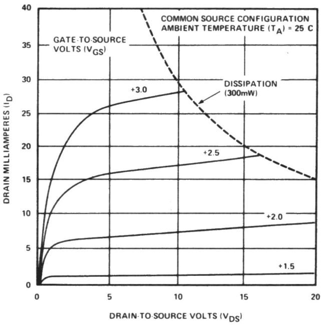
PARAMETER		TEST CONDITIONS	SD203			UNIT
			Min	Typ	Max	
gfs	Forward transconductance	$V_{DS} = +15V$, $I_D = 20mA$, f = 1kHz $V_{GS} \cong +2.5V$	17	20		mmhos
	Small signal short circuit capacitance	$V_{DS} = +15V$, f = 1MHz				
	C_{ISS} input	$I_D = 20mA$		3.0	3.6	pF
	C_{OSS} output	$I_D = 0A$		1.0	1.2	pF
	C_{RSS} reverse transfer	$I_D = 0A$		0.20	0.30	pF
G_{ps}	Power gain	$V_{DS} = +15V$, $I_D = 20mA$, f = 1GHz $V_{GS} \cong +2.5V$	8	10		dB
NF	Noise figure*	$V_{DS} = +15V$, $I_D = 20mA$, f = 1GHz $V_{GS} \cong +2.5V$		4.0	5.0	dB
P_I	Intercept point	$V_{DS} = 15V$, $I_D = 20mA$, f = 1GHz $\Delta f = 2MHz$		29		dBM

*NOTE

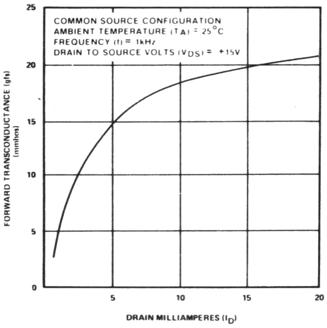
Measured in amplifier test fixture.

TYPICAL PERFORMANCE CHARACTERISTICS—SD203 (Cont'd)

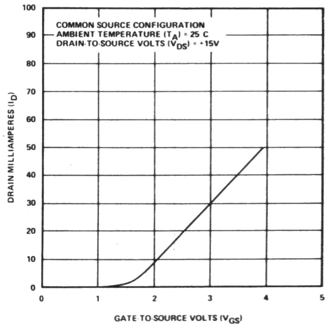
DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



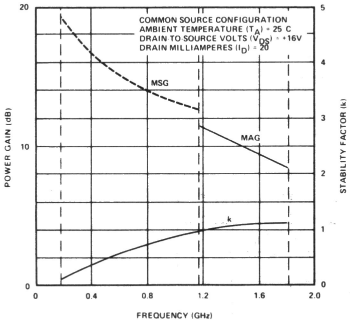
1kHz FORWARD TRANSCONDUCTANCE vs DRAIN CURRENT



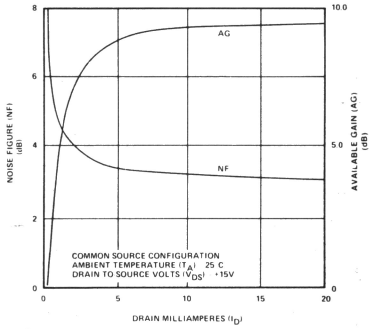
DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE



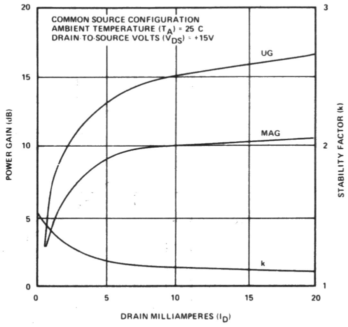
POWER GAIN vs FREQUENCY



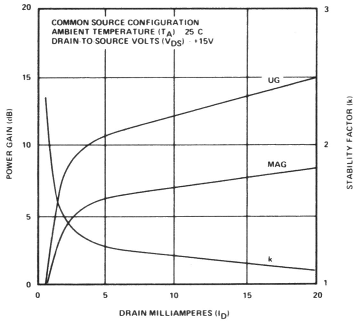
1.0GHz NOISE FIGURE AND AVAILABLE GAIN vs DRAIN CURRENT



1.5GHz POWER GAIN vs DRAIN CURRENT



1.8GHz POWER GAIN vs DRAIN CURRENT

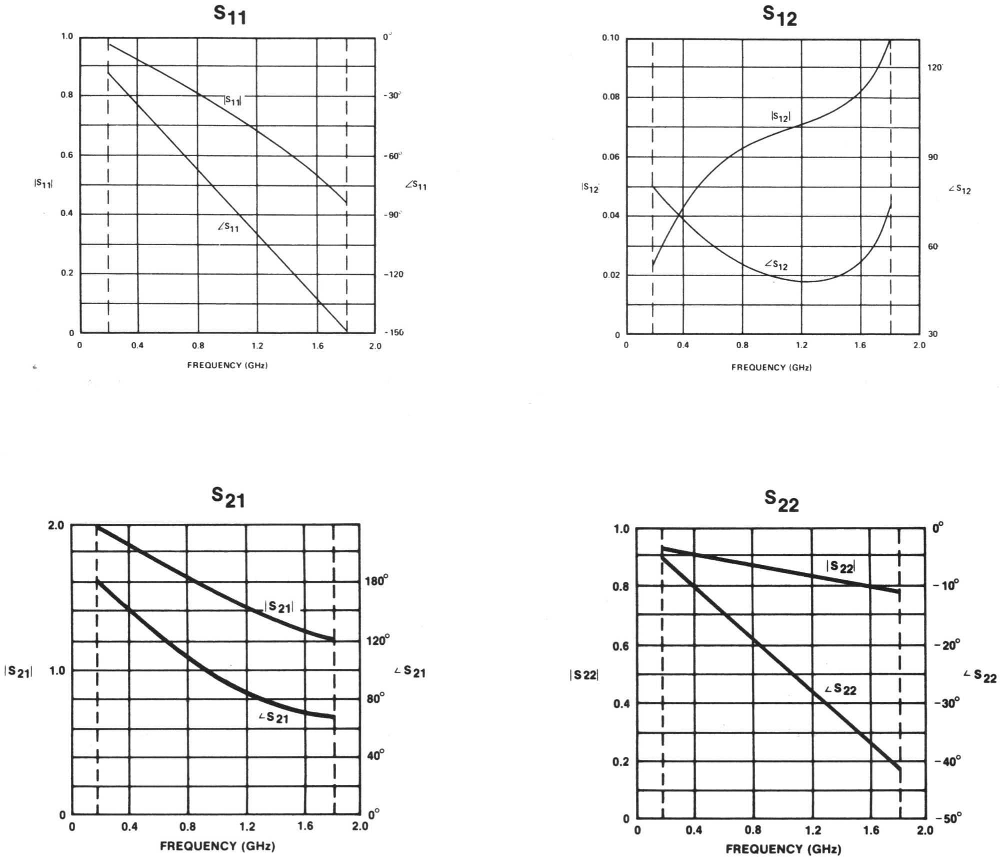


TYPICAL PERFORMANCE CHARACTERISTICS—SD203 (Cont'd)

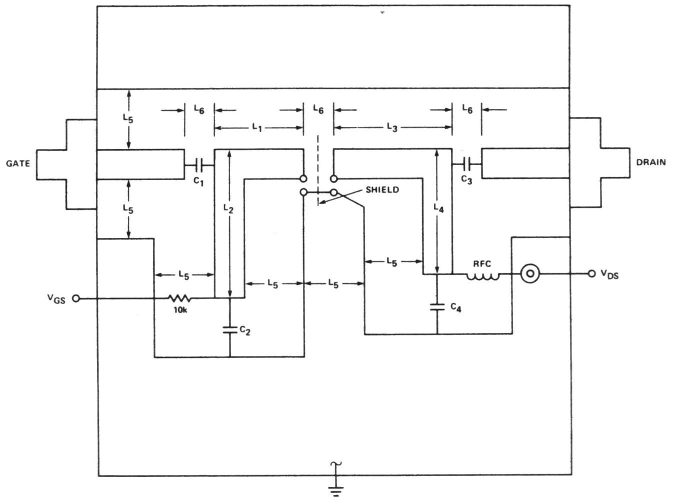
"S" PARAMETERS—SD203

COMMON SOURCE CONFIGURATION
AMBIENT TEMPERATURE (T_A) = 25°C

DRAIN MILLIAMPERES (I_D) = 20
DRAIN-TO-SOURCE VOLTS (V_{DS}) = +15



1GHz NOISE FIGURE TEST FIXTURE


GATE
DRAIN
L5
L6
L1
L6
L3
L6
C1
C3
SHIELD
L5
L2
L4
L5
RFC
VDS
L5
L5
L5
VGS
10k
C2
C4

Dialectric is 1/16" teflon-fiberglass (3M-K6096-11) all microstrip width = 0.175"

L1 = 0.48" C1 = C2 = C3 = 0.8-10pF
L2 = 1.52" Johanson 5201
L3 = 0.64" C4 =1.20pF
L4 = 1.36" Johanson 5501
L5 = 5/16" RFC = 10 turns 26 AWG 1/4" dia.
L6 = 1/8" 1000pF bypass
CORY FT4-01-2
Launchers — OSM248.2

NOTE

Shield and 4 tunable capacitors on ground plane side of amplifier.

D-MOS POWER FET—SINGLE GATE—N-CHANNEL ENHANCEMENT

SD205 (DMP4025DB)

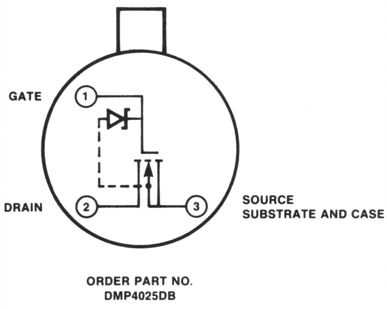
SD205DB

DESCRIPTION

The Signetics DMP4025 is a power MOSFET of the n-channel enhancement mode type designed for switching and amplifier applications requiring high current, high speed, and excellent linear transfer characteristics. Superior performance is achieved by utilizing the Signetics double-diffused MOS process which provides high gain, low drain to source "ON" resistance, low inter-electrode capacitance, and enhanced high frequency operation.

The device is hermetically sealed in a TO-39 package. The source, substrate, and case are connected to pin 3, which results in the package being at ground potential in the common source configuration.

PIN CONFIGURATION (Top View)



FEATURES

- **10dB gain @ 300MHz**
- **High I_{DS}: 800mA @ $V_{GS} = +10V$**
- **Withstands high VSWR**
- **No thermal runaway**
- **Low input capacitance**
- **Low feedback capacitance**
- **Switches 500mA in less than 2ns**
- **CMOS logic compatible input**
- **Extremely low drive current**

APPLICATIONS

- **Broadband power amplifier**
- **Power driver**
- **High speed switching**

ABSOLUTE MAXIMUM RATINGS[1] $T_A = +25°C$ unless otherwise specified

PARAMETER		RATING	UNIT
V_{DS}	Drain-to-source	+25	V
V_{GS}	Gate-to-source	+20	V
V_{DG}	Drain-to-gate	+20	V
$I_{D(ON)}$	Continuous drain current	0.8	A
I_Z	Gate (Zener) current	10	mA
P_D	Power dissipation		
	$T_A = 25°C^2$	1	W
	$T_C = 25°C^3$	4	W
	Power derating factors		
	Free air	10	mW/°C
	Infinite heat sink	40	mW/°C
θ_{JA}	Thermal resistance	100	°C/W
θ_{JC}	Thermal resistance	25	°C/W
T_{OP}	Operating Temperature	−55 to +125	°C
T_{STG}	Storage Temperature	−55 to +150	°C

NOTES

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Free air.
3. Infinite heat sink.

ELECTRICAL CHARACTERISTICS $T_A = +25°C$ unless otherwise specified

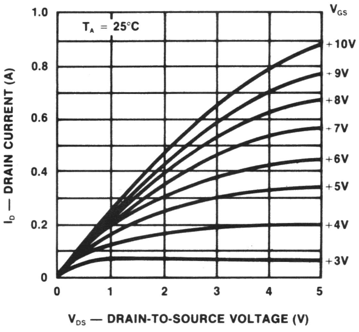
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
BV_{DSS}	Drain-source breakdown	$I_D = 10\mu A$, $V_{GS} = 0$	25	30		V
$V_{GS(th)}$	Gate threshold voltage	$I_D = 10\mu A$, $V_{GS} = V_{DS} = V_{GS(th)}$	0.5		2	V
$I_{D(ON)}$	Drain "ON" current [4]	$V_{GS} = V_{DS} = +10V$	1			A
$I_{D(OFF)}$	Drain "OFF" current	$V_{DS} = +25V$, $V_{GS} = 0$			1	μA
$r_{DS(ON)}$	Drain-source "ON" resistance[4]	$V_{GS} = +5V$, $I_D = 50mA$		6	8	Ω
		$V_{GS} = +10V$, $I_D = 50mA$		4	6	Ω
		$V_{GS} = +10V$, $I_D = 500mA$		4	6	Ω
g_{fs}	Forward Transconductance[4]	$V_{DS} = +15V$, $I_D = 200mA$	100	120		mmhos
	Capacitance	$V_{DS} = +10V$, $I_D = 0$, f = 1MHz				pF
C_{iss}	Input			11	13	
C_{rss}	Reverse transfer			2	3	
C_{oss}	Common source output			6	8	
N_F	Noise figure[5]	f = 300MHz, $V_{DS} = +10V$, $I_D = 100mA$		3.5	4.5	dB
G_{ps}	Common source power gain[5]	f = 300MHz, $V_{DS} = +10V$, $I_D = 100mA$	9	12		dB
t_{ON}		See test figure		1		nS
t_{OFF}		See test figure		3		nS
P_I	Intercept point	f = 300MHz, $V_{DS} = +12V$, $I_D = 400mA$		29		dBM

NOTES

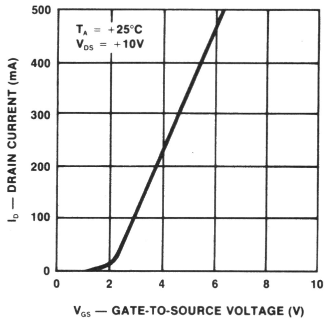
4. Pulsed @ 80μs, 1% duty cycle.
5. Measured in amplifier test fixture.

TYPICAL PERFORMANCE CHARACTERISTICS

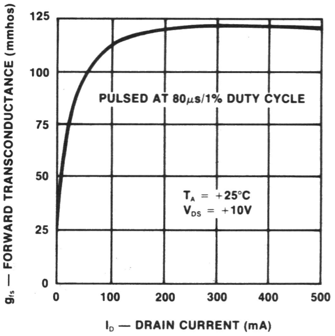
DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



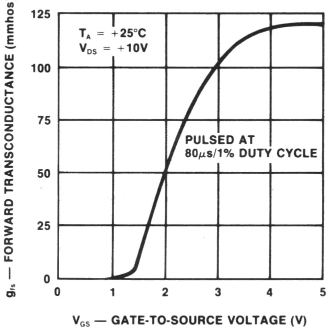
DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE



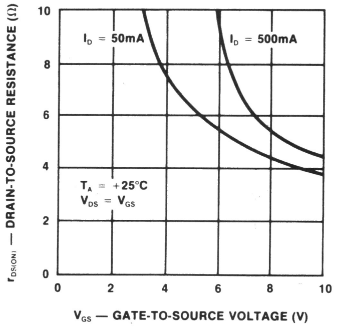
FORWARD TRANSCONDUCTANCE vs DRAIN CURRENT



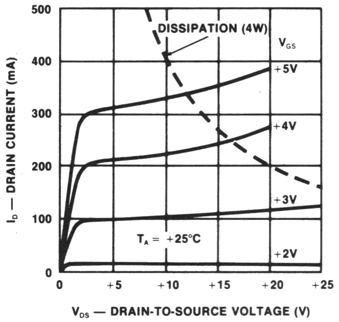
FORWARD TRANSCONDUCTANCE vs GATE-TO-SOURCE VOLTAGE



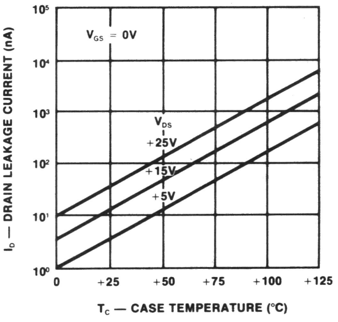
DRAIN-TO-SOURCE RESISTANCE vs GATE-TO-SOURCE VOLTAGE



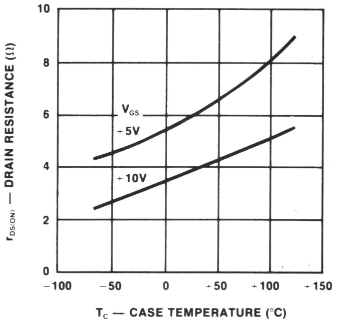
DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



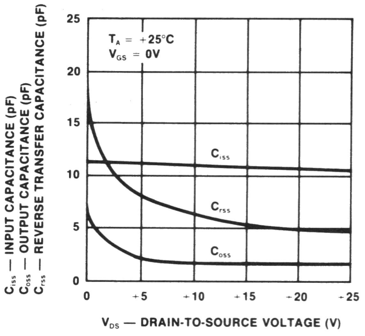
DRAIN LEAKAGE CURRENT vs CASE TEMPERATURE



DRAIN-TO-SOURCE RESISTANCE vs CASE TEMPERATURE

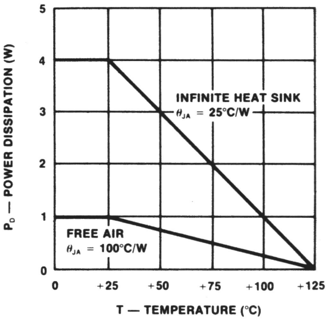


CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

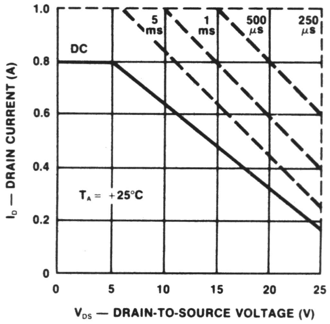


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

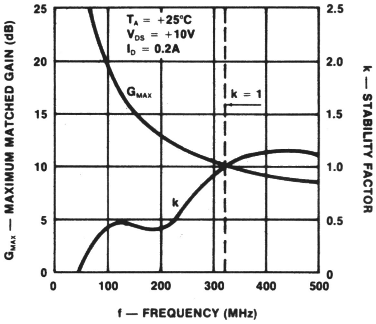
POWER DISSIPATION vs TEMPERATURE



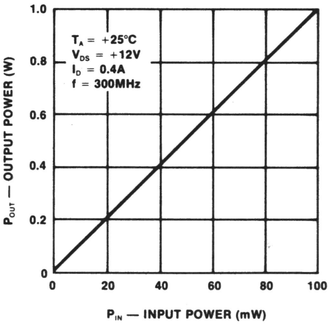
MAXIMUM SAFE OPERATING REGION



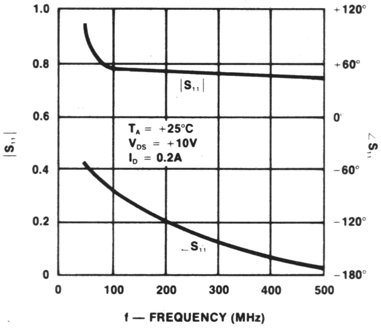
MAXIMUM MATCHED GAIN AND STABILITY FACTOR vs FREQUENCY



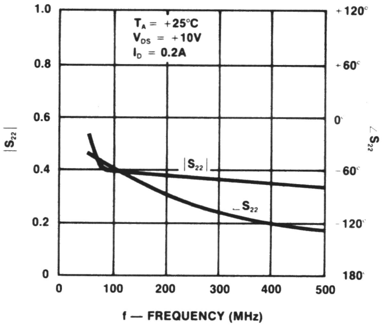
OUTPUT POWER vs INPUT POWER



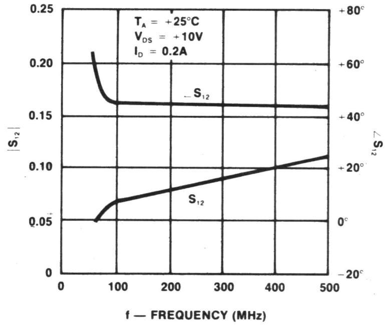
S_{11} vs FREQUENCY



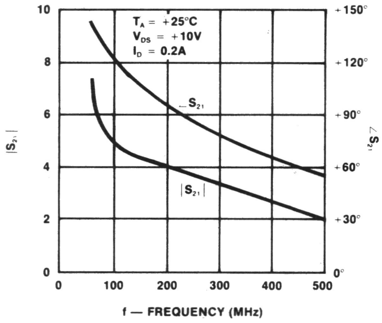
S_{22} vs FREQUENCY



S_{12} vs FREQUENCY



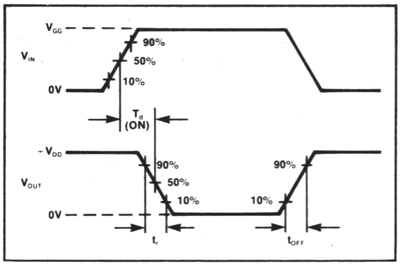
S_{21} vs FREQUENCY



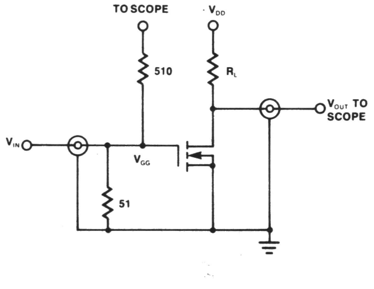
SWITCHING CHARACTERISTICS

V_{GG}(V)	V_{DD}(V)	R_L(Ω)	$t_{d(ON)}$(ns) Typ	t_r(ns) Typ	t_{OFF}(ns) Typ
5	5	100	<1	1	3
	10	200	<1	1	3
	20	390	<1	1	3
10	5	67	<1	1	3
	10	133	<1	1	3
	20	270	<1	1	3

SWITCHING WAVEFORMS


V_{GG}
V_{IN}
0V
90%
50%
10%
T_d (ON)
-V_{DD}
V_{OUT}
0V
90%
50%
10%
90%
10%
t_r
t_{OFF}

TEST CIRCUIT


TO SCOPE
V_{DD}
510
R_L
V_{OUT} TO SCOPE
V_{IN}
V_{GG}
51

NOTE
All resistors standard and are measured in ohms.

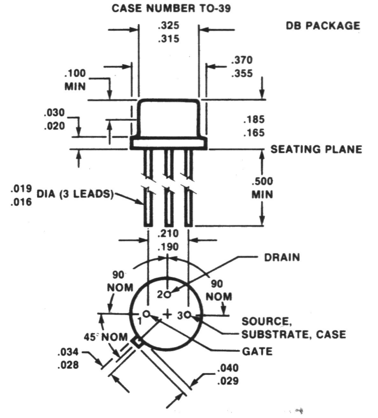
INPUT PULSE

t_d, t_r<1ns
PULSE WIDTH = 10ns
REP RATE = 1MHz

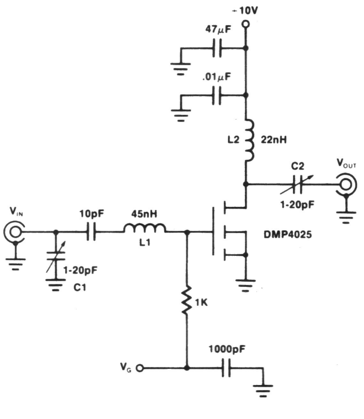
SAMPLING SCOPE

t_r<360ps
R_{IN} = 1MΩ
C_{IN} = 2.0pF

PACKAGE OUTLINE

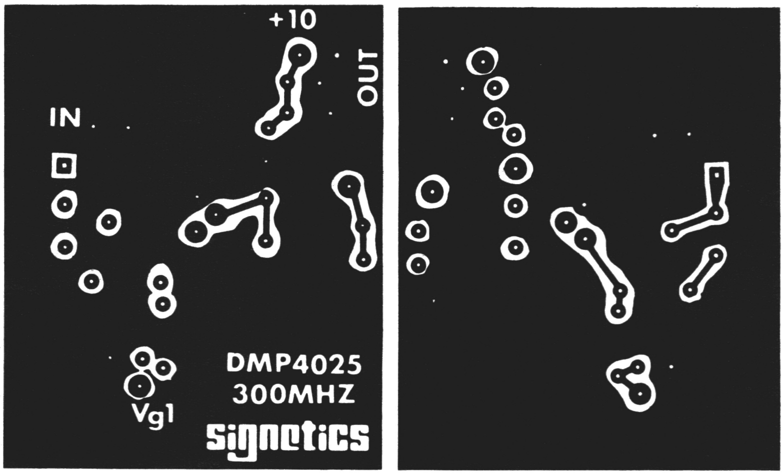

CASE NUMBER TO-39
DB PACKAGE
.325
.315
.370
.355
.100 MIN
.030
.020
.185
.165
SEATING PLANE
.019
.016
DIA (3 LEADS)
.500 MIN
.210
.190
DRAIN
90 NOM
90 NOM
2
1
3
SOURCE, SUBSTRATE, CASE
GATE
45° NOM
.034
.028
.040
.029

300MHz AMPLIFIER TEST CIRCUIT


+10V
47μF
.01μF
L2
22nH
C2
1-20pF
V_{OUT}
V_{IN}
10pF
45nH
L1
DMP4025
1-20pF
C1
1K
1000pF
V_G

C1, C2	Johanson P/N 5501
L1	J.W. Miller P/N 48A518MPC (1½ turns)
L2	J.W. Miller P/N 48A518MPC modified to ½ turn
L2, C2	Mounted on bottom side of board

300MHz AMPLIFIER PC BOARD LAYOUT


+10
OUT
IN
DMP4025
300MHZ
Vg1
signetics

D-MOS FET SWITCH N-CHANNEL ENHANCEMENT

SD210/SD211 SD212/SD213/SD214/SD215

SD210/211/212/213/214/215-DE

DESCRIPTION

The Signetics D-MOS SD210, 211, 212, 213, 214 and 215 are silicon, insulated gate, field effect transistors of the N-channel enhancement mode type. They are fabricated by the Signetics double-diffused process which gives high switching speed and low capacitance. A zener diode is connected between the gate and substrate of the SD211, 213 and 215. The diode bypasses any voltage transients which lie outside the range of -0.3V to +30V. Thus, the gate is protected against damage in all normal handling and operating situations. A drain-to-source breakdown of typically 35V makes the SD210 and 211 ideally suited for ±10V switch driver applications. Other characteristics allow them to be used as ±5V switches. The SD214 and 215 are designed to switch signals up to ±10V and the SD212 and 213 are designed to switch signals up to ±5V.

All the devices feature low gate node capacitance, extremely low drain node capacitance and very low feedback capacitance. Low "ON" resistance and hermetically sealed 4-lead TO-72 packages are also featured.

FEATURES

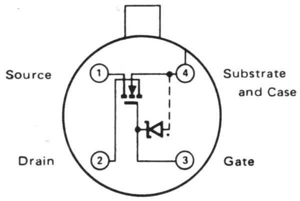
- **Low feedback capacitance: 0.30pF**
- **Low drain node capacitance: 1.3pF**
- **Low gate node capacitance: 2.4pF**
- **Low feedthrough and feedback transients**
- **Ion-implanted for greater reliability**
- **Excellent isolation from input to output: -120dB**
- **35V drain-to-source voltage for SD210/211**
- **Military qualifications pending**

APPLICATIONS

- **Switch driver**
- **Analog switch**
- **Multiplexers**
- **Digital switch**
- **Sample and hold**
- **Choppers**
- **A-TO-D converters**
- **D-TO-A converters**

PIN CONFIGURATION (Top View)

DE PACKAGE

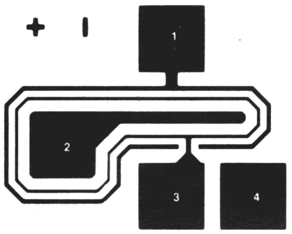


*Diode protection on SD 211/213/215 only.

ORDER PART NO.

SD210DE, SD211DE, SD212DE,
SD213DE, SD214DE, SD215DE

CHIP DIAGRAM



PAD NO.	PAD FUNCTION
1	SOURCE
2	DRAIN
3	GATE
4	DIODE

Die size 19X22

For SD211, 213, 215 bond gate and diode to same point.

ABSOLUTE MAXIMUM RATINGS (all devices)

PARAMETER	RATING	UNIT
Drain current (I_D)	50	mA
Ambient temperature range		
Storage	-65 to +175	°C
Operating	-55 to +125	°C
Transistor dissipation (P_T)		
At 25°C case temperature (Derate linearly to +125°C case temperature at the rate of 8.0mW/°C.)	1.2	W
At 25°C free-air temperature (Derate linearly to +125°C free-air temperature at the rate of 2.0mW/°C.)	300	mW

ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$ unless otherwise specified.*

PARAMETER		SD210	SD211	SD212	SD213	SD214	SD215	UNIT
V_{DS}	Drain-to-source	+30	+30	+10	+10	+20	+20	Vdc
V_{SD}	Source-to-drain*	+10	+10	+10	+10	+20	+20	Vdc
V_{DB}	Drain-to-substrate	+30	+30	+15	+15	+25	+25	Vdc
V_{SB}	Source-to-substrate	+15	+15	+15	+15	+25	+25	Vdc
V_{GS}	Gate-to-source	±40	-15 +25	±40	-15 +25	±40	-25 +30	Vdc
V_{GB}	Gate-to-substrate	±40	-0.3 +25	±40	-0.3 +25	±40	-0.3 +30	Vdc
V_{GD}	Gate-to-drain	±40	-30 +25	±40	-15 +25	±40	-25 +30	Vdc

*NOTE

Refer to test conditions specified in Electrical Characteristics Table.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SD210			SD211			SD212			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Breakdown voltage												
BV_{DS}	Drain-to-source	$V_{GS} = V_{BS} = 0V$, $I_D = 10\mu A$	30	35		30	35					V
		$V_{GS} = V_{BS} = -5V$, $I_S = 10nA$	10	25		10	25		10	25		V
BV_{SD}	Source-to-drain	$V_{GD} = V_{BD} = -5V$ $I_D = 10nA$	10			10			10			V
BV_{DB}	Drain-to-substrate	$V_{GB} = 0V$, source OPEN $I_D = 10nA$	15			15			15			V
BV_{SB}	Source-to-substrate	$V_{GB} = 0V$, drain OPEN $I_S = 10\mu A$	15			15			15			V
Leakage current												
$I_{DS}(OFF)$	Drain-to-source	$V_{GS} = V_{BS} = -5V$ $V_{DS} = +10V$		1	10		1	10		1	10	nA
$I_{SD}(OFF)$	Source-to-drain	$V_{GD} = V_{BD} = -5V$ $V_{SD} = +10V$		1	10		1	10		1	10	nA
I_{GBS}	Gate	$V_{DB} = V_{SB} = 0V$										
		$V_{GB} = \pm 40V$			0.1						0.1	nA
		$V_{GB} = +25V$						10				μA
V_T	Threshold voltage	$V_{DS} = V_{GS} = V_T$, $I_S = 1\mu A$ $V_{SB} = 0V$	0.5	1.0	2.0	0.5	1.0	2.0	0.1	1.0	2.0	V
$r_{DS}(ON)$	Drain-to-source resistance	$I_D = 1.0mA$, $V_{SB} = 0$										
		$V_{GS} = +5V$		50	70		50	70		50	70	Ω
		$V_{GS} = +10V$		30	45		30	45		30	45	Ω
		$V_{GS} = +15V$		23			23			23		Ω
		$V_{GS} = +20V$		19			19			19		Ω
		$V_{GS} = +25V$		17						17		Ω

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25\,°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SD213			SD214			SD215			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Breakdown voltage												
BV_{DS}	Drain-to-source	$V_{GS} = V_{BS} = -5V$, $I_S = 10nA$	10	25		20	25		20	25		V
BV_{SD}	Source-to-drain	$V_{GD} = V_{BD} = -5V$ $I_D = 10nA$	10			20			20			V
BV_{DB}	Drain-to-substrate	$V_{GB} = 0V$, source OPEN $I_D = 10nA$	15			25			25			V
BV_{SB}	Source-to-substrate	$V_{GB} = 0V$, drain OPEN $I_S = 10\mu A$	15			25			25			V
Leakage current												
$I_{DS}(OFF)$	Drain-to-source	$V_{GS} = V_{BS} = -5V$										
		$V_{DS} = +10V$		1	10							nA
		$V_{DS} = +20V$					1	10		1	10	nA
$I_{SD}(OFF)$	Source-to-drain	$V_{GD} = V_{BD} = -5V$										
		$V_{SD} = +10V$		1	10							nA
		$V_{SD} = +20V$					1	10		1	10	nA
I_{GBS}	Gate	$V_{DB} = V_{SB} = 0V$										
		$V_{GB} = \pm 40V$						0.1				nA
		$V_{GB} = +25V$			10							μA
		$V_{GB} = +30V$									10	μA
V_T	Threshold voltage	$V_{DS} = V_{GS} = V_T$, $I_S = 1\mu A$ $V_{SB} = 0V$	0.1	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	V
$r_{DS}(ON)$	Drain-to-source resistance	$I_D = 1.0mA$, $V_{SB} = 0$										
		$V_{GS} = +5V$		50	70		50	70		50	70	Ω
		$V_{GS} = +10V$		30	45		30	45		30	45	Ω
		$V_{GS} = +15V$		23			23			23		Ω
		$V_{GS} = +20V$		19			19			19		Ω
		$V_{GS} = +25V$					17			17		Ω

AC ELECTRICAL CHARACTERISTICS $T_A = 25\,°C$ unless otherwise specified.

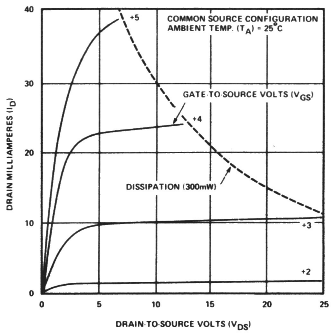
PARAMETER		TEST CONDITIONS	SD210			SD211			SD212			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
gfs	Forward transconductance	$V_{DS} = 10V$, $V_{SB} = 0V$ $I_D = 20mA$, $f = 1kHz$	10	15		10	15		10	15		mmhos
Small Signal Capacitances (See capacitance model)		$V_{DS} = 10V$, $f = 1MHz$ $V_{GS} = V_{BS} = -15V$										
$C_{(GS+GD+GB)}$	Gate node			2.4	3.5		2.4	3.5		2.4	3.5	pF
$C_{(GD+DB)}$	Drain node			1.3	1.5		1.3	1.5		1.3	1.5	pF
$C_{(GS+SB)}$	Source node			3.5	4.0		3.5	4.0		3.5	4.0	pF
C_{DG}	Reverse transfer			0.3	0.5		0.3	0.5		0.3	0.5	pF

AC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25\,°C$ unless otherwise specified.

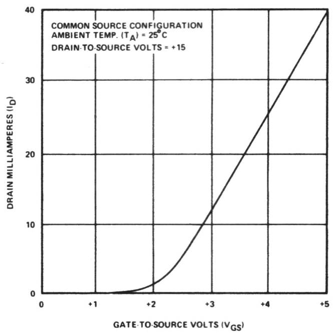
PARAMETER		TEST CONDITIONS	SD213			SD214			SD215			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
gfs	Forward transconductance	$V_{DS} = 10V$, $V_{SB} = 0V$ $I_D = 20mA$, $f = 1kHz$	10	15		10	15		10	15		mmhos
Small Signal Capacitances (See capacitance model)		$V_{DS} = 10V$, $f = 1MHz$ $V_{GS} = V_{BS} = -15V$										
$C_{(GS+GD+GB)}$	Gate node			2.4	3.5		2.4	3.5		2.4	3.5	pF
$C_{(GD+DB)}$	Drain node			1.3	1.5		1.3	1.5		1.3	1.5	pF
$C_{(GS+SB)}$	Source node			3.5	4.0		3.5	4.0		3.5	4.0	pF
C_{DG}	Reverse transfer			0.3	0.5		0.3	0.5		0.3	0.5	pF

TYPICAL PERFORMANCE CHARACTERISTICS

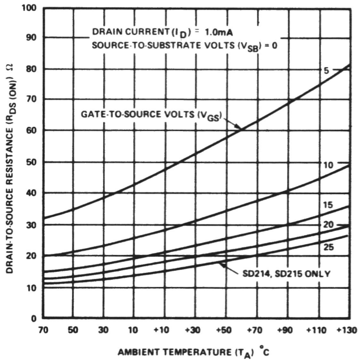
DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



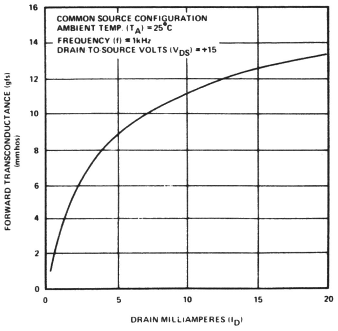
DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE



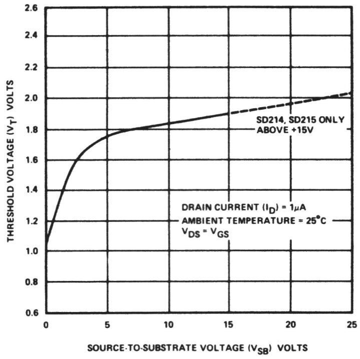
DRAIN-TO-SOURCE RESISTANCE vs TEMPERATURE



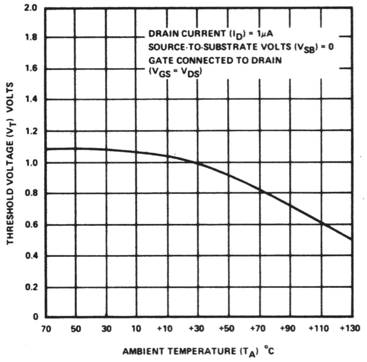
1kHz FORWARD TRANSCONDUCTANCE vs DRAIN CURRENT



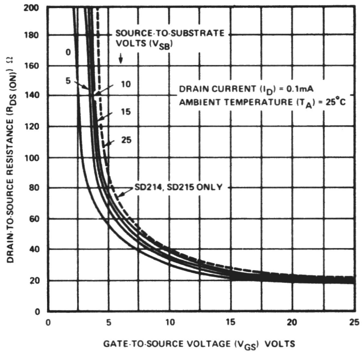
THRESHOLD VOLTAGE vs SOURCE-TO-SUBSTRATE VOLTAGE



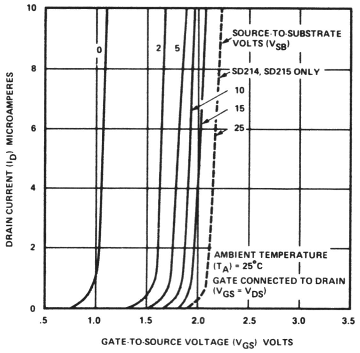
THRESHOLD VOLTAGE vs TEMPERATURE



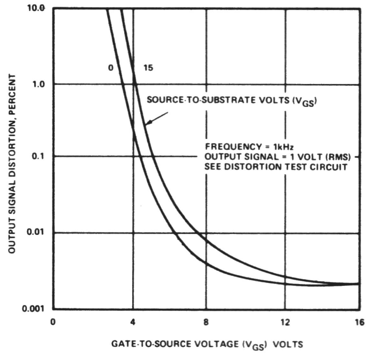
DRAIN-TO-SOURCE RESISTANCE vs GATE-TO-SOURCE VOLTAGE



DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

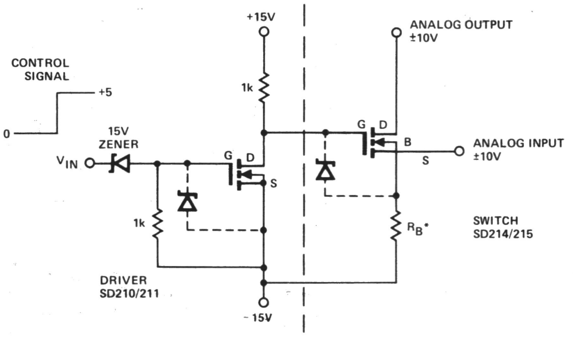


DISTORTION vs GATE-TO-SOURCE VOLTAGE



TYPICAL APPLICATION

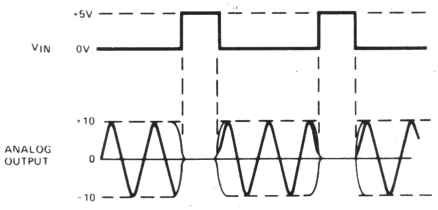
D-MOS DRIVER/SWITCH


+15V
ANALOG OUTPUT
±10V
CONTROL
SIGNAL
+5
0
1k
15V
ZENER
V_{IN}
G
D
S
G
D
B
S
ANALOG INPUT
±10V
1k
R_B*
SWITCH
SD214/215
DRIVER
SD210/211
-15V

R_B*Optional current limiting resistor

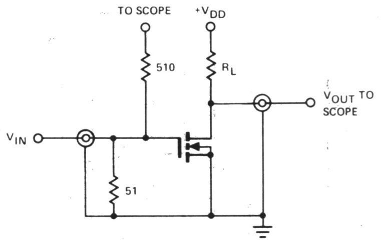
NOTE
*All resistors standard and are measured in ohms.

TYPICAL SWITCHING WAVEFORM



TEST CIRCUITS

SWITCHING

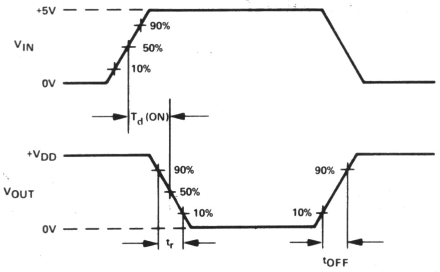

TO SCOPE
$+V_{DD}$
510
R_L
V_{OUT} TO
SCOPE
V_{IN}
51

Input pulse: t_d, $t_r < 1$ns,
Pulse width = 100ns,
Rep rate = 1MHz

SAMPLING SCOPE

$t_r < 360$ps
$R_{IN} = 1M\Omega$
$C_{IN} = 2.0$pF

TYPICAL SWITCHING WAVEFORM

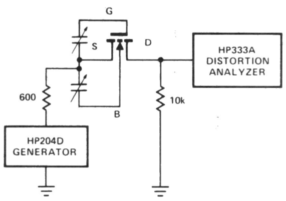


SWITCHING CHARACTERISTICS

		t_d(ON) (ns)		t_r(ns)		t_{OFF}(ns)	
V_{DD}	R_L	Typ	Max	Typ	Max	Typ	Max
5	680	0.6	1.0	0.7	1.0	9.0	*
10	680	0.7		0.8		9.0	*
15	1k	0.9		1.0		14.0	*

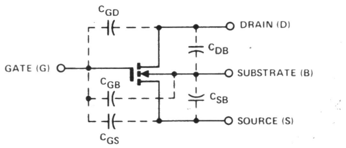
*t_{OFF} is dependent on R_L and C_L and does not depend on the device characteristics.

DISTORTION


G
S
D
HP333A
DISTORTION
ANALYZER
600
B
10k
HP204D
GENERATOR

NOTE: All resistors standard and are measured in ohms.

CAPACITANCE MODEL


C_{GD}
DRAIN (D)
C_{DB}
GATE (G)
SUBSTRATE (B)
C_{GB}
C_{SB}
SOURCE (S)
C_{GS}

D-MOS FET SWITCH N-CHANNEL ENHANCEMENT

SD217 (DMS4025DE)

DESCRIPTION

The Signetics DMS4025DE is a power MOSFET of the n-channel enhancement mode type designed for switching applications requiring high current, high speed, low "ON" resistance and excellent node-to-node isolation. Superior performance is achieved by utilizing the Signetics double-diffused MOS process which provides high gain, low drain to source "ON" resistance, low inter-electrode capacitance, and enhanced high frequency operation. The DMS4025DE is designed to switch analog signals up to ±7.5 volts. The device is hermetically sealed in a 4-lead TO-72 package.

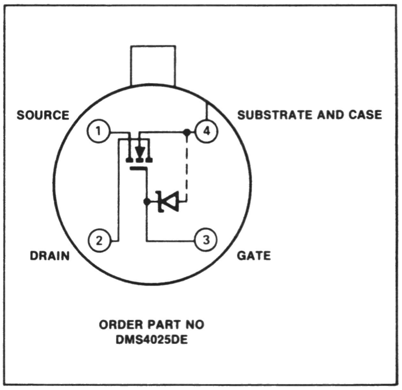
FEATURES

- **Low node capacitances**
- **Low feedthrough and feedback transients**
- **Excellent isolation from input to output**
- **CMOS logic compatible input**
- **Extremely low drive current**
- **Switches 500mA in less than 2ns**

APPLICATIONS

- **Switch driver**
- **Analog switch**
- **Multiplexers**
- **Digital switch**
- **Sample and hold**
- **A-to-D converters**
- **D-to-A converters**

PIN CONFIGURATION (Top View)



ORDER PART NO
DMS4025DE

ABSOLUTE MAXIMUM RATINGS[1] $T_A = +25°C$ unless otherwise specified

PARAMETER		RATING	UNIT
V_{DS}	Drain-to-source	+25	V
V_{SD}	Source-to-drain[2]	+15	V
V_{DB}	Drain-to-body	+22.5	V
V_{SB}	Source-to-body	+22.5	V
V_{GB}	Gate-to-body	+30	V
V_{GS}	Gate-to-source	±22.5	V
V_{GD}	Gate-to-drain	±22.5	V
$I_{D(ON)}$	Continuous drain current	800	mA
P_D	Power dissipation		
	$T_A = +25°C$[3]	300	mW
	$T_C = +25°C$[4]	1.2	W
	Power derating factors		
	Free air	3	mW/°C
	Infinite heat sink	12	mW/°C
θ_{JA}	Thermal resistance	330	°C/W
θ_{JC}	Thermal resistance	83.5	°C/W
T_{OP}	Operating temperature	−55 to +125	°C
T_{STG}	Storage temperature	−55 to +150	°C

NOTES

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. See test conditions in dc electrical characteristics section.
3. Free air.
4. Infinite heat sink.

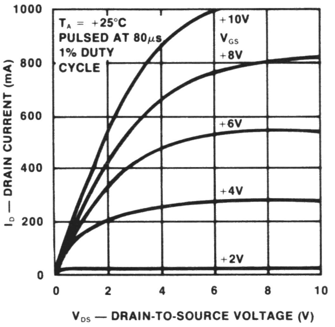
ELECTRICAL CHARACTERISTICS $T_A = +25°C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
BV_{DS}	Breakdown voltage drain-source	$V_{GS} = V_{BS} = 0V, I_D = 10\mu A$	25	30		V
		$V_{GS} = V_{BS} = -5V, I_D = 100nA$	15			V
BV_{SD}	Breakdown voltage source-drain	$V_{GD} = V_{BD} = -5V, I_S = 100nA$	15			V
BV_{DB}	Breakdown voltage drain-body	$V_{GB} = 0V, I_D = 100nA$, source open	22.5			V
BV_{SB}	Breakdown voltage source-body	$V_{GB} = 0V, I_S = 100nA$, drain open	22.5			V
$I_{D(OFF)}$	Leakage current drain node	$V_{GS} = V_{BS} = -5V, V_{DS} = +15V$		10	100	nA
$I_{S(OFF)}$	Leakage current source node	$V_{GD} = V_{BD} = -5V, V_{SD} = +15V$		10	100	nA
$I_{G(OFF)}$	Leakage current gate node (OFF)	$V_{GB} = 0V, V_{GS} = V_{GD} = -22.5V$		1	100	nA
$I_{G(ON)}$	Leakage current gate node (ON)	$V_{GB} = +30V, V_{GS} = V_{GD} = +22.5V$		.05	10	μA
$I_{D(ON)}$	Drain "ON" current [5]	$V_{GS} = V_{DS} = +10V, V_{SB} = 0V,$	1			A
V_T	Threshold voltage	$V_{DS} = V_{GS} = V_T, V_{SB} = 0V,$ $I_D = 10\mu A$	0.1	1	2	V
$r_{DS(ON)}$	Drain-source "ON" resistance[5]	$V_{GS} = +5V, I_D = 50mA$		6	8	Ω
		$V_{GS} = +10V, I_D = 50mA$		4	6	Ω
		$V_{GS} = +10V, I_D = 500mA$		4	6	Ω
g_{fs}	Forward Transconductance[5]	$V_{DS} = +15V, I_D = 200mA$	100	120		mmhos
	Capacitances	(See capacitance model) $V_{DS} = +10V,$ $V_{GS} = V_{BS} = -15V, I_D = 0A, f = 1 MHz$				
$C_{(GS+GD+GB)}$	Gate node			25	30	pF
$C_{(GD+DB)}$	Drain node			13	15	pF
$C_{(GS+SB)}$	Source node			35	40	pF
C_{DG}	Reverse transfer			3	5	pF
t_{ON}	Turn ON time	See switching time test circuit		2	4	ns
t_{OFF}	Turn OFF time			3	5	ns

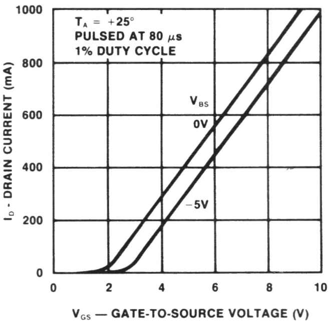
NOTES
5. Pulsed @ 80µs, 1% duty cycle.

TYPICAL PERFORMANCE CHARACTERISTICS

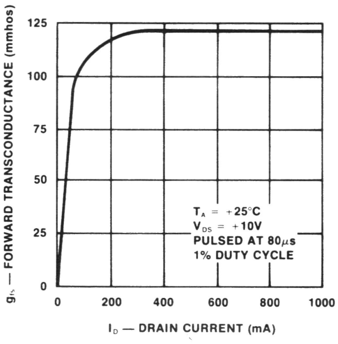
DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

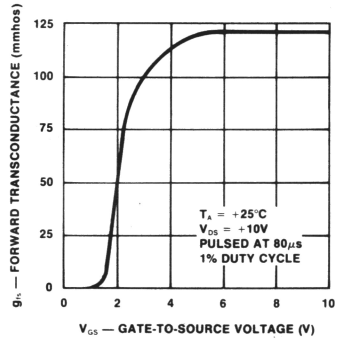


FORWARD TRANSCONDUCTANCE vs DRAIN CURRENT

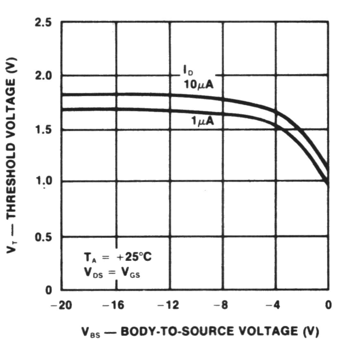


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

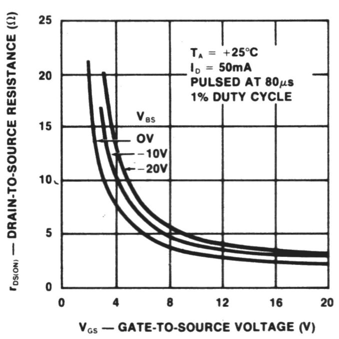
FORWARD TRANSCONDUCTANCE vs GATE-TO-SOURCE VOLTAGE



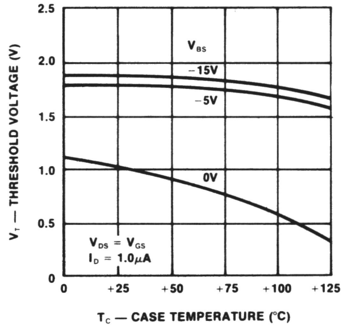
THRESHOLD VOLTAGE vs BODY-TO-SOURCE VOLTAGE



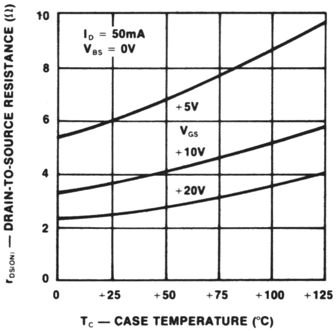
DRAIN-TO-SOURCE RESISTANCE vs GATE-TO-SOURCE VOLTAGE



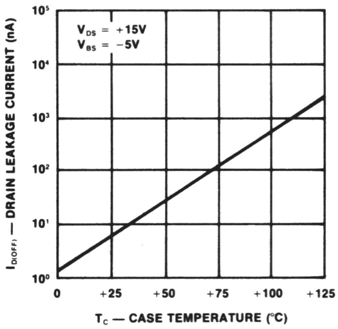
THRESHOLD VOLTAGE vs CASE TEMPERATURE



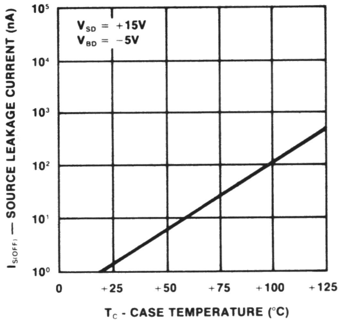
DRAIN-TO-SOURCE RESISTANCE vs CASE TEMPERATURE



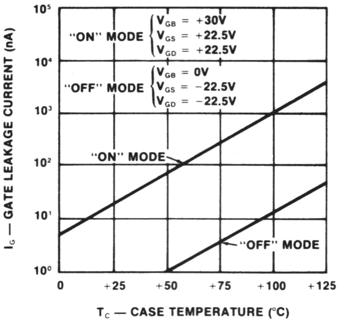
DRAIN LEAKAGE CURRENT vs CASE TEMPERATURE



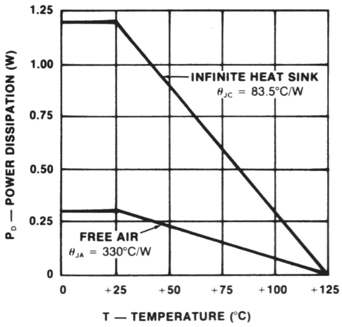
SOURCE LEAKAGE CURRENT vs CASE TEMPERATURE



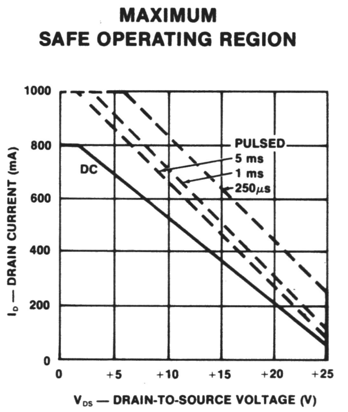
GATE LEAKAGE CURRENT vs CASE TEMPERATURE



POWER DISSIPATION vs TEMPERATURE



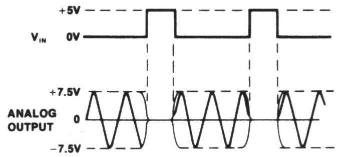
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)



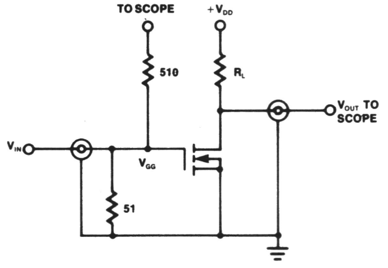
SWITCHING CHARACTERISTICS

V_{GG}(V)	V_{DD}(V)	R_L(Ω)	$t_{d(ON)}$(ns) Typ	t_r(ns) Typ	t_{OFF}(ns) Typ
5	5	100	<1	1	3
	10	200	<1	1	3
	20	390	<1	1	3
10	5	67	<1	1	3
	10	133	<1	1	3
	20	270	<1	1	3

TYPICAL WAVEFORMS



TEST CIRCUIT

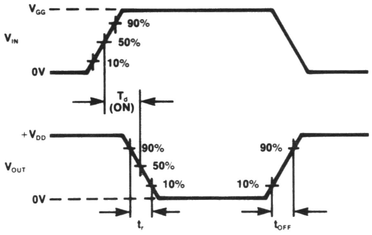

TO SCOPE
$+V_{DD}$
510
R_L
V_{OUT} TO SCOPE
V_{IN}
V_{GG}
51

NOTE
All resistors standard and are measured in ohms.

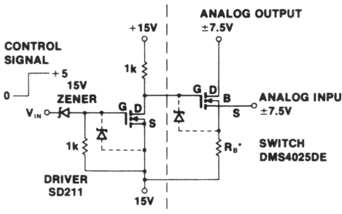
INPUT PULSE
t_d, t_r <1ns
PULSE WIDTH = 10ns
REP RATE = 1MHz

SAMPLING SCOPE
t_r <360ps
R_{IN} = 1MΩ
C_{IN} = 2.0pF

SWITCHING WAVEFORMS



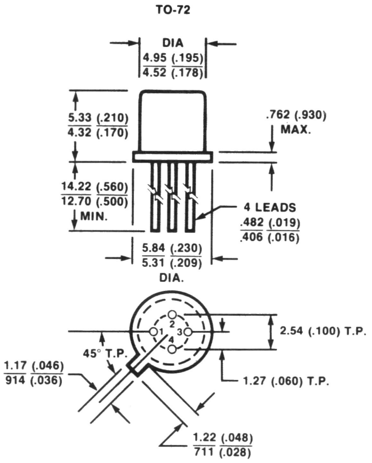
D-MOS DRIVER/SWITCH APPLICATION


CONTROL SIGNAL
+5
0
+15V
1k
15V ZENER
V_{IN}
G
D
S
1k
DRIVER SD211
15V
ANALOG OUTPUT ±7.5V
G
D
B
S
ANALOG INPUT ±7.5V
R_B*
SWITCH DMS4025DE

R_B* OPTIONAL CURRENT LIMITING RESISTOR

NOTE
All resistors standard and are measured in ohms.

PACKAGE INFORMATION


TO-72
DIA
4.95 (.195)
4.52 (.178)
5.33 (.210)
4.32 (.170)
.762 (.930) MAX.
14.22 (.560)
12.70 (.500)
MIN.
4 LEADS
.482 (.019)
.406 (.016)
5.84 (.230)
5.31 (.209)
DIA.
1
2
3
4
2.54 (.100) T.P.
45° T.P.
1.17 (.046)
914 (.036)
1.27 (.060) T.P.
1.22 (.048)
711 (.028)

NOTES
1. Lead Material: Kover or equivalent—gold plated.
2. Body Material: Eyelet, Kover or equivalent—gold plated, glass body
3. Lid Material: Nickel, weld seal
4. All dimensions shown in parenthesis are English (inches)

D-MOS POWER FET SINGLE GATE N-CHANNEL ENHANCEMENT SD220H

PRELIMINARY SPECIFICATION

DESCRIPTION

The Signetics SD220 is a POWER MOSFET of the N-channel enhancement mode type designed for switching and amplifier applications requiring high voltage, high current, high speed, and exceptional linear transfer characteristics. Superior performance is achieved by utilizing the Signetics D-MOS process which provides high gain, low inter-electrode capacitances, low drain-to-source "ON" resistance, and enhanced high frequency operation.

The device is hermetically sealed in a TO-39 package. The source, substrate, and case are internally connected.

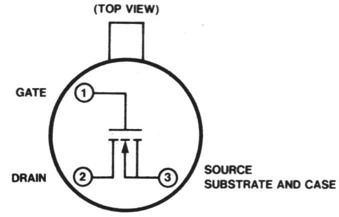
FEATURES

- **Low "ON" resistance: $<10\Omega$ @ 500mA**
- **High current: 500mA dc**
- **High voltage: $V_{DS} > +60V$**
- **Low input drive power**
- **Low inter-electrode capacitances**
- **Linear transfer characteristics**
- **No secondary breakdown**
- **Withstands high VSWR**

APPLICATIONS

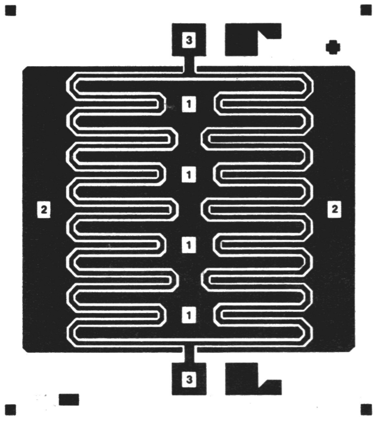
- **Power amplification**
- **Power driver**
- **High speed switching**
- **Switching power supplies**

PIN CONFIGURATION



ORDER PART NO.
SD220H

CHIP DIAGRAM



PAD NO.	PAD FUNCTION
1	DRAIN
2	SOURCE
3	GATE

ABSOLUTE MAXIMUM RATINGS[1] $T_A = +25°C$ unless otherwise specified.

PARAMETER		RATING	UNIT
V_{DS}	Drain-to-source	+60	V
V_{GS}	Gate-to-source	±20	V
V_{DG}	Drain-to-gate	+60	V
		−20	
$I_D(ON)$	"ON" drain current		
	Continuous	500	mA
	Pulsed (80μs, 1% duty cycle)	800	mA
P_D	Power dissipation		
	$T_A = +25°C$[2]	1	W
	$T_C = +25°C$[3]	6.25	W
	Power derating factors		
	Free air	8	mW/°C
	Infinite heat sink	50	mW/°C
Θ_{JA}	Thermal resistance	125	°C/W
Θ_{JC}	Thermal resistance	20	°C/W
T_{op}	Operating temperature	−55 to +125	°C
T_{STG}	Storage temperature	−55 to +150	°C

NOTES

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Free air.
3. Infinite heat sink.

PRELIMINARY SPECIFICATION

ELECTRICAL CHARACTERISTICS $T_A = +25°C$

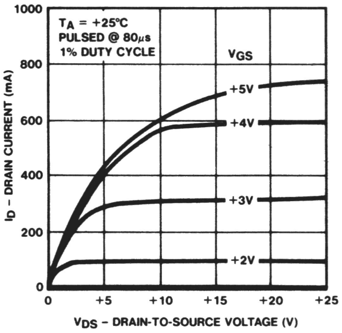
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
BV_{DS}	Drain-source Breakdown voltage	$V_{GS} = V_{SB} = 0$, $I_D = 1\mu A$	60	100		V
I_{GSS}	Gate leakage current	$V_{GSS} = \pm 20V$			1.0	nA
$I_D(OFF)$	Drain leakage current	$V_{DS} = +60V$, $V_{GS} = 0$		0.1	1.0	μA
$I_D(ON)$	Drain "ON" current	$V_{DS} = +6V$, $V_{GS} = +10V$	500			mA
$I_D(ON)$	Drain "ON" current^4	$V_{DS} = +10V$, $V_{GS} = +10V$	600	700		mA
V_T	Threshold voltage	$V_{DS} = V_{GS} = V_T$, $I_D = 10\mu A$ $V_{DS} = V_{GS} = V_T$, $I_D = 1mA$	0.1 0.5	0.8 1.5	2.3 3.0	V V
$r_{DS}(ON)$	Drain-source "ON" resistance^4	$V_{GS} = +5V$, $I_D = 50mA$ $V_{GS} = +10V$, $I_D = 50mA$ $V_{GS} = +10V$, $I_D = 500mA$		7.5 6.5 9	10 9 12	Ω Ω Ω
g_{fs}	Forward transconductance^4	$V_{DS} = +30V$, $I_D = 300mA$	220	250		mmhos
 C_{iss} C_{oss} C_{rss}	Capacitances Input Output Reverse transfer	$V_{DS} = +30V$, $I_D = 0$, $f = 1MHz$		 12 2.8 0.6	 15 3.5 1.0	 pF pF pF
$t_d(ON)$ t_r t_f	Turn-ON Delay Time Rise Time Fall Time	See switching Time test Circuit		1 1 3	2 3 5	ns ns ns

NOTE

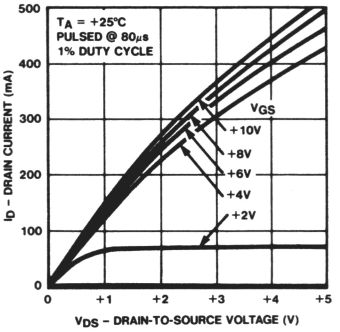
4. Pulsed @ 80μs; 1% duty cycle.

TYPICAL PERFORMANCE CHARACTERISTICS

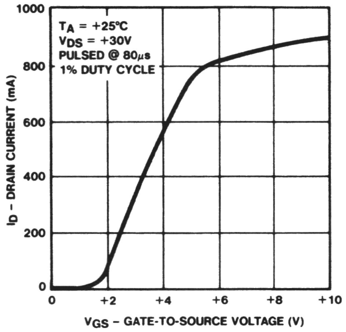
DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

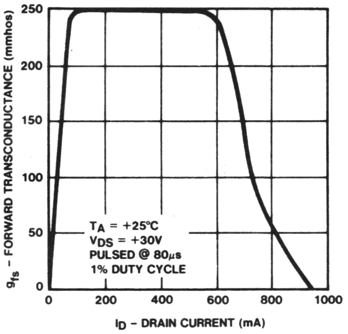


DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

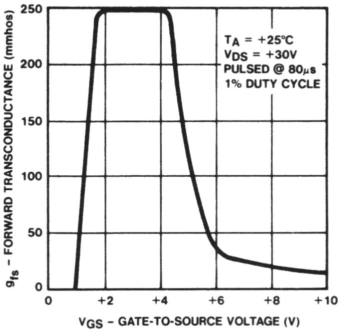


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

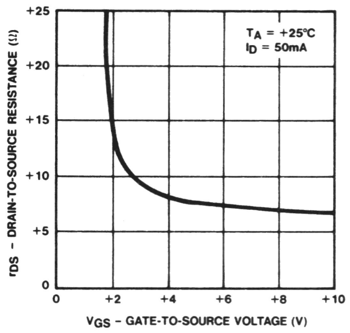
FORWARD TRANSCONDUCTANCE vs DRAIN CURRENT



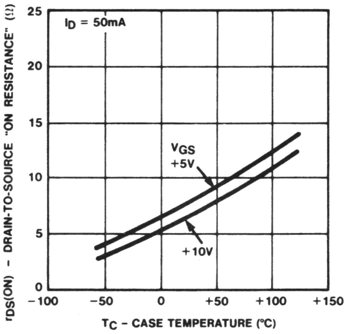
FORWARD TRANSCONDUCTANCE vs GATE-TO-SOURCE VOLTAGE



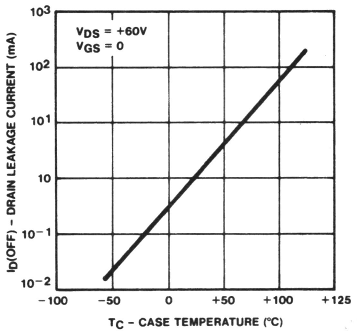
DRAIN-TO-SOURCE RESISTANCE vs GATE-TO-SOURCE VOLTAGE



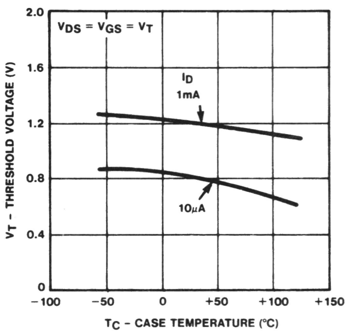
DRAIN-TO-SOURCE "ON RESISTANCE" vs CASE TEMPERATURE



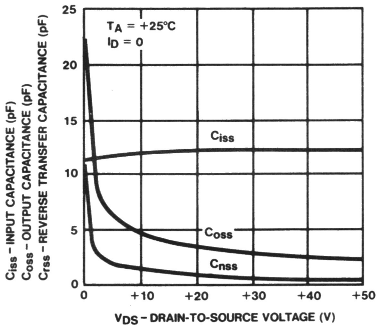
DRAIN LEAKAGE CURRENT vs CASE TEMPERATURE



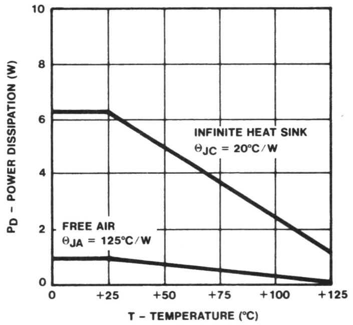
THRESHOLD VOLTAGE vs CASE TEMPERATURE



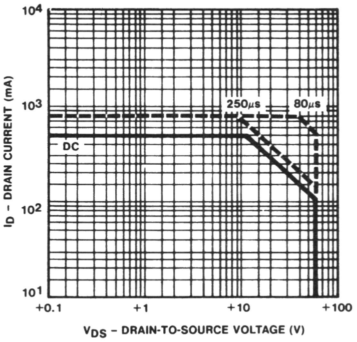
CAPACITANCES vs DRAIN-TO-SOURCE VOLTAGE



POWER DISSIPATION vs TEMPERATURE



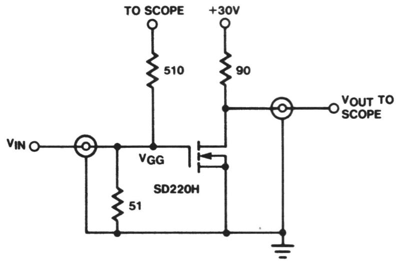
MAXIMUM SAFE OPERATING REGION



PRELIMINARY SPECIFICATION

SWITCHING SPEED

TEST CIRCUIT

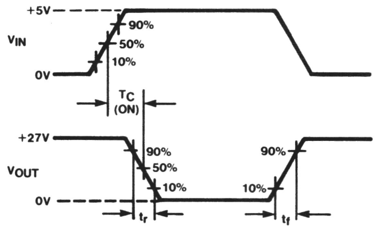

TO SCOPE
+30V
510
90
V_{OUT} TO SCOPE
V_{IN}
V_{GG}
SD220H
51

INPUT PULSE
t_d, t_r < 1ns
PULSE WIDTH = 10ns
REP RATE = 1MHz

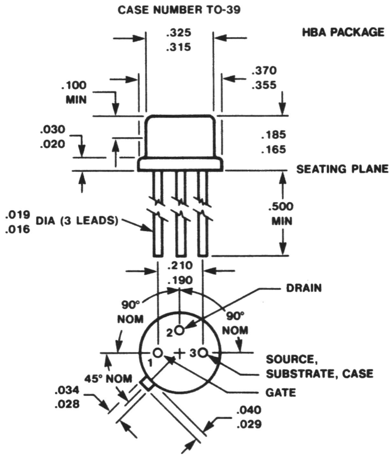
SAMPLING SCOPE
t_r < 360ps
R_{IN} = 1MΩ
C_{IN} = 2.0pF

NOTE
All resistors standard and are measured in ohms.

WAVEFORM


+5V
V_{IN}
0V
90%
50%
10%
T_C (ON)
+27V
V_{OUT}
0V
90%
50%
10%
90%
10%
t_r
t_f

PACKAGE OUTLINE


CASE NUMBER TO-39
HBA PACKAGE
.325
.315
.370
.355
.100 MIN
.030
.020
.185
.165
SEATING PLANE
.019
.016
DIA (3 LEADS)
.500 MIN
.210
.190
DRAIN
90° NOM
90° NOM
2
1
3
SOURCE, SUBSTRATE, CASE
45° NOM
GATE
.034
.028
.040
.029

D-MOS POWER FET SINGLE GATE N-CHANNEL ENHANCEMENT SD222DC

PRELIMINARY SPECIFICATION

DESCRIPTION

The Signetics SD222 is a POWER MOSFET of the N-channel enhancement mode type designed for switching applications requiring high voltage, high current, low "ON" resistance and high node-to-node isolation. Superior performance is achieved by utilizing the Signetics D-MOS process which provides high gain, low inter-electrode capacitances, low drain-to-source "ON" resistance and enhanced high frequency operation.

The device is hermetically sealed in a 4-lead TO-72 package.

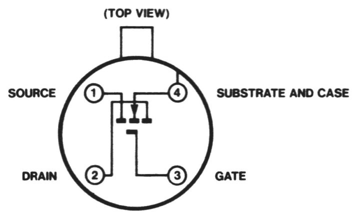
FEATURES

- **Low node capacitances**
- **Low feedthrough and feedback transients**
- **Excellent input and output isolations**
- **Extremely low input drive power**
- **High voltage: $V_{DS} > +60V$**

APPLICATIONS

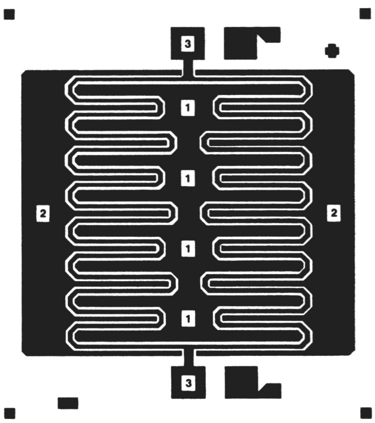
- **Power driver**
- **High speed switching**
- **Analog switching**
- **Multiplexers**
- **Sample and hold**

PIN CONFIGURATION



ORDER PART NO.
SD222DC

CHIP DIAGRAM



PAD NO.	PAD FUNCTION
1	DRAIN
2	SOURCE
3	GATE

ABSOLUTE MAXIMUM RATINGS[1] $T_A = +25°C$ unless otherwise specified.

PARAMETER		RATING	UNIT
V_{DS}	Drain-to-source	+60	V
V_{DB}	Drain-to-body	+60	V
V_{DG}	Drain-to-gate	+60 −20	V
V_{GS}	Gate-to-source	±20	V
V_{GB}	Gate-to-body	±20	V
V_{SB}	Source-to-body	+10	V
$I_D(ON)$	"ON" Drain current		
	Continuous	350	mA
	Pulsed (80μs, 1% duty cycle)	800	mA
P_D	Power dissipation		
	$T_A = +25°C^2$	300	mW
	$T_C = 25°C^3$	1.2	W
	Power derating factors		
	Free air	2.4	mW/°C
	Infinite heat sink	9.6	mW/°C
Θ_{JA}	Thermal resistance	417	°C/W
Θ_{JC}	Thermal resistance	104	°C/W
T_{op}	Operating temperature	−55 to +125	°C
T_{STG}	Storage temperature	−55 to +150	°C

NOTES

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Free air.
3. Infinite heat sink.

PRELIMINARY SPECIFICATION

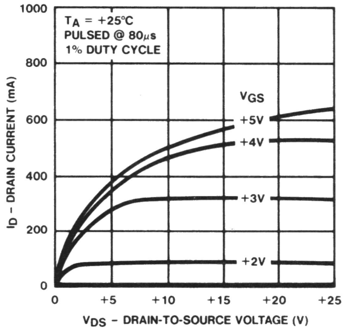
ELECTRICAL CHARACTERISTICS $T_A = +25°C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
BV_{DS}	Drain-source breakdown voltage	$V_{GS} = V_{SB} = 0, I_D = 1\mu A$	+60	+100		V
BV_{SB}	Source-Body breakdown voltage	$V_{GB} = 0$, Drain Open, $I_S = 1\mu A$	10			V
I_{GSS}	Gate leakage current	$V_{GSS} = \pm 20V$			1.0	nA
I_D (OFF)	Drain leakage current	$V_{DS} = +60V, V_{GS} = V_{SB} = 0$		0.1	1	μA
I_D (ON)	Drain "ON" current	$V_{DS} = +3.5V, V_{SB} = 0, V_{GS} = +10V$	275			mA
I_D (ON)	Drain "ON" current[4]	$V_{DS} = +6.5V, V_{SB} = 0, V_{GS} = +10V$	500	720		mA
V_T	Threshold voltage	$V_{DS} = V_{GS} = V_T, V_{SB} = 0, I_D = 10\mu A$	0.1	0.8	2.3	V
		$V_{DS} = V_{GS} = V_T, V_{SB} = 0, I_D = 1mA$	0.5	1.5	3.0	V
r_{DS} (ON)	Drain-source "ON" resistance[4]	$V_{GS} = +5V, V_{SB} = 0, I_D = 50mA$		7.5	10	Ω
		$V_{GS} = +10V, V_{SB} = 0, I_D = 50mA$		6.5	9	Ω
		$V_{GS} = +10V, V_{SB} = 0, I_D = 500mA$		9	13	Ω
g_{fs}	Forward transconductance[4]	$V_{DS} = +30V, V_{SB} = 0, I_D = 300mA$	220	250		mmhos
	Capacitances	$V_{DSS} = +30V, I_D = 0, f = 1MHz$				
C_{iss}	Input			12	15	pF
C_{oss}	Output			2.8	3.5	pF
C_{rss}	Reverse transfer			0.6	1.0	pF
t_d (ON)	Turn-ON delay time	See switching		1	2	ns
t_r	Rise time	Time test		1	3	ns
t_f	Fall time	Circuit		3	5	ns

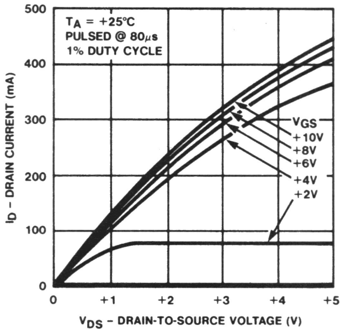
NOTE
[4] Pulsed @ 80μs, 1% duty cycle.

TYPICAL PERFORMANCE CHARACTERISTICS

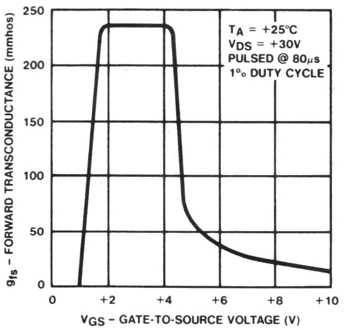
DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



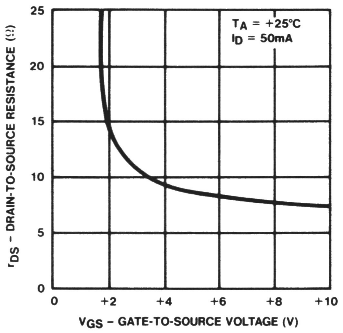
FORWARD TRANSCONDUCTANCE vs GATE-TO-SOURCE VOLTAGE



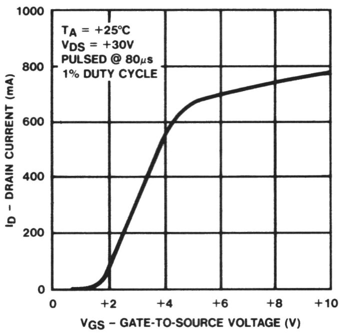
PRELIMINARY SPECIFICATION

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

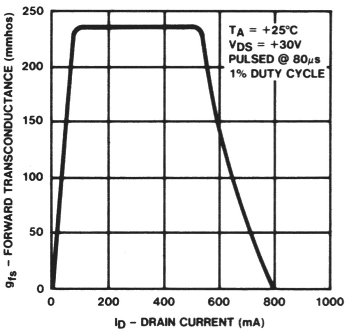
DRAIN TO SOURCE RESISTANCE vs GATE-TO-SOURCE VOLTAGE



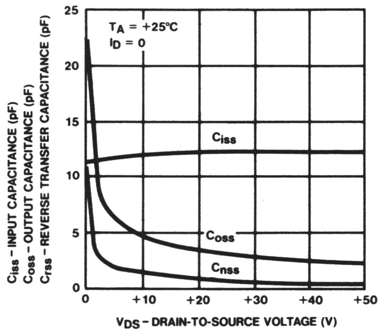
DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE



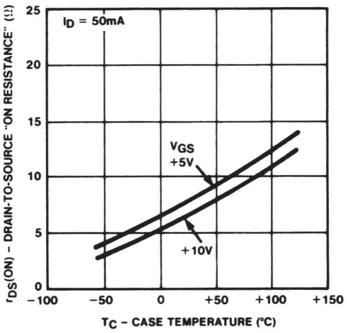
FORWARD TRANSCONDUCTANCE vs DRAIN CURRENT



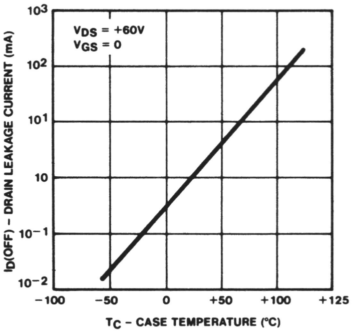
CAPACITANCES vs DRAIN-TO-SOURCE VOLTAGE



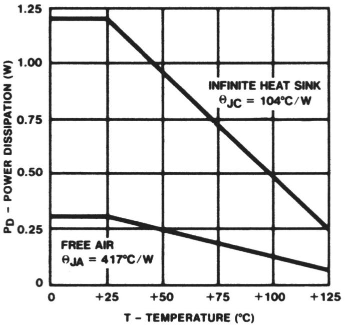
DRAIN-TO-SOURCE "ON" RESISTANCE vs CASE TEMPERATURE



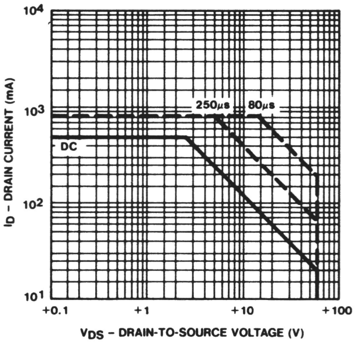
DRAIN LEAKAGE CURRENT vs CASE TEMPERATURE



POWER DISSIPATION vs TEMPERATURE



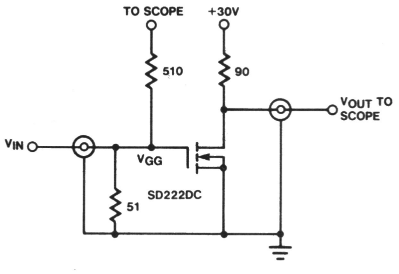
MAXIMUM SAFE OPERATING REGION



PRELIMINARY SPECIFICATION

SWITCHING SPEED

TEST CIRCUIT

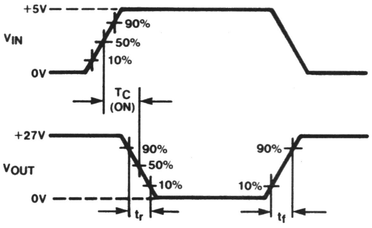

TO SCOPE
+30V
510
90
V_{OUT} TO SCOPE
V_{IN}
V_{GG}
SD222DC
51

INPUT PULSE
t_d, t_r < 1ns
PULSE WIDTH = 10ns
REP RATE = 1MHz

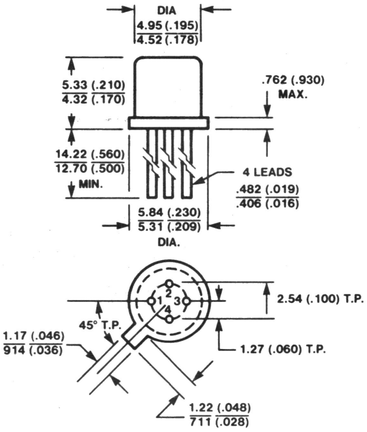
SAMPLING SCOPE
t_r < 360ps
R_{IN} = 1MΩ
C_{IN} = 2.0pF

NOTE
All resistors standard and are measured in ohms

WAVEFORM


+5V
V_{IN}
0V
90%
50%
10%
T_C (ON)
+27V
V_{OUT}
0V
90%
50%
10%
90%
10%
t_r
t_f

PACKAGE INFORMATION


DIA
4.95 (.195)
4.52 (.178)
5.33 (.210)
4.32 (.170)
.762 (.930)
MAX.
14.22 (.560)
12.70 (.500)
MIN.
4 LEADS
.482 (.019)
.406 (.016)
5.84 (.230)
5.31 (.209)
DIA.
1
2
3
4
2.54 (.100) T.P.
45° T.P.
1.17 (.046)
.914 (.036)
1.27 (.060) T.P.
1.22 (.048)
.711 (.028)

NOTES

1. Lead Material: Kover or equivalent—gold plated.
2. Body Material: Eyelet, Kover or equivalent—gold plated.
3. Lid Material: Nickel, weld seal.
4. All dimensions shown in parenthesis are English (inches).

D-MOS POWER FET SINGLE GATE N-CHANNEL ENHANCEMENT SD226H

PRELIMINARY SPECIFICATION SD226H

DESCRIPTION

The Signetics SD226 is a POWER MOSFET of the N-channel enhancement mode type designed for switching and amplifier applications requiring high current, high speed, and exceptionally linear transfer characteristics. Superior performance is achieved by utilizing the Signetics D-MOS process which provides high gain, low drain-to-source "ON" resistance, low inter-electrode capacitances, and enhanced high frequency operation.

The device is hermetically sealed in a TO-39 package. The source, substrate, and case are internally connected.

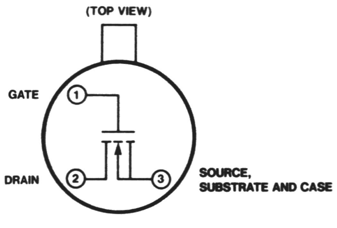
FEATURES

- **Low "ON" resistance: 1Ω @ 1A**
- **High current: 2A dc, 3A pulsed**
- **Withstands high VSWR**
- **No secondary breakdown**
- **Low drive power**
- **Low inter-electrode capacitances**
- **Linear transfer characteristics**

APPLICATIONS

- **Power amplification**
- **Power driver**
- **High speed switching**
- **Motor controls**
- **Switching power supplies**
- **Analog switching**

PIN CONFIGURATION



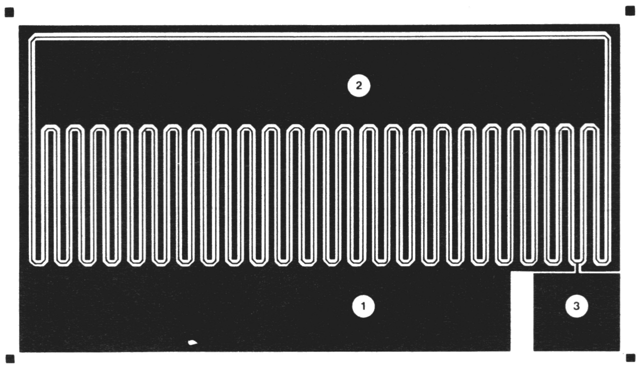
ORDER PART NO.
SD226H

ABSOLUTE MAXIMUM RATINGS[1] $T_A = +25°C$ unless otherwise specified

PARAMETER		RATING	UNIT
V_{DS}	Drain-to-source	+30	V
V_{GS}	Gate-to-source	±20	V
V_{GD}	Gate-to-drain	+20 −30	V
$I_D(ON)$	Continuous drain current	2	A
$I_D(ON)$	Pulsed drain current	3	A
P_D	Power dissipation		
	$T_A = 25°C^2$	1	W
	$T_C = 25°C^3$	6.25	W
	Power derating factors		
	Free Air	8	mW/°C
	Infinite Heat Sink	50	mW/°C
Θ_{JA}	Thermal Resistance[2]	125	°C/W
Θ_{JC}	Thermal Resistance[3]	20	°C/W
T_{op}	Operating Temperature	−55 to +125	°C
T_{STG}	Storage Temperature	−55 to +150	°C

NOTES
1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Free air.
3. Infinite heat sink.

CHIP DIAGRAM



PAD NO.	PAD FUNCTION
1	SOURCE
2	DRAIN
3	GATE

PRELIMINARY SPECIFICATION

ELECTRICAL CHARACTERISTICS $T_A = +25°C$

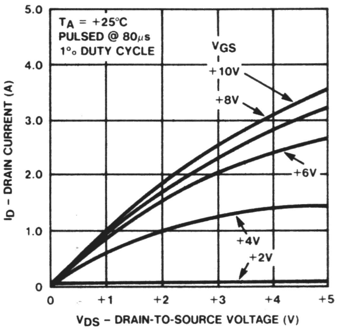
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
BV_{DS}	Drain-source breakdown voltage	$V_{GS} = V_{SB} = 0$, $I_D = 1\mu A$	+30	+35		V
I_{GSS}	Gate leakage current	$V_{GSS} = \pm 20V$			1.0	nA
$I_D(OFF)$	Drain leakage current	$V_{DS} = +30V$, $V_{GS} = 0$		0.1	1	μA
$I_D(ON)$ $I_D(ON)$	Drain "ON" current Drain "ON" current[4]	$V_{DS} = +2.2V$, $V_{GS} = +10V$ $V_{DS} = +3.3V$, $V_{GS} = +10V$	1.4 2.2	2.0 3.0		A A
V_T	Threshold voltage	$V_{DS} = V_{GS} = V_T$, $I_D = 10\mu A$ $V_{DS} = V_{GS} = V_T$, $I_D = 1mA$	0.1 0.5	1.0 1.5	2.3 3.0	V V
$r_{DS}(ON)$	Drain-source "ON" resistance[4]	$V_{GS} = +5V$, $I_D = 50mA$ $V_{GS} = +10V$, $I_D = 50mA$ $V_{GS} = +10V$, $I_D = 3A$		1.4 1.1 1.1	2.0 1.5 1.5	Ω Ω Ω
g_{fs}	Forward transconductance[4]	$V_{DS} = +15V$, $I_D = 2A$	700	750		mmhos
 C_{iss} C_{oss} C_{rss}	Capacitances Input Output Reverse transfer	$V_{DS} = +15V$, $I_D = 0$, f = 1MHz		 35 20 5	 45 25 6	 pF pF pF
$t_d(ON)$ t_r t_f	Turn-ON delay time Rise time Fall time	See Switching Time Test Circuit		1 1 3	2 3 5	ns ns ns

NOTE

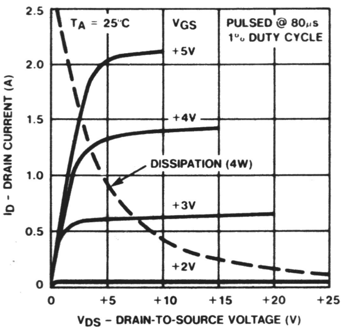
[4] Pulsed @ 80μs, 1% duty cycle.

TYPICAL PERFORMANCE CHARACTERISTICS

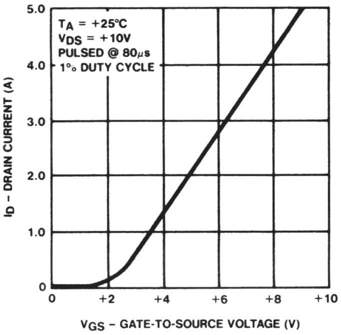
DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

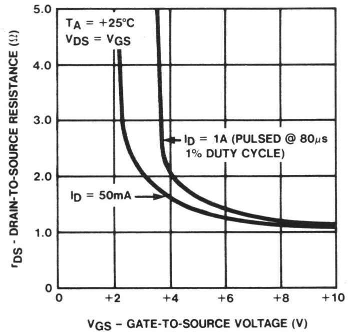


DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

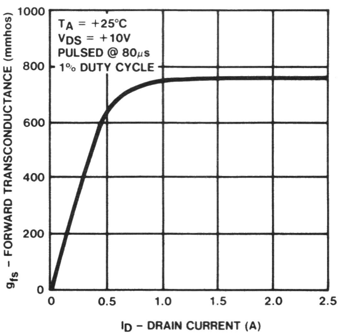


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

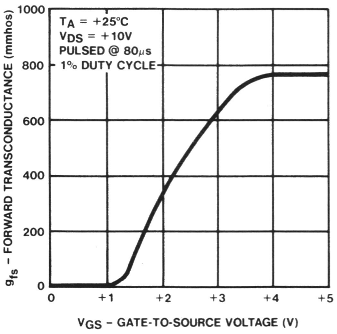
DRAIN-TO-SOURCE RESISTANCE vs GATE-TO-SOURCE VOLTAGE



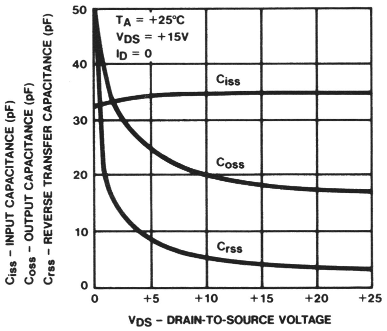
FORWARD TRANSCONDUCTANCE vs DRAIN CURRENT



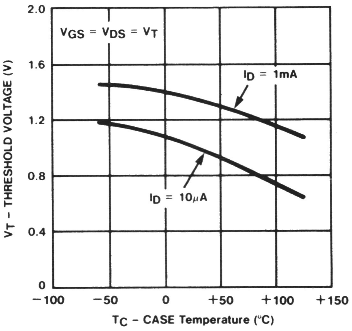
FORWARD TRANSCONDUCTANCE vs GATE-TO-SOURCE VOLTAGE



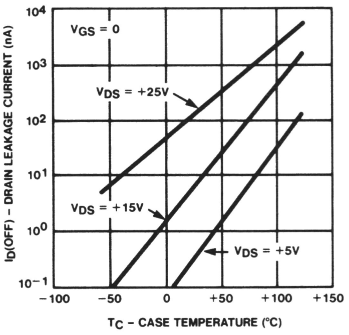
CAPACITANCES vs DRAIN-TO-SOURCE VOLTAGE



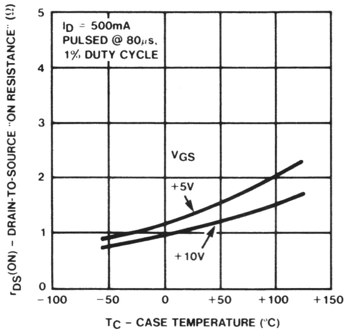
THRESHOLD VOLTAGE vs CASE TEMPERATURE



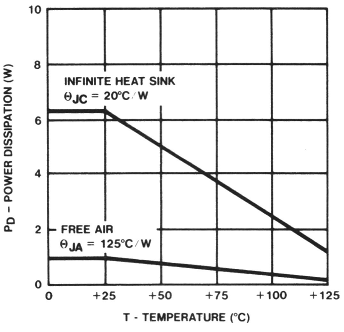
DRAIN LEAKAGE CURRENT vs CASE TEMPERATURE



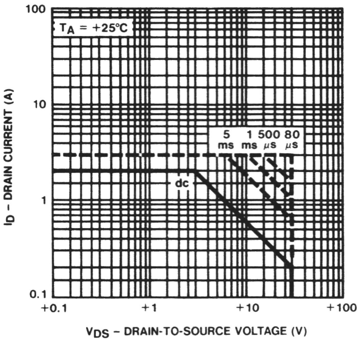
DRAIN-TO-SOURCE "ON RESISTANCE" vs CASE TEMPERATURE



POWER DISSIPATION vs TEMPERATURE



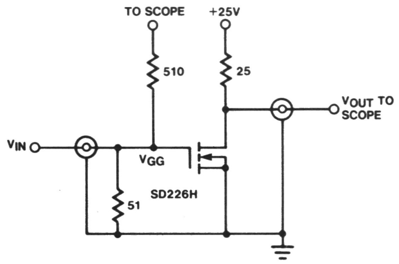
MAXIMUM SAFE OPERATING REGION



PRELIMINARY SPECIFICATION

SWITCHING SPEED

TEST CIRCUIT

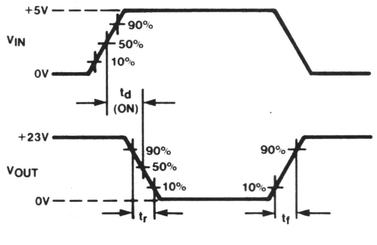

TO SCOPE
+25V
510
25
V_{OUT} TO SCOPE
V_{IN}
V_{GG}
SD226H
51

INPUT PULSE
t_d, t_r < 1ns
PULSE WIDTH = 10ns
REP RATE = 1MHz

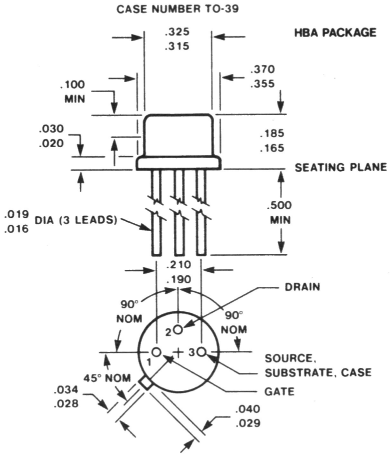
SAMPLING SCOPE
t_r < 360ps
R_{IN} = 1MΩ
C_{IN} = 2.0pF

NOTE
All resistors standard and are measured in ohms.

WAVEFORM


+5V
V_{IN}
0V
90%
50%
10%
t_d (ON)
+23V
V_{OUT}
0V
90%
50%
10%
t_r
90%
10%
t_f

PACKAGE OUTLINE


CASE NUMBER TO-39
HBA PACKAGE
.325
.315
.370
.355
.100
MIN
.030
.020
.185
.165
SEATING PLANE
.019
.016
DIA (3 LEADS)
.500
MIN
.210
.190
DRAIN
90°
NOM
90°
NOM
2
1
3
SOURCE, SUBSTRATE, CASE
GATE
45° NOM
.034
.028
.040
.029

D-MOS FET DUAL GATE N-CHANNEL ENHANCEMENT SD303

SD303-DC

DESCRIPTION

The Signetics D-MOS SD303 is a silicon, dual-insulated-gate, field effect transistor of the N-channel enhancement mode type. It is fabricated by the Signetics double-diffused process which gives superior high frequency performance. Zener diodes are connected between the two gates and the substrate. These diodes bypass any voltage transients which lie outside the range of -0.3V to +25.0V. Thus, the gates are protected against damage in all normal handling and operating situations.

The device characteristics make it ideally suited for a variety of high frequency amplifier and mixer applications. The presence of two gates plus the incorporation of the drift region in the structure has made the feedback capacity (Crss) less than 0.02pF. A wide AGC capability plus a significant reduction in cross-modulation distortion is now available because of the inherent linearity of these devices. The SD303 is hermetically sealed in a modified 4-lead TO-72 package.

GENERAL FEATURES

- **Lower cross-modulation and wider dynamic range than bipolar or single gate FETs**
- **Reverse AGC capability**
- **Linear mixing capability**
- **Diode protected gates**
- **High forward transconductance: 10mmhos**
- **ION-implanted**
- **Positive bias only**

FEATURES

PARAMETER	SD303	UNIT
High gain through UHF range	14	dB at 1GHz
High gain through VHF range		dB at 500MHz
Low noise through UHF range	5.5	dB at 1GHz
Low noise through VHF range		dB at 500MHz
Low input capacitance	3.0	pF
Low feedback capacitance	0.02	pF
Low outut capacitance	0.6	pF

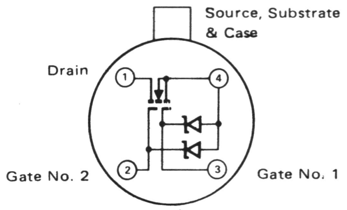
ABSOLUTE MAXIMUM RATINGS

$T_A = 25°C$ unless otherwise specified.

	PARAMETER	RATING	UNIT
V_{DS}	Drain-to-source		
	SD303	+20	V
V_{G1B}	DC gate no. 1-to-substrate voltage	-0.3, +10	V
V_{G2B}	DC gate no. 2-to-substrate voltage	-0.3, +15	V
I_D	Drain current	50	mA
T_A	Ambient temperature range		
	Storage	-65 to +175	°C
	Operating	-55 to +125	°C
P_T	Transistor dissipation		
	At +25°C case temperature (Derate linearly to +125°C case temperature at the rate of 8.0mW/°C.)	1.2	W
	At +25°C free-air temperature (Derate linearly to +125°C free-air temperature at the rate of 2.0mW/°C.)	300	mW

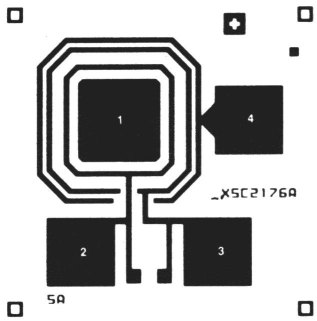
PIN CONFIGURATIONS (Top View)

DC, DE PACKAGE



ORDER PART NO.
SD303DC

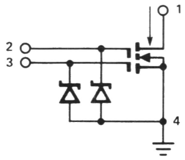
CHIP DIAGRAM



PAD NO.	PAD FUNCTION
1	DRAIN
2	GATE NO. 2
3	GATE NO. 1
4	SOURCE

Die Size 20X20

DUAL GATE CASCODE BIAS SCHEME



$+V_{DS} = 0 \rightarrow +20$ volts
$+V_{G1S} = 0 \rightarrow +4$ volts
$+V_{G2S} = 0 \rightarrow +10$ volts
$+I_{DS} = 0 \rightarrow +20mA$

SD/303-DC

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SD303			UNIT
			Min	Typ	Max	
BV_{DS}	Drain-to-source Breakdown voltage	$V_{G1S} = V_{G2S} = 0V$, $I_D = 5\mu A$	20	25		V
I_{G1SS}	Gate 1 Leakage current	$V_{G1S} = +5V$, $V_{G2S} = V_{DS} = 0V$		0.001	0.1	μA
I_{G2SS}	Gate 2 Leakage current	$V_{G2S} = +10V$ $V_{G1S} = V_{DS} = 0V$		0.001	0.1	μA
$I_D(OFF)$	Drain-to-source Leakage current	$V_{DS} = +15V$, $V_{G1S} = V_{G2S} = 0V$		0.001	0.1	μA
I_{DSS}	Zero bias Drain current	$V_{DS} = +15V$ $V_{G1S} = V_{G2S} = 0V$		0.001	0.1	μA
V_{T1}	Gate 1 Threshold voltage	$V_{DS} = V_{G1S} = V_{T1}$ $V_{G2S} = +10V$, $I_D = 1\mu A$	0.1	0.5	1.5	V
V_{T2}	Gate 2 Threshold voltage	$V_{DS} = V_{G2S} = V_{T2}$, $V_{G1S} = +4V$, $I_D = 1\mu A$	0.1	0.5	1.5	V
r_{DS} (ON)	Drain-to-source On resistance	$V_{G1S} = +5V$, $V_{G2S} = +10V$, $I_D = 1.0mA$		65	80	Ω

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

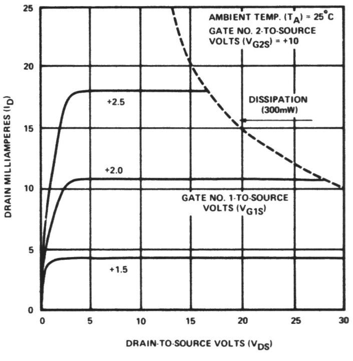
PARAMETER		TEST CONDITIONS	SD303			UNIT
			Min	Typ	Max	
C_{iss}	Small signal short circuit Capacitances Input	f = 1MHz, Gate 2 AC grounded $V_{DS} = +15V$, $V_{G1S} \cong 3.5V$, $V_{G2S} = +10V$, $I_D = 18mA$				pF
		$V_{DS} = +15V$, $V_{G1S} \cong +2.5V$, $V_{G2S} = +10V$, $I_D = 18mA$		3.0	3.5	pF
C_{oss}	Output	$V_{DS} = +15V$, $V_{G1S} = 0V$, $V_{G2S} = +10V$		0.6		pF
C_{rss}	Reverse transfer	$V_{DS} = +15V$, $V_{G1S} = 0V$, $V_{G2S} = +10V$		0.02		pF
gfs	Forward transconductance	$V_{DS} = +15V$, $V_{G1S} \cong +3.5V$, $V_{G2S} = +10V$, $I_D = 18mA$, f = 1kHz				mmhos
		$V_{DS} = +15V$, $V_{G1S} \cong +2.5V$, $V_{G2S} = +10V$, $I_D = 18mA$	13.0	15.0		mmhos
Gps	Power gain	$V_{DS} = +15V$, $V_{G1S} \cong +3.5V$, $V_{G2S} = +10V$, $I_D = 18mA$ f = 1GHz				dB
		f = 500MHz				dB
		f = 200MHz				dB
		$V_{DS} = +15V$, $V_{G1S} \cong +2.5V$, $V_{G2S} = +10V$, $I_D = 18mA$, f = 1GHz	10.0	14.0*		dB
E_{int}	Noise figure	$V_{DS} = +15V$, $V_{G1S} \cong +3.5V$, $V_{G2S} = +10V$, $I_D = 18mA$ f = 1GHz				dB
		f = 500MHz				dB
		f = 200MHz				
		$V_{DS} = +15V$, $V_{G1S} \cong +2.5V$, $V_{G2S} = +10V$, $I_D = 18mA$, f = 1GHz		5.5*	7.0	dB
NF	Interfering signal level at gate for 1% cross-modulation distortion. Peak voltage referenced to 300Ω system.	$V_{DS} = +15V$, $V_{G2S} = +10V$, $I_D = 18mA$, Desired signal f = 500MHz, Undersired signal f = 501MHz				mV
		$V_{DS} = +15V$, $V_{G2S} = +10V$, $I_D = 18mA$, Wanted Signal f = 1GHz, Interfering signal f = 0.995GHz		150		mV
AGC (V_{G2S})	Range of automatic Gain control	$V_{DS} = +15V$, $V_{G1S} \cong +3.5V$, f = 500MHz				dB
		$V_{DS} = +15V$, $V_{G1S} \cong +2.5V$, f = 500MHz		40		dB

*NOTE

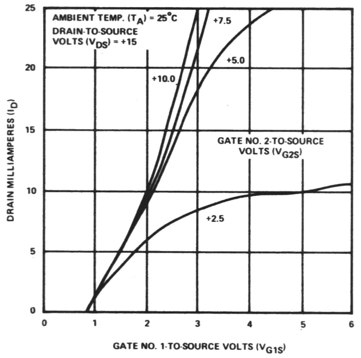
Measured in amplifier test fixture.

SD303 TYPICAL PERFORMANCE CHARACTERISTICS

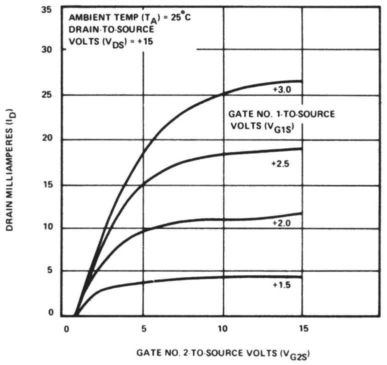
DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



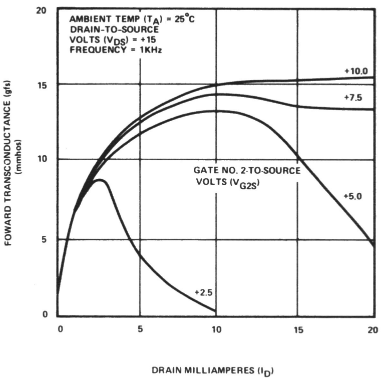
DRAIN CURRENT vs GATE NO. 1-TO-SOURCE VOLTAGE



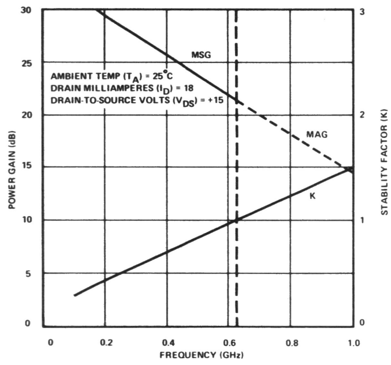
DRAIN CURRENT vs GATE NO. 2-TO-SOURCE VOLTAGE



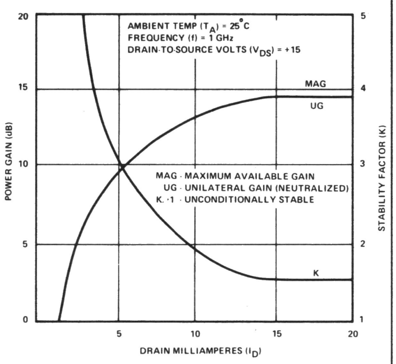
1kHz FORWARD TRANSCONDUCTANCE vs DRAIN CURRENT



POWER GAIN vs FREQUENCY



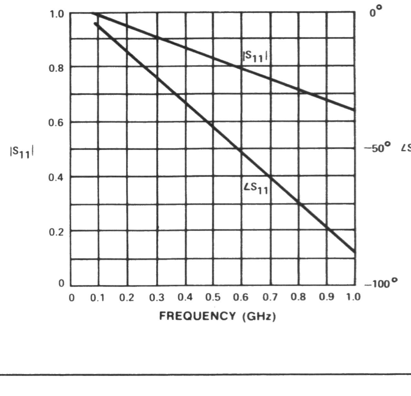
POWER GAIN vs DRAIN CURRENT

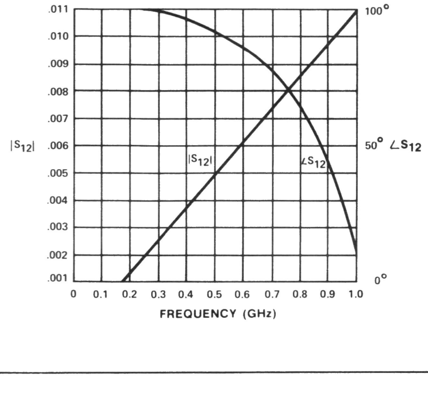


SD303 "S" PARAMETERS

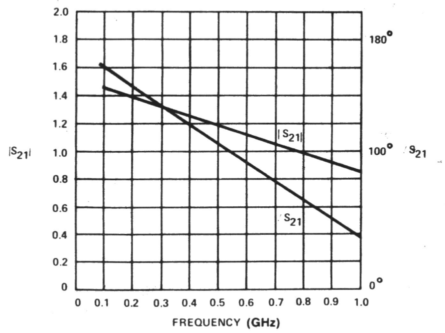
AMBIENT TEMP. (T_A) = +25°C
DRAIN MILLIAMPERES (I_D) = 18

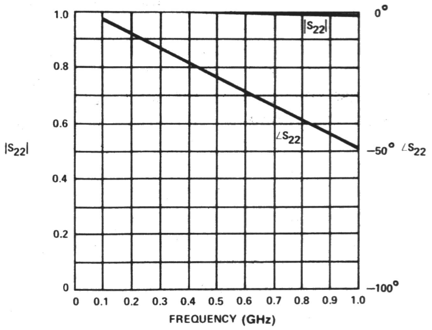
DRAIN-TO-SOURCE VOLTS (V_{DS}) = +15
GATE NO. 1-TO-SOURCE VOLTS (V_{G1S}) ≃ +2.5
GATE NO. 2-TO-SOURCE VOLTS (V_{G2S}) = +10



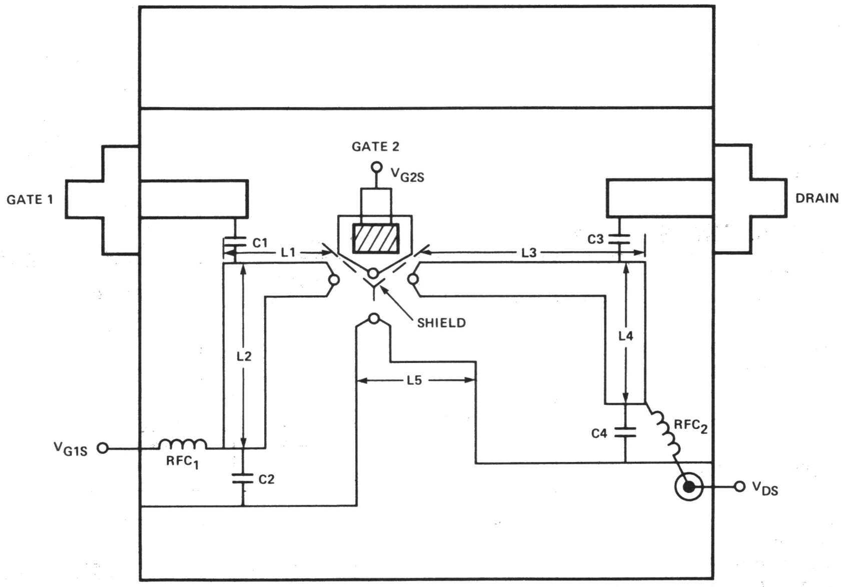


SD303 TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)





1GHz TEST FIXTURE


GATE 2
VG2S
GATE 1
DRAIN
C1
L1
L3
C3
SHIELD
L2
L4
L5
C4
RFC2
VG1S
RFC1
C2
VDS

Dielectric is 1/16" Teflon-Fiberglass (3M-K6098-11).
All microstrip width = 0.175 inch.

L_1 = 0.42 inch
L_2 = 1.68 inches
L_3 = 0.64 inch
L_4 = 1.52 inches
L_5 = 0.30 inch

C_1 = 0.8-10pF Johanson 5201
C_2 = C_4 1.20pF Johanson 5501
C_3 = 0.4-6.0pF Johanson 4642
RFC_1 = 0.22μH
RFC_2 = 18μH

NOTE Shield and all passive components on ground plane side of amplifier.
1000pF bypasses are:
Drain: Cory FT4-01-2

Gate 2: American technical
Ceramics ATC100B
(Chip capacitor)

Launchers are OSM248-2

D-MOS FET-DUAL GATE N-CHANNEL ENHANCEMENT SD305/SD306

SD305/306 - DE

DESCRIPTION

The Signetics D-MOS SD305 and 306 are silicon, dual-insulated gate, field-effect transistors of the N-channel enhancement mode type. Zener diodes are connected between the two gates and the substrate. These diodes bypass any voltage transients which lie outside the range of -0.3V to +20.0V. Thus, the gates are protected against damage in all normal handling and operating situations. The characteristics of the devices make them ideally suited for a variety of VHF amplifier and mixer applications. The presence of two gates plus the incorporation of the drift region in the structure has made the feedback capacity (C_{G1D}) typically less than 0.03pF. A wide AGC capability plus significant reduction in cross modulation distortion is now available because of the inherent linearity of the devices. The SD305 and SD306 are hermetically sealed in a 4-lead TO-72 package.

GENERAL FEATURES

- **Positive bias only**
- **Low gate voltages**
- **Enhancement mode operation**
- **Wide AGC range: -50dB at 200MHz**
- **Zener diode gate protection**
- **ION implanted for greater reliability**

FEATURES—SD305 (VHF TV and FM Mixer)

- **High conversion gain: 17dB at 200MHz with $V_{G1S} = V_{G2S}$ for biasing simplicity**
- **Excellent isolation from Gate No. 1 (RF) to Gate No. 2 (LO): -20dB at 200MHz**
- **Low input capacitance: 4.0pF**
- **Low feedback capacitance: 0.03pF**
- **Excellent cross modulation performance and low noise operation**
- **High transconductance: 27mmhos**

FEATURES—SD306 (VHF TV and FM RF Amplifier)

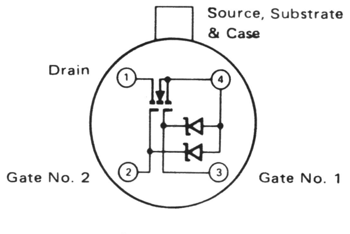
- **High power gain without neutralization: 20dB at 200MHz**
- **Low noise figure: 1.5dB at 200MHz**
- **Low input and output capacitance: 3.3pF and 1.0pF constant with AGC**
- **Low feedback capacitance: 0.03pF**
- **Superior cross modulation performance**
- **High transconductance: 15mmhos**

ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$ unless otherwise specified.

PARAMETER		RATING	UNIT
V_{DS}	Drain-to-source voltage	+20	V
V_{G1B}	Gate no. 1—to-substrate voltage	-0.3 to +20	Vdc
V_{G2B}	Gate no. 1—to-substrate voltage	-0.3 to +20	Vdc
I_D	Drain current		
	SD305	150	mA
	SD306	50	mA
T_A	Ambient temperature range		
	Storage	-65 to +175	°C
	Operating	-55 to +125	°C
P_T	Transistor dissipation		
	At 25°C case temperature (Derate linearly to 125°C case temperature at the rate of 8.0mW/°C)	1.2	W
	At 25°C free-air temperature (Derate linearly to 125°C free-air temperature at the rate of 2.0mW/°C)	300	mW

PIN CONFIGURATION

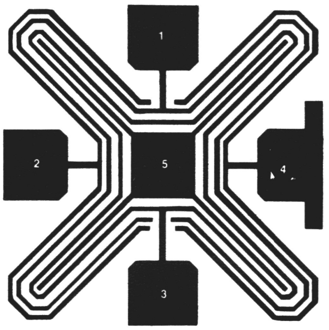
DE PACKAGE
(Top View)



ORDER PART NO.
SD305DE and SD306DE

CHIP DIAGRAMS

SD305

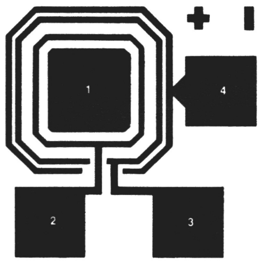


PAD NO.	PAD FUNCTION
1	GATE NO. 1
2	SOURCE
3	GATE NO. 2
4	SOURCE
5	DRAIN

Die Size 24 X 24

NOTE
Pads 2 and 4 must both be utilized for source connection

SD306



PAD NO.	PAD FUNCTION
1	DRAIN
2	GATE NO. 2
3	GATE NO. 1
4	SOURCE

Die Size 20 X 20

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SD305			SD306			UNIT
			Min	Typ	Max	Min	Typ	Max	
OFF Characteristics									
BV_{DS}	Drain-to-source Breakdown voltage	$V_{G1S} = V_{G2S} = 0V$, $I_D = 5\mu A$	20	30		20	25		V
I_D (OFF)	Drain-to-source Leakage current	$V_{DS} = +15V$ $V_{G1S} = V_{G2S} = 0V$		0.001	1.0		0.001	1.0	μA
I_{DSS}	Zero bias drain current	$V_{DS} = +15V$ $V_{G1S} = V_{G2S} = 0V$		0.001	1.0		0.001	1.0	μA
I_{G1SS}	Gate no. 1 leakage current	$V_{G1S} = +5V$ $V_{G2S} = V_{DS} = 0V$		0.001	0.1		0.001	0.1	μA
I_{G2SS}	Gate no. 2 leakage current	$V_{G2S} = +10V$ $V_{G1S} = V_{DS} = 0V$		0.001	0.1		0.001	0.1	μA
ON Characteristics									
V_{T1}	Gate 1 threshold voltage	$V_{DS} = V_{G1S} = V_{T1}$, $V_{G2S} = +10V$, $I_D = 1\mu A$	0.1	1.0	2.0	0.1	0.5	1.5	V
V_{T2}	Gate 2 threshold voltage	$V_{DS} = V_{G2S} = V_{T2}$, $V_{G1S} = +5V$, $I_D = 1\mu A$	0.1	1.0	2.0	0.1	0.5	1.5	V
r_{DS}(ON)	Drain-to-source on resistance	$V_{G1S} = +5V$, $V_{G2S} = +10V$, $I_D = 1.0mA$		30	60		65	100	Ω

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SD305			SD306			UNIT
			Min	Typ	Max	Min	Typ	Max	
Small signal characteristics									
gfs	Forward transconductance	$V_{DS} = +15V$, $V_{G2S} = +10V$, f = 1kHz							
		$I_D = 50mA$	24	27					mmhos
		$I_D = 18mA$				13	15		mmhos
gfs (CONV)	Conversion transconductance	$V_{DS} = +15V$, $V_{G1S} = V_{G2S}$, $I_D = 8mA$, f = 1kHz, $E_{LO}(RMS) = 750mV$		10					mmhos
Capacitances		f = 1MHz, gate 2 AC grounded							
C_{G1S}	Input	$V_{DS} = +15V$, $V_{G2S} = +10V$							
		$I_D = 50mA$		4.0	5.0				pF
		$I_D = 18mA$					3.3	3.6	pF
		$V_{DS} = +15V$, $V_{G1S} = V_{G2S}$, $I_D = 8mA$		4.0	5.0				pF
C_{DS}	Output	$V_{DS} = +15V$, $V_{G1S} = 0V$, $V_{G2S} = +10V$		1.3	1.7		1.0	1.3	pF
C_{G1D}	Reverse transfer	$V_{DS} = +15V$ $V_{G1S} = 0V$, $V_{G2S} = +10V$		0.03			0.03		pF
	Input admittance	f = 200MHz, $V_{DS} = +15V$	$V_{G1S} = V_{G2S}$, $I_D = 8mA$			$V_{G2S} = +10V$, $I_D = 18mA$			
	$Re(Y_{11})$			1.05			1.11		mmhos
	$Im(Y_{11})$			6.66			4.76		mmhos
	Output admittance	f = 200MHz, $V_{DS} = +15V$							
	$Re(Y_{22})$			0.73			1.05		mmhos
	$Im(Y_{22})$			2.09			1.54		mmhos
	Forward transmittance	f = 200MHz, $V_{DS} = +15V$							
	$Re(Y_{21})$			4.69			13.23		mmhos
	$Im(Y_{21})$			-3.01			-5.62		mmhos
	Reverse transmittance	f = 200MHz, $V_{DS} = +15V$							
	$Re(Y_{12})$			0.04			0.01		mmhos
	$Im(Y_{12})$			−0.03			−0.04		mmhos
G_{ps}	Power gain[2]	$V_{DS} = +15V$, $V_{G2S} = +10V$ $I_D = 18mA$, f = 200MHz				17	20		dB

AC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$ unless otherwise specified.

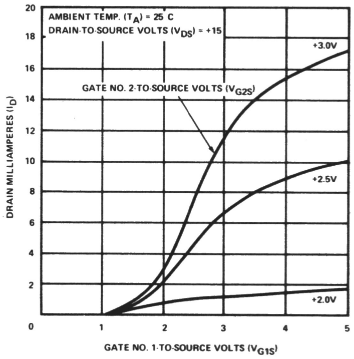
PARAMETER		TEST CONDITIONS	SD305			SD306			UNIT
			Min	Typ	Max	Min	Typ	Max	
G_{ps}(CONV)	Conversion power gain[1]	$V_{DS} = +15V$, $V_{G1S} = V_{G2S}$, $I_D = 8mA$, $f_{rf} = 200MHz$, $f_{LO} = 245MHz$	14	17					dB
NF	Noise figure	$V_{DS} = +15V$, $V_{G2S} = +10V$, $I_D = 18mA$, $f = 200MHz$					1.5	2.5	dB
AGC_{VG2S}	Range of automatic gain control	$V_{DS} = +15V$, $V_{G1S} \cong +2.5V$, $V_{G2S} = +10V \rightarrow 0V$, $f = 200MHz$					50		dB
E_{INT}	Interfering signal level at gate 1 for 1% cross modulation distortion, peak voltage referenced to 50Ω system[3]	$V_{DS} = 15V$, $V_{G2S} = +8V$, $I_D = 15mA$ Wanted signal f = 200MHz interfering signal f = 196MHz					480		mV

NOTES

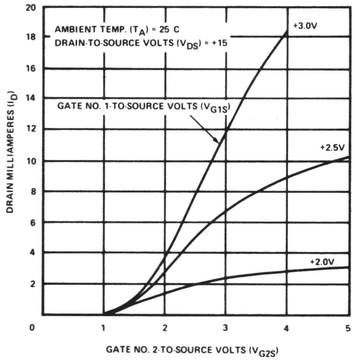
1. Measured in mixer test fixture.
2. Measured in amplifier test fixture.
3. Measured as shown in block diagram.

SD305 TYPICAL PERFORMANCE CHARACTERISTICS

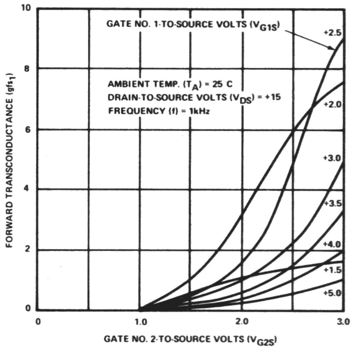
DRAIN CURRENT vs GATE NO. 1-TO-SOURCE VOLTAGE



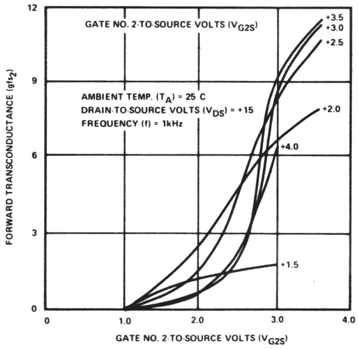
DRAIN CURRENT vs GATE NO. 2-TO-SOURCE VOLTAGE



GATE NO. 1 FORWARD TRANSCONDUCTANCE vs GATE NO. 2-TO-SOURCE VOLTAGE



GATE NO. 2 FORWARD TRANSCONDUCTANCE vs GATE NO. 1-TO-SOURCE VOLTAGE

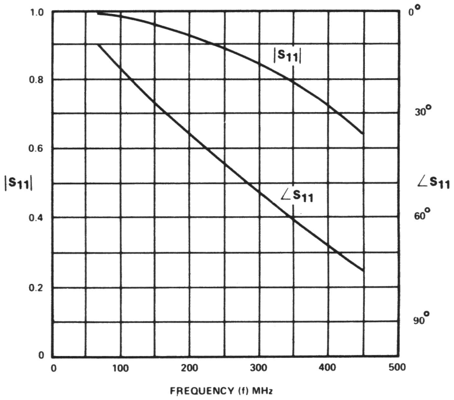


SD305 TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

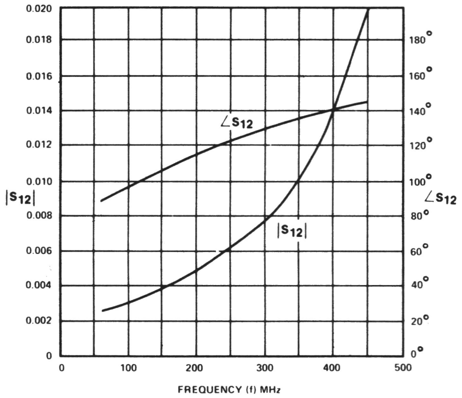
"S" PARAMETERS

AMBIENT TEMP. (T_A) = +25°C
DRAIN-TO-SOURCE VOLTS (V_{DS}) = +15
DRAIN MILLIAMPERES (I_D) = 8
GATE NO. 1-TO-SOURCE VOLTS (V_{G1S}) =
GATE NO. 2-TO-SOURCE VOLTS (V_{G2S})

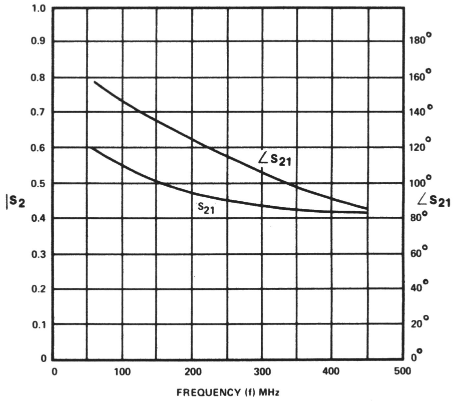
S_{11}



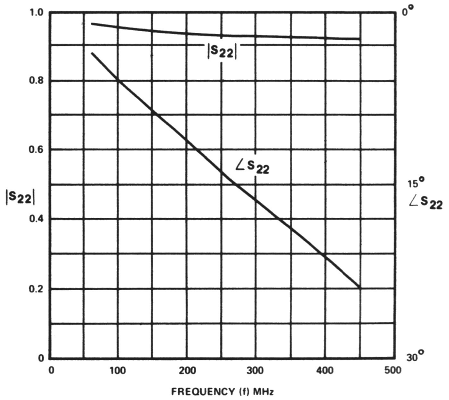
S_{12}



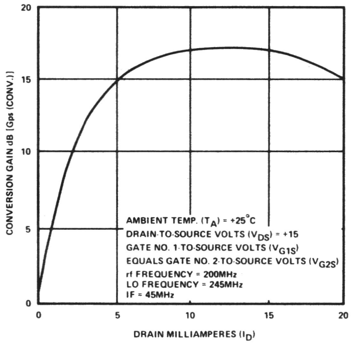
S_{21}



S_{22}

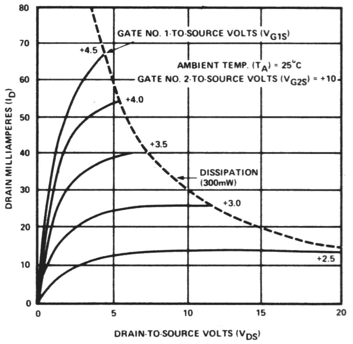


CONVERSION GAIN vs DRAIN CURRENT



AMBIENT TEMP. (T_A) = +25°C
DRAIN-TO-SOURCE VOLTS (V_{DS}) = +15
GATE NO. 1-TO-SOURCE VOLTS (V_{G1S})
EQUALS GATE NO. 2-TO-SOURCE VOLTS (V_{G2S})
rf FREQUENCY = 200MHz
LO FREQUENCY = 245MHz
IF = 45MHz

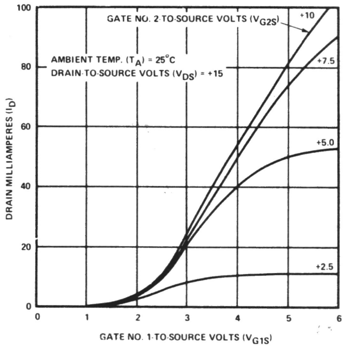
DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



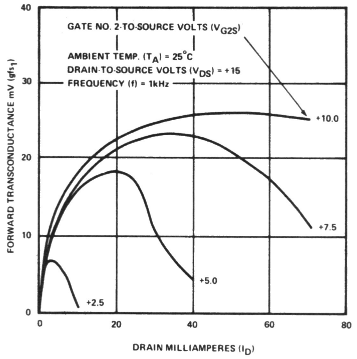
AMBIENT TEMP. (T_A) = 25°C
GATE NO. 2-TO-SOURCE VOLTS (V_{G2S}) = +10

SD305 TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

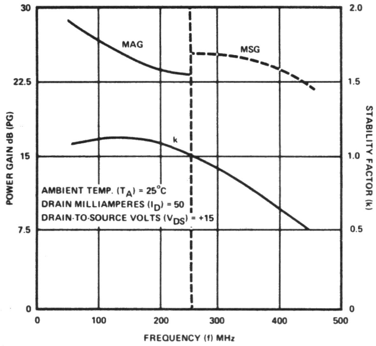
DRAIN CURRENT vs GATE NO. 1-TO-SOURCE VOLTAGE



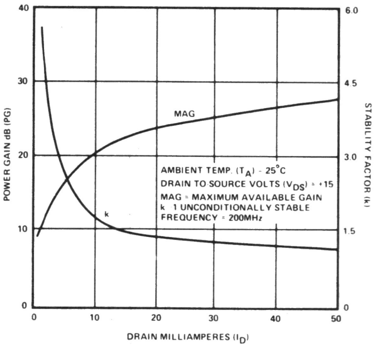
GATE NO. 1 FORWARD TRANSCONDUCTANCE vs DRAIN CURRENT



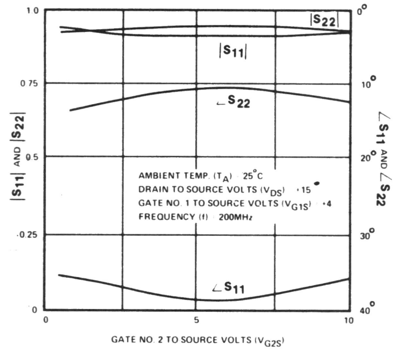
POWER GAIN vs FREQUENCY



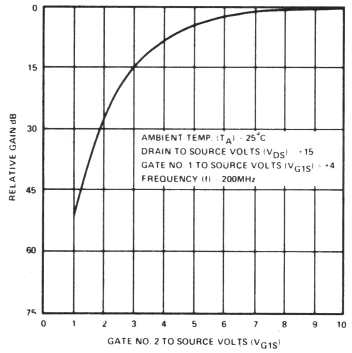
POWER GAIN vs DRAIN CURRENT



AUTOMATIC GAIN CONTROL vs S_{11} AND S_{22}



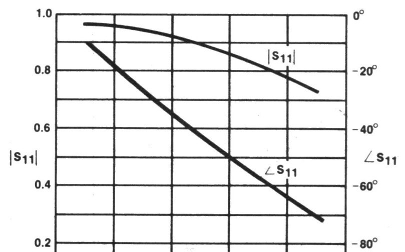
AUTOMATIC GAIN CONTROL RANGE



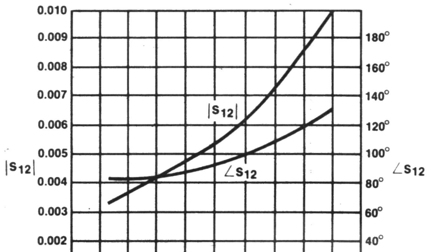
"S" PARAMETERS

AMBIENT TEMP. (T_A) = +25° C
DRAIN-TO-SOURCE VOLTS (V_{DS}) = +15
DRAIN MILLIAMPERES (I_D) = 50
GATE NO. 1-TO-SOURCE VOLTS (V_{G1S}) ≃ +3.5
GATE NO. 2-TO-SOURCE VOLTS (V_{G2S}) = +10

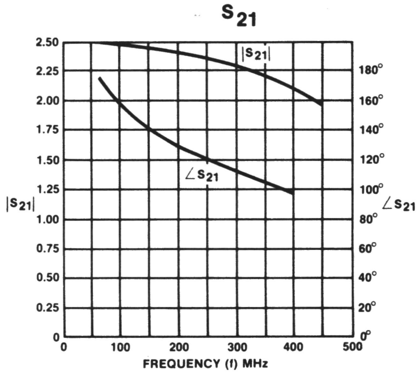
S_{11}

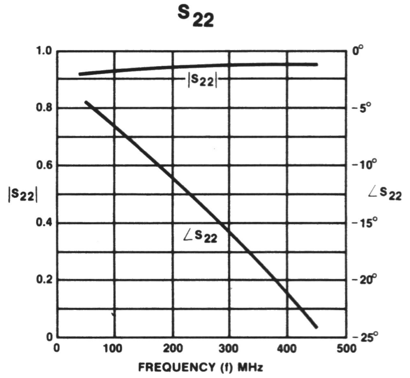


S_{12}



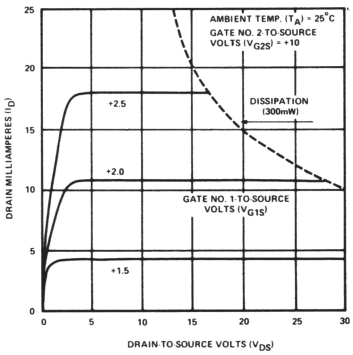
SD305 TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)



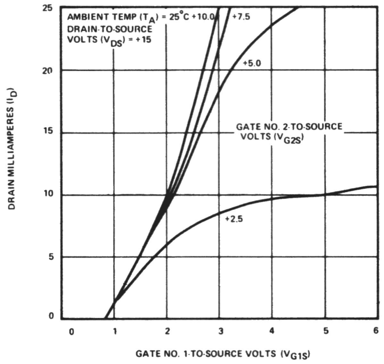


SD306 TYPICAL PERFORMANCE CHARACTERISTICS

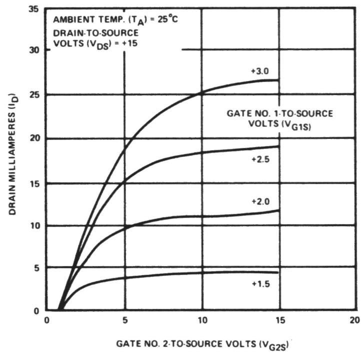
DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



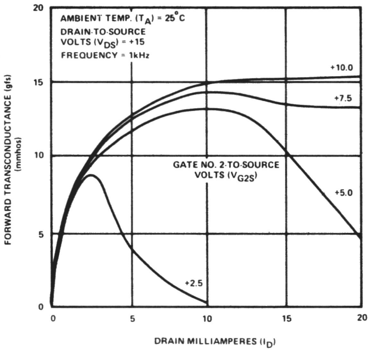
DRAIN CURRENT vs GATE NO. 1-TO-SOURCE VOLTAGE



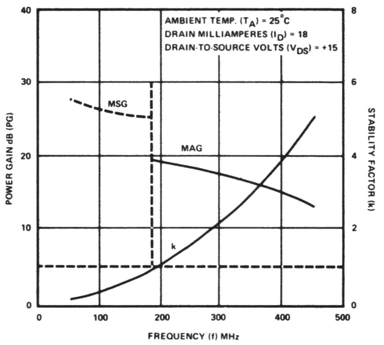
DRAIN CURRENT vs GATE NO. 2-TO-SOURCE VOLTAGE



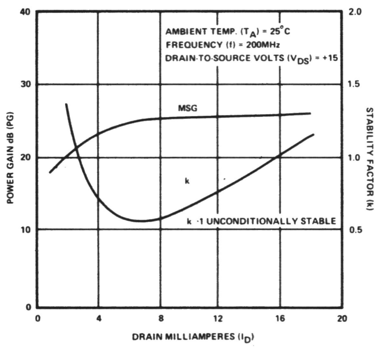
1kHz FORWARD TRANSCONDUCTANCE vs DRAIN CURRENT



POWER GAIN vs FREQUENCY

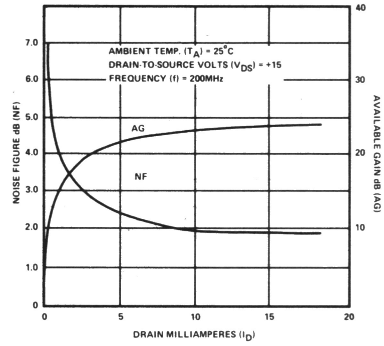


POWER GAIN vs DRAIN CURRENT

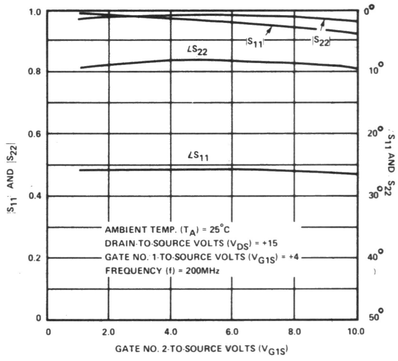


SD306 TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

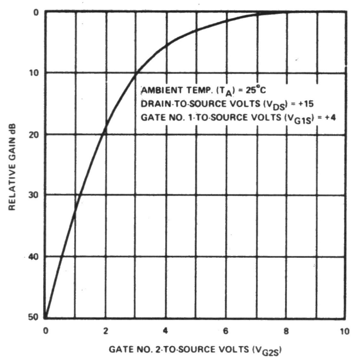
NOISE FIGURE AND AVAILABLE GAIN vs DRAIN CURRENT



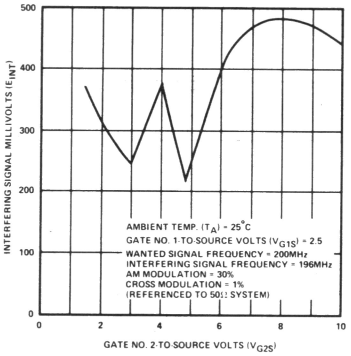
S_{11} AND S_{22} vs AUTOMATIC GAIN CONTROL



AUTOMATIC GAIN CONTROL RANGE AT 200MHz



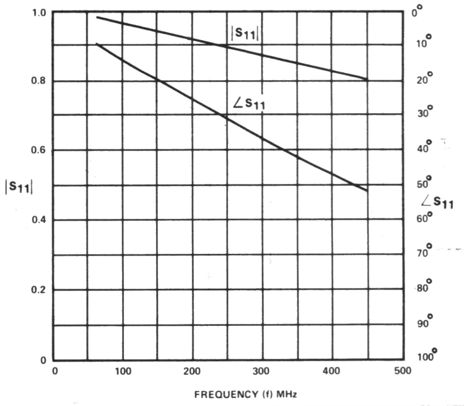
INTERFERING SIGNAL LEVEL vs GATE NO. 2-TO-SOURCE VOLTS



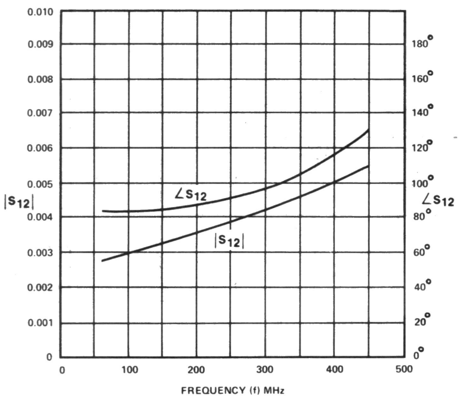
"S" PARAMETERS

AMBIENT TEMP. (T_A) = +25° C
DRAIN-TO-SOURCE VOLTS (V_{DS}) = 15
DRAIN MILLIAMPERES (I_D) = 8
GATE NO. 1-TO-SOURCE VOLTS (V_{G1S}) ≃ +2.5
GATE NO. 2-TO-SOURCE VOLTS (V_{G2S}) = +10

S_{11}

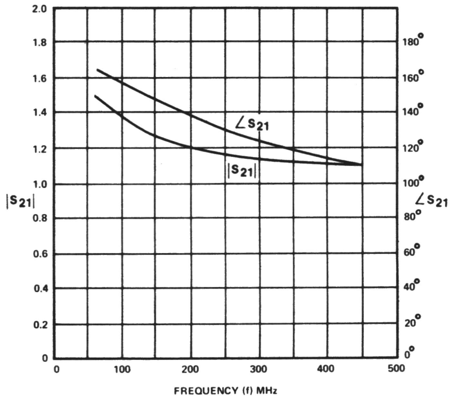


S_{12}

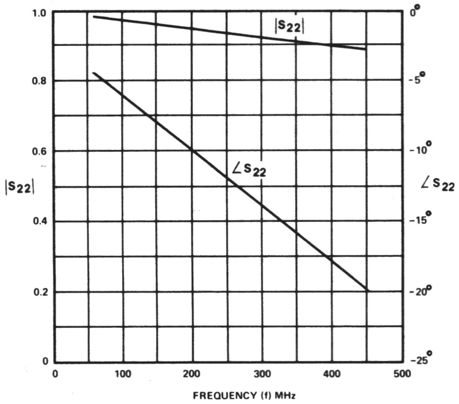


SD306 TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

S_{21}

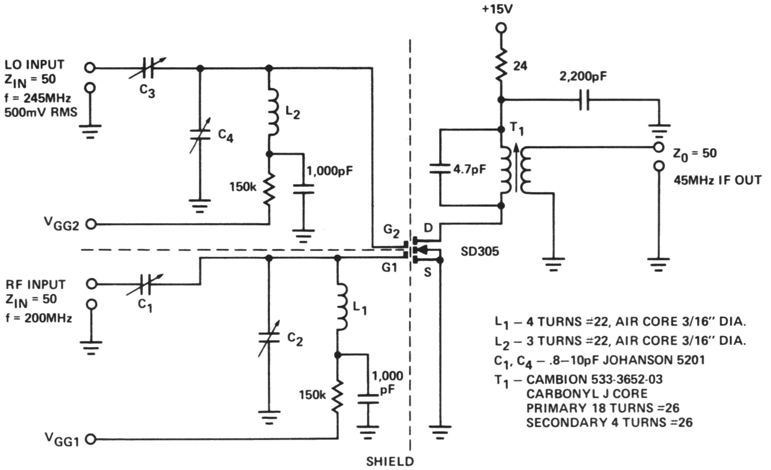


S_{22}



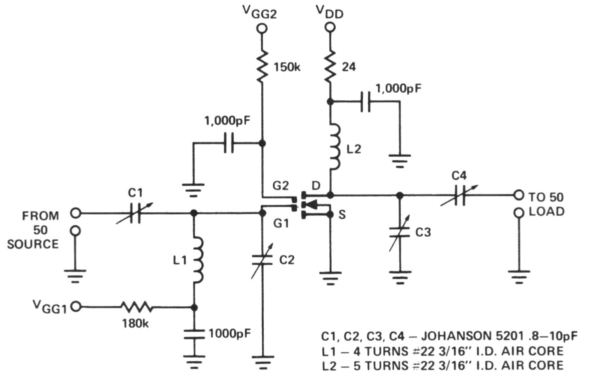
TEST CIRCUITS

SD305
200MHz/45MHz MIXER


+15V
LO INPUT
ZIN = 50
f = 245MHz
500mV RMS
C3
C4
L2
150k
1,000pF
VGG2
24
2,200pF
T1
4.7pF
Z0 = 50
45MHz IF OUT
G2
D
G1
S
SD305
RF INPUT
ZIN = 50
f = 200MHz
C1
C2
L1
150k
1,000 pF
VGG1
SHIELD

L_1 – 4 TURNS #22, AIR CORE 3/16" DIA.
L_2 – 3 TURNS #22, AIR CORE 3/16" DIA.
C_1, C_4 – .8–10pF JOHANSON 5201
T_1 – CAMBION 533-3652-03
CARBONYL J CORE
PRIMARY 18 TURNS #26
SECONDARY 4 TURNS #26

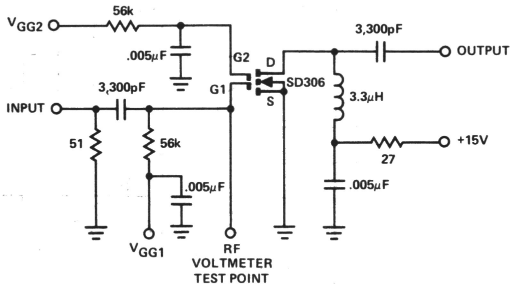
SD306
POWER GAIN, NOISE FIGURE 200MHz TEST AMPLIFIER;


VGG2
VDD
150k
24
1,000pF
1,000pF
L2
G2
D
S
G1
C1
C4
FROM
50
SOURCE
TO 50
LOAD
L1
C2
C3
VGG1
180k
1000pF

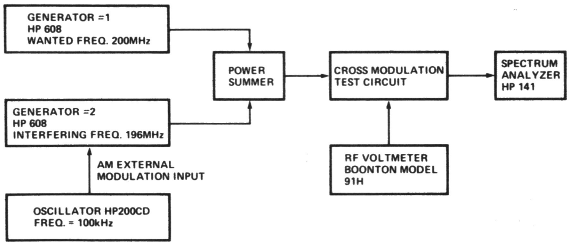
C1, C2, C3, C4 – JOHANSON 5201 .8–10pF
L1 – 4 TURNS #22 3/16" I.D. AIR CORE
L2 – 5 TURNS #22 3/16" I.D. AIR CORE

TEST CIRCUITS (Cont'd)

SD306 CROSS MODULATION


VGG2
56k
.005µF
G2
D
3,300pF
OUTPUT
3,300pF
G1
SD306
S
3.3µH
INPUT
51
56k
27
+15V
.005µF
.005µF
VGG1
RF VOLTMETER TEST POINT

BLOCK DIAGRAM OF CROSS MODULATION TEST


GENERATOR =1
HP 608
WANTED FREQ. 200MHz
POWER SUMMER
CROSS MODULATION TEST CIRCUIT
SPECTRUM ANALYZER HP 141
GENERATOR =2
HP 608
INTERFERING FREQ. 196MHz
AM EXTERNAL MODULATION INPUT
RF VOLTMETER BOONTON MODEL 91H
OSCILLATOR HP200CD
FREQ. = 100kHz

SD306 TEST PROCEDURE FOR CROSS MODULATION DISTORTION MEASUREMENTS

1. Modulation on Generator #2 is set at 100kHz, 30% AM modulation (sidebands down 15.6dB) with an output signal frequency equal to 196MHz.
2. Generator #2 is set at approximately −15dbm, 200MHz.
3. While observing the test circuit output spectrum, adjust the signal level of the interfering frequency so that the sidebands on the desired frequency are 46dB down from the carrier. This corresponds to 1% cross modulation.
4. Turn off Generator #1 and turn off the modulation on Generator #2.
5. Using the RF voltmeter, measure the amplitude of the interfering signal at the test point.

SD6000 - N

DESCRIPTION

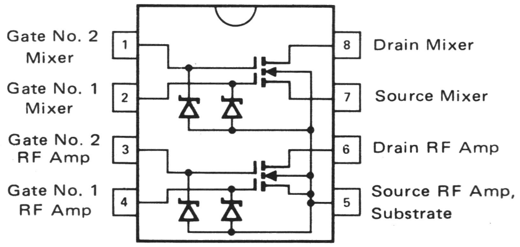
The Signetics D-MOS SD6000 is an integrated circuit fabricated by the double-diffused process and employing silicon N-channel enhancement mode MOSFETs with dual gates. Zener diodes are connected between all gates and the substrate. These diodes bypass any voltage transients which lie outside the range of -0.3V to +20.0V. Thus, the gates are protected against damage in all normal handling and operating situations. The use of the dual gate structure plus the incorporation of the drift region has made the feedback capacity (C_{G1D}) typically less than 0.03pF. The attributes of the IC make it ideally suited for FM/VHF RF amplifier and mixer applications. The IC is specifically characterized for incorporation into varactor or conventional FM tuners but the performance guaranteed makes it useful in a wide variety of VHF tuner applications. The power gain at 100MHz is 30dB minimum with a guaranteed noise figure of 3.0dB. A wide AGC capability plus significant reduction in cross modulation is now available because of the inherent linearity of the D-MOS FETs. The SD6000 is packaged in the Signetics 8-pin plastic N package.

GENERAL FEATURES

- **Positive bias only**
- **Low gate voltages**
- **Enhancement mode operation**
- **Zener diode gate protection**
- **Ion implanted for greater reliability**

PIN CONFIGURATION

N PACKAGE
(Top View)



ORDER PART NO.
SD6000N

FEATURES (RF AMP Section)

- **High power gain without neutralization: 25dB at 100MHz**
- **Low noise figure: 2.5dB at 100MHz**
- **Low input and output capacitances constant with AGC: 3.0pF and 1.0pF**
- **Low feedback capacitance: 0.025pF**
- **Superior cross modulation performance**
- **High transconductance: 15mmhos**
- **Wide AGC range: 50dB at 100MHz**

FEATURES (Mixer Section)

- **High conversion gain: 17dB at 100MHz with $V_{G1S} = V_{G2S}$ for biasing simplicity**
- **Excellent isolation from gate no. 1 (RF) to gate no. 2 (LO)**
- **Low input capacitance: 4.0pF**
- **Low feedback capacitance: 0.03pF**
- **Excellent cross modulation performance and low noise operation**
- **High conversion transconductance at low drain currents: 10mmhos**

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise specified.

PARAMETER		RATING	UNIT
V_{DS}	Drain-to-source voltage	+20	V
V_{G1B}	Gate no. 1-to-substrate voltage	-0.3 to +20	Vdc
V_{G2B}	Gate no. 2-to-substrate voltage	-0.3 to +20	Vdc
	Drain current	50	mA
T_A	Ambient temperature range		
	Storage	-65 to +150	°C
	Operating	-55 to +85	°C
P_T	Power dissipation		
	At 25°C case temperature	625	mW
	Temperature above 25°C	Derate at 5.0	mW/°C

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	RFAMP			MIXER			UNIT
			Min	Typ	Max	Min	Typ	Max	
OFF CHARACTERISTICS									
BV_{DS}	Drain-to-source breakdown voltage	$V_{G1S} = V_{G2S} = 0V$, $I_D = 5\mu A$	20	30		20	30		V
$I_{D(OFF)}$	Drain-to-source leakage current	$V_{DS} = +15V$, $V_{G1S} = V_{G2S} = 0V$		0.001	1.0		0.001	1.0	μA
I_{DSS}	Zero bias drain current	$V_{DS} = +15V$, $V_{G1S} = V_{G2S} = 0V$		0.001	1.0		0.001	1.0	μA
I_{G1SS}	Gate no. 1 leakage current	$V_{G1S} = +5V$, $V_{G2S} = V_{DS} = 0V$		0.001	0.1		0.001	0.1	μA
I_{G2SS}	Gate no. 2 leakage current	$V_{G2SS} = +10V$, $V_{G1S} = V_{DS} = 0V$		0.001	0.1		0.001	0.1	μA
ON CHARACTERISTICS									
V_{T1}	Gate 1 threshold voltage	$V_{DS} = V_{G1S} = V_{T1}$, $V_{G2S} = +10V$, $I_D = 1\mu A$	0.1	0.5	1.5	0.1	1.0	2.0	V
V_{T2}	Gate 2 threshold voltage	$V_{DS} = V_{G2S} = V_{T2}$, $V_{G1S} = +5V$, $I_D = 1\mu A$	0.1	0.5	1.5	0.1	1.0	2.0	V
$r_{DS(ON)}$	Drain-to-source on resistance	$V_{G1S} = +5V$, $V_{G2S} = +10V$, $I_D = 1.0mA$		65	100		30	60	Ω

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.[1,2]

PARAMETER		TEST CONDITIONS	SD6000			UNIT
			Min	Typ	Max	
SMALL SIGNAL CHARACTERISTICS-RF Amp						
gfs	Forward transconductance	$V_{DS} = +15V$, $V_{G2S} = +10V$, $I_D = 18mA$, f = 1kHz	12	15		mmhos
	Capacitances	f = 1MHz, gate no. 2 AC grounded				
C_{G1S}	Input	$V_{DS} = +15V$, $V_{G2S} = +10V$, $I_D = 18mA$		3.0	3.5	pF
C_{DS}	Output	$V_{DS} = +15V$, $V_{G1S} = 0V$, $V_{G2S} = 10V$		1.0	1.3	pF
C_{G1D}	Reverse transfer	$V_{DS} = +15V$, $V_{G1S} = 0V$, $V_{G2S} = 10V$		0.025		pF
	Input admittance	f = 100MHz, $V_{DS} = +15V$, $V_{G2S} = +10V$, $I_D = 18mA$				
	Re (Y_{11})			0.21		mmhos
	Im (Y_{11})			2.26		mmhos
	Output admittance					
	Re (Y_{22})			0.20		mmhos
	Im(Y_{22})			0.68		mmhos
	Forward transmittance					
	Re (Y_{21})			12.85		mmhos
	Im (Y_{21})			-1.50		mmhos
	Reverse transmittance					
	Re (Y_{12})			0.01		mmhos
	Im (Y_{12})			-0.03		mmhos
Gps	Power gain[1]	$V_{DS} = +15V$, $V_{G2S} = +10V$, $I_D = 18mA$, f = 100MHz	20	25		dB
NF	Noise figure[1]	$V_{DS} = +15V$, $V_{G2S} = +10V$, $I_D = 18mA$, f = 100MHz		2.5	3.0	dB
AGC(V_{G2S})	Range of automatic gain control	$V_{DS} = +15V$, $V_{G1S} \cong +2.5V$, f = 100MHz		50		dB

AC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$ unless otherwise specified.[1,2]

SMALL SIGNAL CHARACTERISTICS—MIXER $g_{fs(CONV)}$ conversion transconductance	$V_{DS} = +15V$, $V_{G1S} = V_{G2S}$ $I_D = 8mA$, $f = 1kHz$ $E_{LO}(RMS) = 750mV$		10		mmhos
Capacitances	f = 1MHz, gate no. 2 AC grounded				
C_{G1S} Input	$V_{DS} = +15V$, $V_{G1S} = V_{G2S}$, $I_D = 8mA$		4.0	4.75	pF
C_{DS} Output	$V_{DS} = +15V$, $V_{G1S} = V_{G2S} = 0V$		1.1	1.5	pF
C_{G1D} Reverse transfer	$V_{DS} = +15V$, $V_{G1S} = V_{G2S} = 0V$		0.030		pF
Input admittance					
Re (Y_{11})			0.21		mmhos
Im (Y_{11})			2.28		mmhos
Output admittance					
Re (Y_{22})			0.41		mmhos
Im (Y_{22})	$f = 100MHz$, $V_{DS} = +15V$		1.04		mmhos
Forward transmittance	$V_{G1S} = V_{G2S}$, $I_D = 8mA$				
Re (Y_{21})			3.18		mmhos
Im (Y_{21})			-0.83		mmhos
Reverse transmittance					
Re (Y_{12})			0.03		mmhos
Im (Y_{12})			-0.01		mmhos
$G_{ps(CONV)}$ Conversion power gain[2]	$V_{DS} = +15V$, $V_{G1S} = V_{G2S}$, $I_D = 8mA$, $f_{RF} = 100MHz$, $f_{LO} = 89.3MHz$	14	19		dB

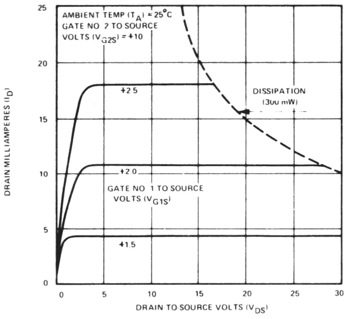
NOTES

1. Measured in amplifier test fixture.
2. Measured in MIXER test fixture.

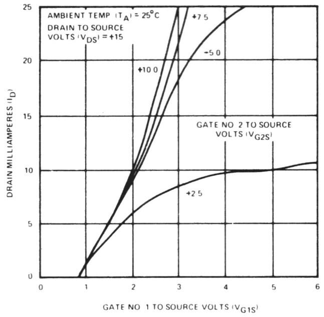
TYPICAL PERFORMANCE CHARACTERISTICS

RF AMP SECTION

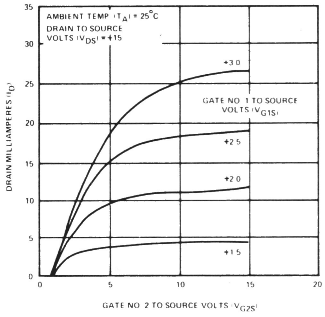
DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



DRAIN CURRENT vs GATE NO. 1-TO-SOURCE VOLTAGE



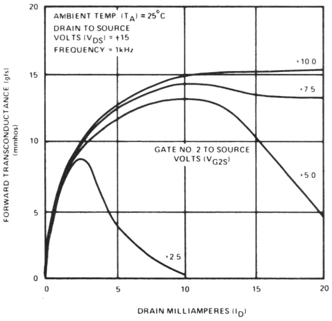
DRAIN CURRENT vs GATE NO. 2-TO-SOURCE VOLTAGE



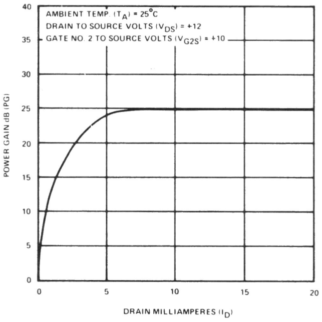
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

RF AMP SECTION

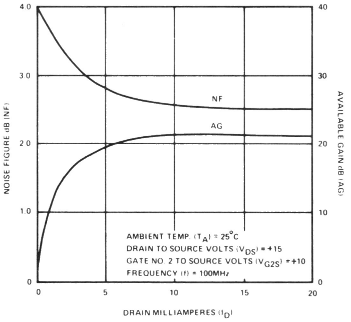
1kHz FORWARD TRANSCONDUCTANCE vs DRAIN CURRENT



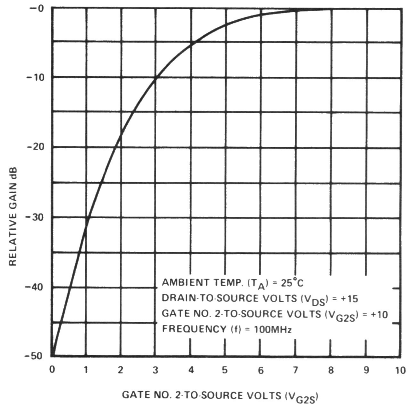
POWER GAIN vs DRAIN CURRENT



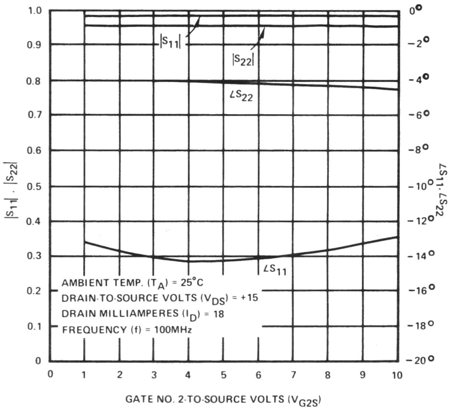
NOISE FIGURE AND AVAILABLE GAIN vs DRAIN CURRENT



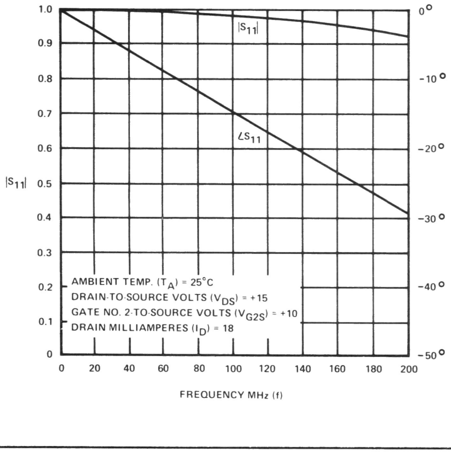
AUTOMATIC GAIN CONTROL RANGE



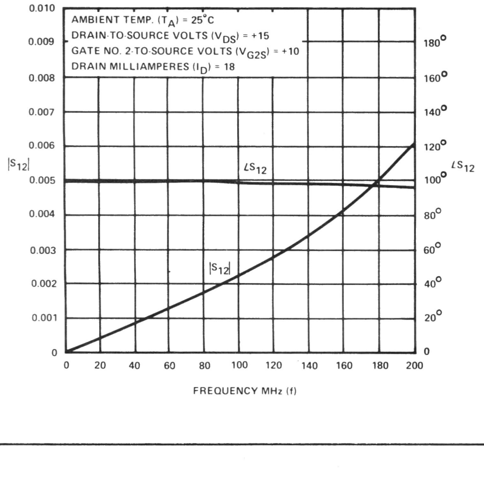
S_{11} AND S_{22} vs GATE NO. 2-TO-SOURCE VOLTAGE



S_{11} vs FREQUENCY



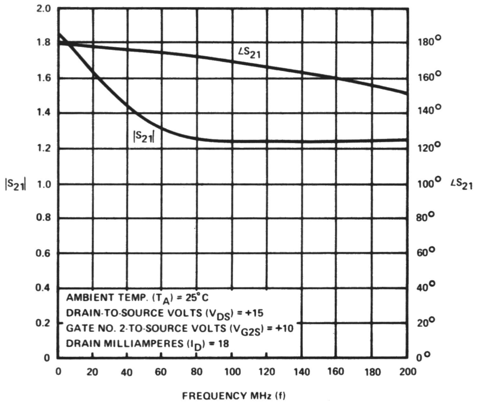
S_{12} vs FREQUENCY



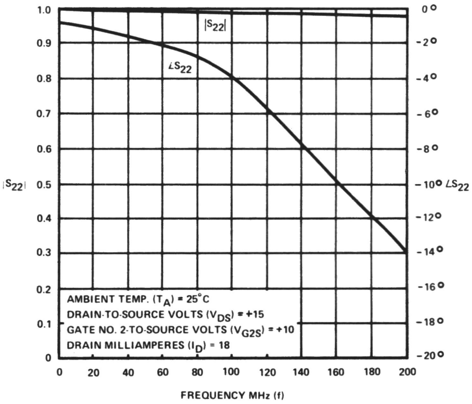
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

RF AMP SECTION

S_{21} vs FREQUENCY

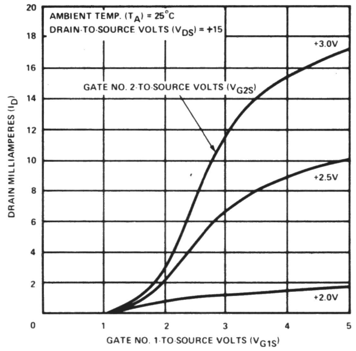


S_{22} vs FREQUENCY

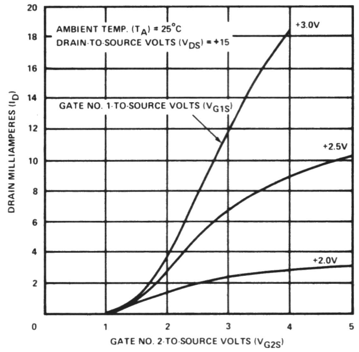


MIXER SECTION

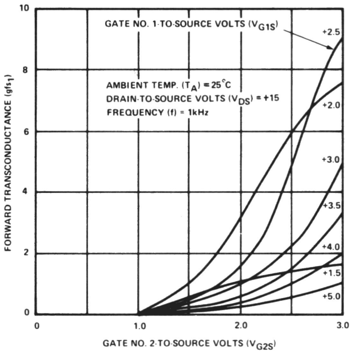
DRAIN CURRENT vs GATE NO. 1-TO-SOURCE VOLTAGE



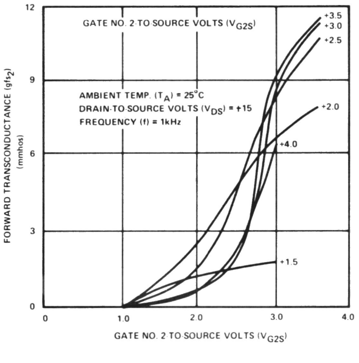
DRAIN CURRENT vs GATE NO. 2-TO-SOURCE VOLTAGE



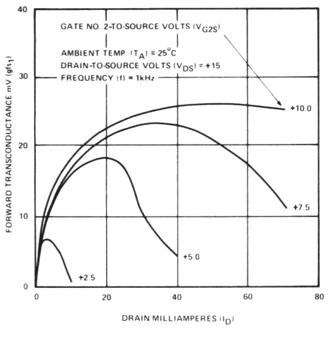
GATE NO. 1 FORWARD TRANSCONDUCTANCE vs GATE NO. 2-TO-SOURCE VOLTAGE



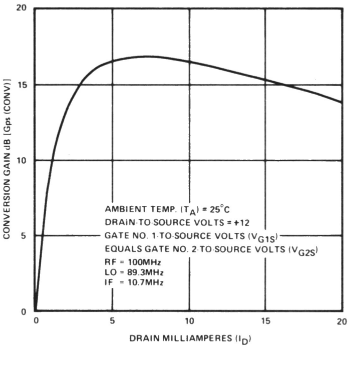
GATE NO. 2 FORWARD TRANSCONDUCTANCE vs GATE NO. 1-TO-SOURCE VOLTAGE



GATE NO. 1 FORWARD TRANSCONDUCTANCE vs DRAIN CURRENT

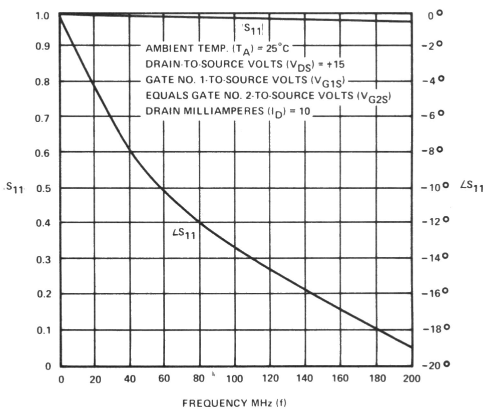


CONVERSION GAIN vs DRAIN CURRENT

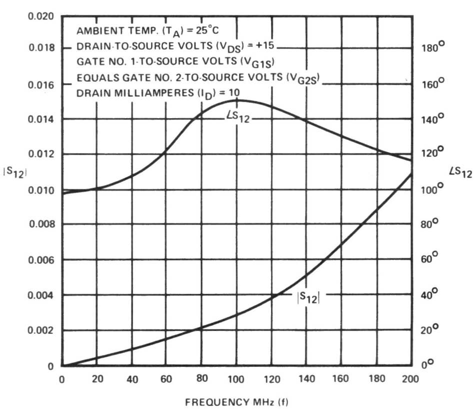


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

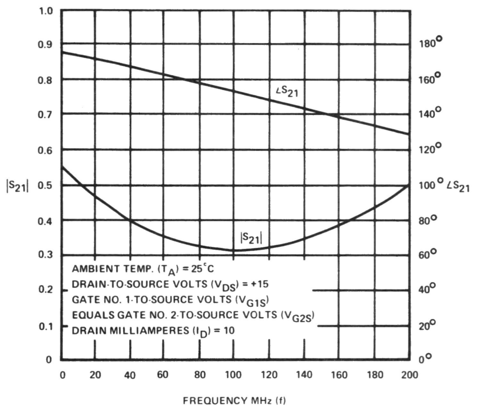
MIXER SECTION



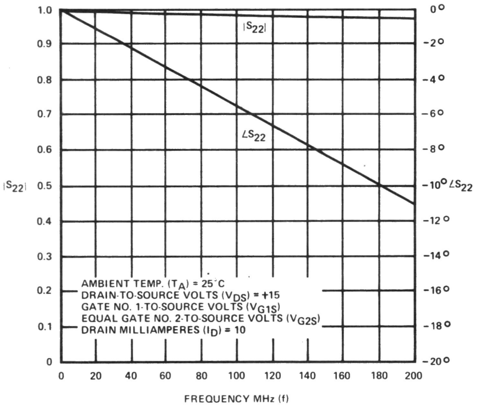
S11 vs FREQUENCY



S12 vs FREQUENCY



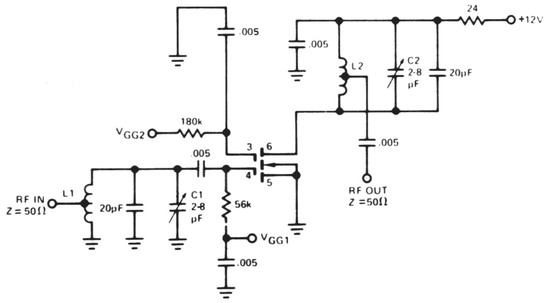
S21 vs FREQUENCY



S22 vs FREQUENCY

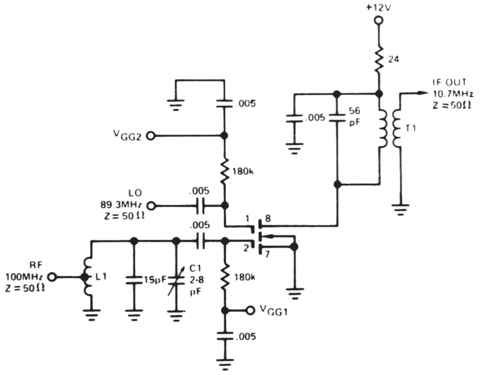
TEST CIRCUITS

RF AMP SECTION


.005
.005
24
+12V
L2
C2
2-8
pF
20pF
180k
VGG2
.005
3
6
4
5
.005
RF OUT
Z = 50Ω
RF IN
Z = 50Ω
L1
20pF
C1
2-8
pF
56k
VGG1
.005

L1-L2 5 turn #18 wire 3/16" dia. air core tapped at 1 turn
C1-C2 NPO, ERIE no. 538-011A-2-8

MIXER SECTION


+12V
24
IF OUT
10.7MHz
Z = 50Ω
.005
.005
56
pF
T1
VGG2
180k
LO
89.3MHz
Z = 50Ω
.005
.005
1
8
2
7
RF
100MHz
Z = 50Ω
L1
15pF
C1
2-8
pF
180k
VGG1
.005

T1 Cambion core = 533-3652-003
Carbonyl J core,
Primary coil 30 turns = 26 wire
Secondary coil 2 turns = 26 wire
L1 5 turns = 18 wire, 3/16" dia. air core
Tap 1 turn from ground side
C1 NPO, ERIE no. 538-011A-2-8

D-MOS FET QUAD ANALOG SWITCH ARRAYS, MULTIPLEXERS AND DRIVER

SD5000/SD5001/SD5002 SD5200

SD5000/5001/5002/5200-N,I

DESCRIPTION

The Signetics D-MOS SD5000 and 5200 series are monolithic arrays of silicon, insulated-gate, field-effect transistors using the N-channel enhancement mode technology.

This family of devices is designed to handle a wide variety of analog switching and driver applications. They are capable of high speed operation where excellent transient response, and wide voltage range are required. The SD5000 quad switch array quad multiplexer can handle high voltage analog signals (±10V). The SD5002 is designed for ±7.5V analog signals using ±15V power supplies. The SD5001 is designed for lower voltage applications. The SD5200 is intended for use as a 30V driver to complement the other switch products.

FEATURES

- **Low input capacitance: 2.4pF**
- **Low feedback capacitance: 0.3pF**
- **Low output capacitance: 1.3pF**
- **±10V analog signal range**
- **Low propagation delay time: 600ps**
- **Low on resistance: 30Ω**
- **Low feedthrough and feedback transients**
- **Ion implanted for greater reliability**
- **High channel-to-channel isolation: 107dB**
- **Transient protection for gates**
- **Military qualifications pending**

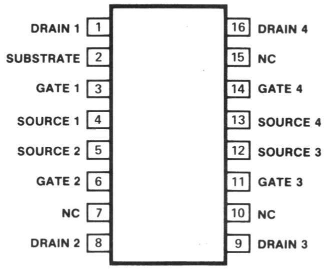
APPLICATIONS

- **SD5000 applications**
  - **Analog switching (up to very high frequencies)**
  - **Audio routing**
  - **Choppers**
  - **Crosspoint switches**
  - **Sample and hold**
- **SD5200 applications**
  - **Switch drivers**

PIN CONFIGURATIONS

I, N PACKAGE

(Top View)

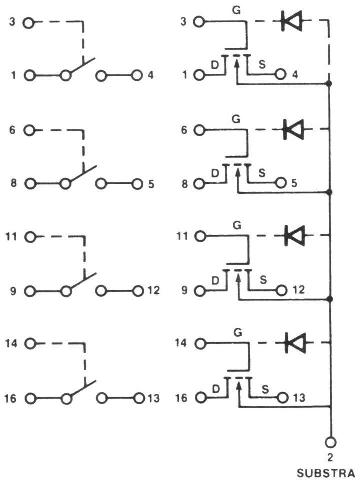


ORDER PART NO.

SD5000N,I SD5001N,I SD5002N,I SD5200N,I

FUNCTIONAL AND SCHEMATIC DIAGRAM

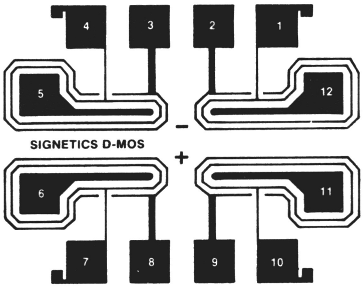
SD5000, 5001, 5002, 5200



SD5000/5001/5002/5200-N,I

CHIP DIAGRAM

SD5000, 5001, 5002, 5200
SWITCH ARRAYS



PAD NO.	PAD FUNCTION
1	Gate No. 1
2	Source No. 1
3	Source No. 2
4	Gate No. 2
5	Drain No. 2
6	Drain No. 3
7	Gate No. 3
8	Source No. 3
9	Source No. 4
10	Gate No. 4
11	Drain No. 4
12	Drain No. 1

Die Size 40X32

ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$ unless otherwise specified.

PARAMETER		SD5000	SD5001	SD5002	SD5200	UNIT
V_{DS}	Drain-to-source	+20	+10	+15	+30	Vdc
V_{SD}	Source-to-drain[1]	+20	+10	+15	+.5	Vdc
V_{DB}	Drain-to-substrate	+25	+15	+22.5	+30	Vdc
V_{SB}	Source-to-substrate	+25	+15	+22.5	+15	Vdc
V_{GS}	Gate-to-source	+30	+25	+30	+25	Vdc
		-25	-15	-22.5		
V_{GB}	Gate-to-substrate	+30	+25	+30	+25	Vdc
		-0.3	-0.3	-0.3	-0.3	
V_{GD}	Gate-to-drain	+30	+25	+30	+25	Vdc
		-25	-15	-22.5		
I_D	Drain current	50	50	50	50	mA
Ambient temperature range						
	Storage	-55 to +150				°C
	Operating	0 to +85				°C
Power Dissipation						
	Total package dissipation[2]	640				mW
	Individual transistor dissipation	300				mW

NOTES

1. Refer to test conditions specified in Electrical Characteristics Table.
2. Derated 5mW per degree centigrade.

DC ELECTRICAL CHARACTERISTICS $T_A = +25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SD5000			SD5001			UNIT
			Min	Typ	Max	Min	Typ	Max	
BREAKDOWN VOLTAGE									
BV_{DS}	Drain-to-source	$V_{GS} = V_{BS} = -5V$, $I_S = 10nA$	20	25		10	25		V
BV_{SD}	Source-to-drain	$V_{GD} = V_{BD} = -5V$, $I_D = 10nA$	20			10			V
BV_{DB}	Drain-to-substrate	$V_{GB} = 0V$, source Open							
		$I_D = 10nA$	25			15			V
BV_{SB}	Source-to-substrate	$V_{GB} = 0V$, drain Open							
		$I_S = 10\mu A$	25			15			V
LEAKAGE CURRENT									
$I_{DS}(OFF)$	Drain-to-source	$V_{GS} = V_{BS} = -5V$							
		$V_{DS} = +20V$		1	10				nA
		$V_{DS} = +10V$					1	10	nA
$I_{SD}(OFF)$	Source-to-drain	$V_{GD} = V_{BD} = -5V$							
		$V_{SD} = +20V$		1	10				nA
		$V_{SD} = +10V$					1	10	nA
I_{GBS}	Gate	$V_{DB} = V_{SB} = 0V$							
		$V_{GB} = 30V$			1				μA
		$V_{GB} = 25V$						1	μA
V_T	Threshold voltage	$V_{DS} = V_{GS} = V_T$, $I_S = 1\mu A$ $V_{SB} = 0V$	0.1	1.0	2.0	0.1	1.0	2.0	V
$r_{DS}(ON)$	Drain-to-source-resistance	$I_D = 1.0mA$, $V_{SB} = 0$							
		$V_{GS} = +5V$		50	70		50	70	Ω
		$V_{GS} = +10V$		30			30		Ω
		$V_{GS} = +15V$		23			23		Ω
		$V_{GS} = +20V$		19			19		Ω
$r_{DS}(ON)$	Resistance match	$I_D = 1.0mA$, $V_{SB} = 0$							
		$V_{GS} = +5V$		1	5		1	5	Ω

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = +25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SD5002			UNIT
			Min	Typ	Max	
BREAKDOWN VOLTAGE						
BV_{DS}	Drain-to-source	$V_{GS} = V_{BS} = -5V$, $I_S = 10nA$	15	25		V
		$V_{GS} = V_{BS} = 0V$, $I_S = 1\mu A$				V
BV_{SD}	Source-to-drain	$V_{GD} = V_{BD} = -5V$, $I_D = 10nA$	15			V
BV_{DB}	Drain-to-substrate	$V_{GB} = 0V$, source Open				
		$I_D = 10nA$	22.5			V
		$I_D = 1\mu A$				V
BV_{SB}	Source-to-substrate	$V_{GB} = 0V$, drain Open				
		$I_S = 10\mu A$	22.5			V
LEAKAGE CURRENT						
$I_{DS}(OFF)$	Drain-to-source	$V_{GS} = V_{BS} = -5V$				
		$V_{DS} = +15V$		1	10	nA
		$V_{GS} = V_{BS} = 0V$, $V_{DS} = +10V$				nA
$I_{SD}(OFF)$	Source-to-drain	$V_{GD} = V_{BD} = -5V$				
		$V_{SD} = +15V$		1	10	nA
I_{GBS}	Gate	$V_{DB} = V_{SB} = 0V$				
		$V_{GB} = 30V$			1	μA
		$V_{GB} = 25V$				μA
V_T	Threshold voltage	$V_{DS} = V_{GS} = V_T$, $I_S = 1\mu A$	0.1	1.0	2.0	V
		$V_{SB} = 0V$				
$r_{DS}(ON)$	Drain-to-source-resistance	$I_D = 1.0mA$, $V_{SB} = 0$				
		$V_{GS} = +5V$		50	70	Ω
		$V_{GS} = +10V$		30		Ω
		$V_{GS} = +15V$		23		Ω
		$V_{GS} = +20V$		19		Ω
$r_{DS}(ON)$	Resistance match	$I_D = 1.0mA$, $V_{SB} = 0$				
		$V_{GS} = +5V$		1	5	Ω

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = +25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SD5200			UNIT
			Min	Typ	Max	
BREAKDOWN VOLTAGE						
BV_{DS}	Drain-to-source					
		$V_{GS} = V_{BS} = 0V$, $I_S = 1\mu A$				
		$V_{GS} = V_{BS} = 0V$, $I_D = 10\mu A$	30	35		V
BV_{SD}	Source-to-drain	$V_{GD} = V_{BD} = -5V$, $I_D = 10nA$				V
BV_{DB}	Drain-to-substrate	$V_{GB} = 0V$, source Open				
		$I_D = 1\mu A$				V
BV_{SD}	Source-to-substrate	$V_{GB} = 0V$, drain Open				
		$I_S = 10\mu A$				V
LEAKAGE CURRENT						
$I_{DS}(OFF)$	Drain-to-source	$V_{GS} = V_{BS} = 0V$, $V_{DS} = +10V$				nA
I_{GBS}	Gate	$V_{DB} = V_{SB} = 0V$				
		$V_{GB} = 25V$			1	μA
V_T	Threshold voltage	$V_{DS} = V_{GS} = V_T$, $I_S = 1\mu A$	0.5	1.0	2.0	V
		$V_{SB} = 0V$				
$r_{DS}(ON)$	Drain-to-source-resistance	$I_D = 1.0mA$, $V_{SB} = 0$				
		$V_{GS} = +5V$		50	80	Ω
		$V_{GS} = +10V$		30		Ω
		$V_{GS} = +15V$		23		Ω
		$V_{GS} = +20V$		19		Ω
$r_{DS}(ON)$	Resistance match	$I_D = 1.0mA$, $V_{SB} = 0$				
		$V_{GS} = +5V$				Ω

AC ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	SD5000			SD5001			UNIT
			Min	Typ	Max	Min	Typ	Max	
gfs	Forward transconductance	$V_{DS} = 10V$, $V_{SB} = 0V$	10	15		10	15		mmhos
		$I_D = 20mA$, $f = 1kHz$							
	Small signal capacitances	$V_{DS} = 10V$, $f = 1MHz$							
		$V_{GS} = V_{BS} = -15V$							
$C_{(GS+GD+GB)}$	Gate node	See capacitance model		2.4	3.5		2.4	3.5	pF
$C_{(GD+DB)}$	Drain node	in Figure 1		1.3	1.5		1.3	1.5	pF
$C_{(GS+SB)}$	Source node			3.5	4.0		3.5	4.0	pF
C_{DG}	Reverse transfer			0.3	0.5		0.3	0.5	pF
C_T	Cross talk	See test circuits		-107			-107		dB
		no. 1 and 2, $f = 3kHz$							

AC ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS	SD5002 Min	SD5002 Typ	SD5002 Max	UNIT
gfs	Forward transconductance	$V_{DS} = 10V$, $V_{SB} = 0V$ $I_D = 20mA$, f = 1kHz	10	15		mmhos
	Small signal capacitances	$V_{DS} = 10V$, f = 1MHz $V_{GS} = V_{BS} = -15V$				
$C_{(GS+GD+GB)}$	Gate node	See capacitance model in Figure 1		2.4	3.5	pF
$C_{(GD+DB)}$	Drain node			1.3	1.5	pF
$C_{(GS+SB)}$	Source node			3.5	4.0	pF
C_{DG}	Reverse transfer			0.3	0.5	pF
C_T	Cross talk	See test circuits no. 1 and 2, f = 3kHz		-107		dB

AC ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS	SD5200 Min	SD5200 Typ	SD5200 Max	UNIT
gfs	Forward transconductance	$V_{DS} = 10V$, $V_{SB} = 0V$ $I_D = 20mA$, f = 1kHz	10	15		mmhos
	Small signal capacitances	$V_{DS} = 10V$, f = 1MHz $V_{GS} = V_{BS} = -15V$				
$C_{(GS+GD+GB)}$	Gate node	See capacitance model in Figure 1		2.4	3.5	pF
$C_{(GD+DB)}$	Drain node			1.3	1.5	pF
C_{DG}	Reverse transfer			0.3	0.5	pF
C_T	Cross talk	See test circuits no. 1 and 2, f = 3kHz		-107		dB

THEORY OF OPERATION

The SD5000 series consists of four SPST switches with analog signal capability of up to ±10 volts for the SD5000 and ±7.5 volts for the SD5002. Each switch of the array is a D-MOS N-channel field-effect transistor of the enhancement-mode type; that is, the device is normally off when gate-to-source voltage (V_{GS}) is zero volts. When V_{GS} exceeds the threshold voltage, V_T, the FET switch starts to turn ON with V_{GS} in excess of +10 volts, a low resistance path (typically 30Ω) exists between input and output of the switch. Figure 1 shows the normal mode of operation of a single switch of the array for ±5 volt analog signal processing. Note that the source is recommended for the input since feedback or reverse transfer capacitance is lower when drain is used as the output. In this case, the switch is driven by ±10 volts for which the SD5200 could be used as discussed later. When analog signals are routed from one point to another the important factors are **isolation, crosstalk between switches, feedthrough and feedback transients, insertion loss and speed of operation**. The SD5000 series offers superior performance in all these areas (Figure 1).

Isolation. ON resistance is typically 30Ω and OFF resistance is typically 10^{10}Ω, which results in an OFF to ON resistance ratio in excess of 10^9. Isolation from output to input from 3kHz analog signals is typically -107dB.

Feedback and feedthrough transients. These are kept to a minimum because of the very low feedback and feedthrough capacitances. This means that "glitchless" or "clean" signals appear at the output.

Insertion loss. This depends upon the source and load impedances involved. As an example, for 600Ω source impedance the insertion loss for voice signals (1V RMS at 3kHz) is less than 0.3dB. This indicates that the SD5000 series would make good telephone cross-point switches.

Speed. Because of the low ON resistance and low input capacitance, the SD5000 switches turn ON at sub-nanosecond speeds. They are also capable of handling very high frequency analog signals and still maintain excellent isolation (20-30dB at 1GHz).

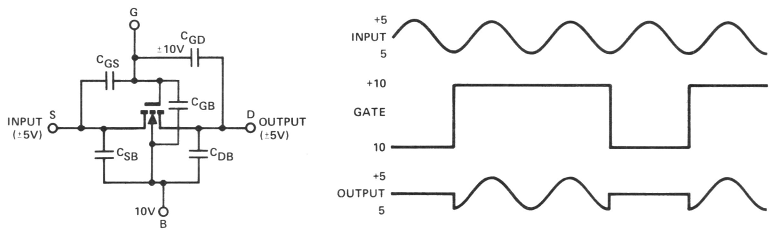


Figure 1

The SD5200 is intended as a driver for the SD5000/5001/5002 but is capable of driving any system which requires ±15 volts. Four drivers are in each package and Figure 2 shows how a single driver is biased for ±15 volts. Two external resistors, R_1 and R_2, and a zener diode, D_1, are required per driver. The input is 5V open collector TTL (Figure 2).

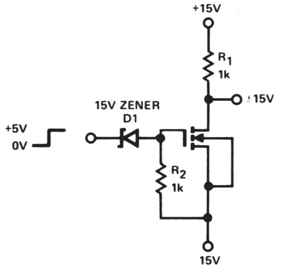

+15V
R_1
1k
±15V
15V ZENER
D1
+5V
0V
R_2
1k
15V

Figure 2

ANALOG SWITCH/DRIVER APPLICATION

The SD5200 operates as an inverting switch capable of driving 30 volts maximum. This wide range capability with high speed fulfills most analog switching applications. Figure 3 demonstrates how the SD5000 drives the SD5000 in a typical analog switching application (Figure 3).

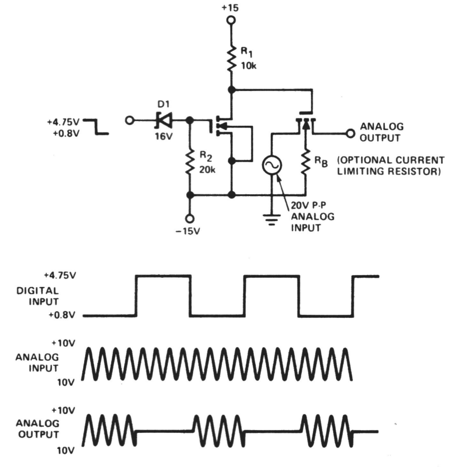
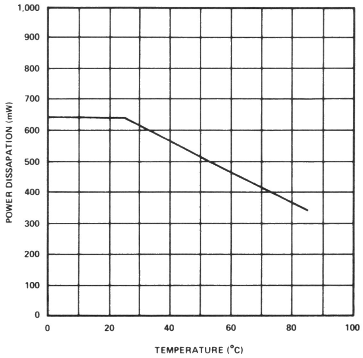

+15
R_1
10k
D1
+4.75V
+0.8V
16V
R_2
20k
−15V
ANALOG OUTPUT
R_B (OPTIONAL CURRENT LIMITING RESISTOR)
20V P-P ANALOG INPUT
+4.75V
DIGITAL INPUT
+0.8V
+10V
ANALOG INPUT
10V
+10V
ANALOG OUTPUT
10V

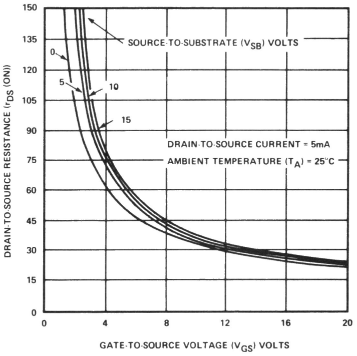
Figure 3

TYPICAL PERFORMANCE CHARACTERISTICS

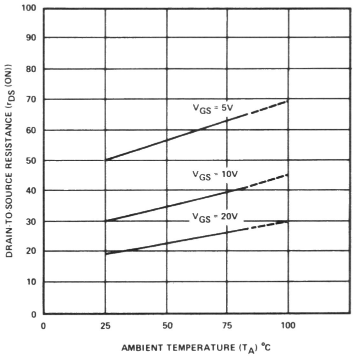
MAXIMUM POWER DISSIPATION vs TEMPERATURE



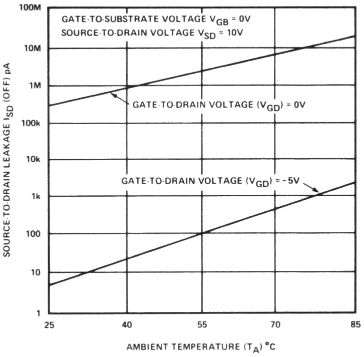
DRAIN-TO-SOURCE RESISTANCE vs SOURCE-TO-SUBSTRATE AND GATE-TO-SOURCE VOLTAGE



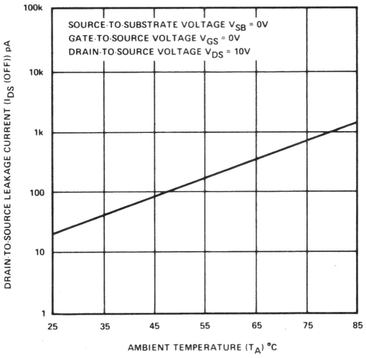
DRAIN-TO-SOURCE RESISTANCE vs TEMPERATURE



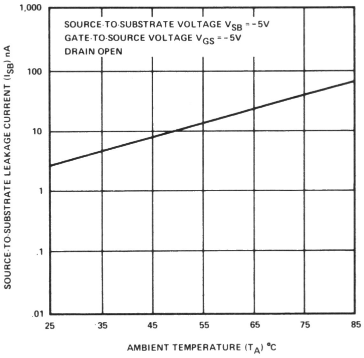
SOURCE-TO-DRAIN LEAKAGE CURRENT vs TEMPERATURE



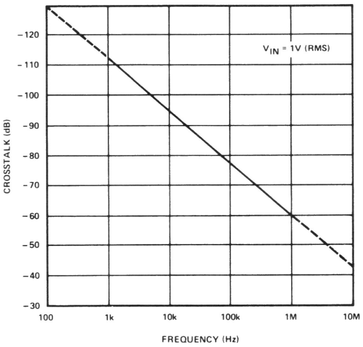
DRAIN-TO-SOURCE LEAKAGE CURRENT vs TEMPERATURE



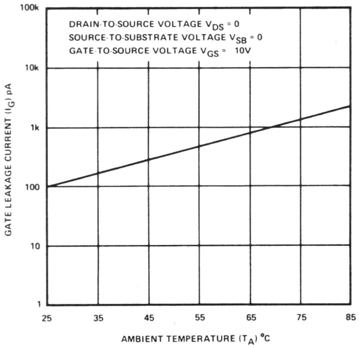
SOURCE-TO-SUBSTRATE LEAKAGE CURRENT vs TEMPERATURE



CROSSTALK vs FREQUENCY



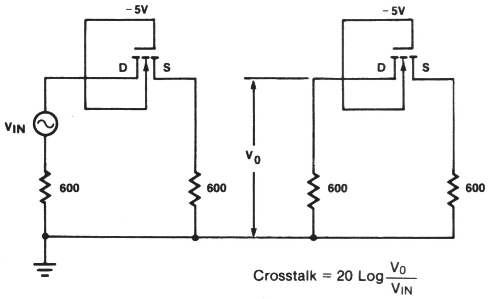
GATE LEAKAGE CURRENT vs TEMPERATURE



TEST CIRCUIT

CROSSTALK MEASUREMENT

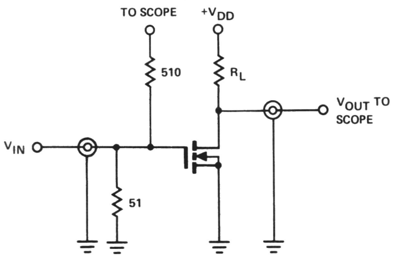
Quad Switch
SD5000/SD5001/SD5002


−5V
D
S
−5V
D
S
V_{IN}
V_0
600
600
600
600

Crosstalk = $20 \text{ Log} \frac{V_O}{V_{IN}}$

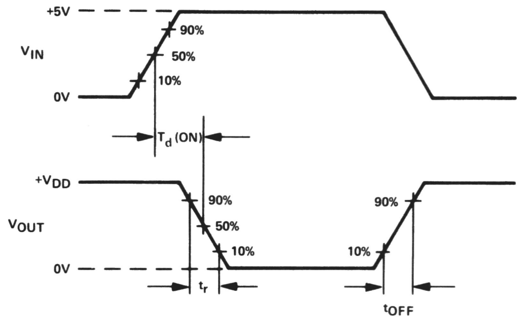
Where V_{IN} = 1V RMS at 3kHz

SWITCHING TEST CIRCUIT


TO SCOPE
$+V_{DD}$
510
R_L
V_{OUT} TO SCOPE
V_{IN}
51

Input Pulse	Sampling Scope
t_r, t_F < 1ns	t_r < 350ps
Pulse Width = 100ns	R_{IN} = 1MΩ
Rep Rate = 1MHz	C_{IN} = 2.0pF

SWITCHING WAVEFORMS


+5V
V_{IN}
0V
90%
50%
10%
T_d (ON)
$+V_{DD}$
V_{OUT}
0V
90%
50%
10%
90%
10%
t_r
t_{OFF}

SWITCHING CHARACTERISTICS

		t_d (ON) (ns)		t_r (ns)		t_{OFF} (ns)*	
V_{DD}	R_L	TYP	MAX	TYP	MAX	TYP	MAX
5	680	0.6	1.0	0.7	1.0	9.0	
10	680	0.7		0.8		9.0	
15	1k	0.9		1.0		14.0	

*t_{OFF} is dependent on R_L and C_L and does not depend on the device characteristics.

D-MOS 8X2 ANALOG/DIGITAL SWITCHING ARRAYS

SD5301
SD5302

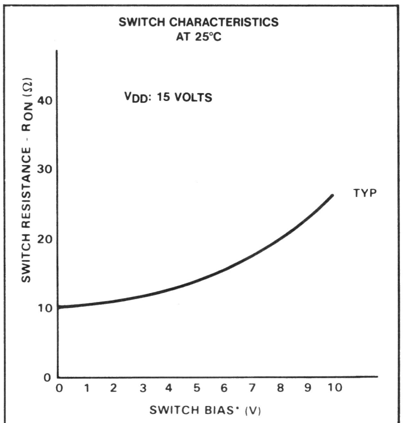
DESCRIPTION

The SD5301/SD5302 D-MOS 8X2 Switching Arrays are monolithic chips consisting of 16 D-MOS enhancement mode transistors arranged in an 8X2 switching matrix. Control is included on the chip to provide a complete switching subsystem which has minimum pinout and is easily expandable to larger arrays.

FEATURES

- **Excellent bilateral transmission specifications**
- **Useful in unbalanced or balanced networks**
- **On chip control and decoding**
- **Easy adaptation to microcomputer control**
- **Serial control input, independent of signal paths**
- **No latch-up from spurious signals on signal paths**
- **Easy system design for cost reduction as switch array density increases**
- **Easy expansion to larger systems with minimum external components**
- **Single supply operation**
- **Open collector TTL and C-MOS compatible inputs**
- **Encoded chip select**

TYPICAL PERFORMANCE CHARACTERISTICS

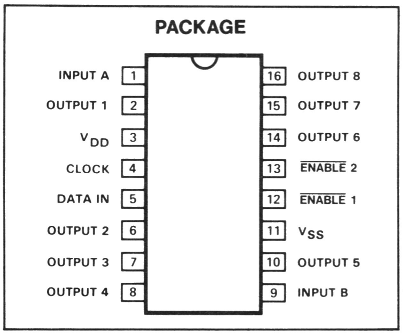


*Switch bias determines the On resistance (R_{ON}) of a particular switch, i.e. if switch A• 4 was On and input A & Output 4 = 5V, then R_{ON} = 14Ω typ

APPLICATIONS

- **PABX/Key switching networks**
- **Video switching**
- **Analog signal routing/multiplexing**
- **Digital routing**

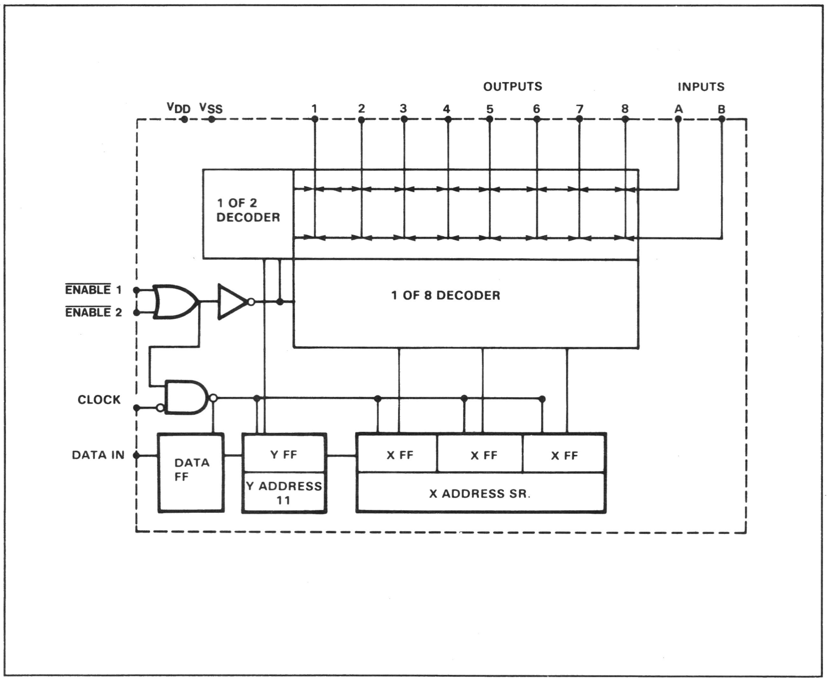
PIN CONFIGURATION


PACKAGE
INPUT A 1
OUTPUT 1 2
VDD 3
CLOCK 4
DATA IN 5
OUTPUT 2 6
OUTPUT 3 7
OUTPUT 4 8
9 INPUT B
10 OUTPUT 5
11 VSS
12 ENABLE 1
13 ENABLE 2
14 OUTPUT 6
15 OUTPUT 7
16 OUTPUT 8

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
T_A	Operating ambient temperature	0 to +70	°C
t_{stg}	Storage temperature	−65 to +150	°C
P_D	Package dissipation		
	At T_A = 25°C	640 max	mW
	Above 25°C	Derate at 5.1	mW/°C
T_J	Junction temperature	150	°C
	V_{DD}, data, clock and enable voltages with respect to V_{SS}	−0.3 to +16.0	V

BLOCK DIAGRAM


OUTPUTS
INPUTS
VDD VSS
1 2 3 4 5 6 7 8
A B
1 OF 2 DECODER
ENABLE 1
ENABLE 2
1 OF 8 DECODER
CLOCK
DATA IN
DATA FF
Y FF
Y ADDRESS 11
X FF
X FF
X FF
X ADDRESS SR.

DC ELECTRICAL CHARACTERISTICS[1] $T_A = 25°C$, $V_{DD} = 15Vdc \pm 5\%$, $V_{SS} = 0Vdc$ unless otherwise specified

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
R_{ON}	Switch on resistance^2	$V_{DD} = 15V$, $V_{AB} = V_{1\text{-}8} = 1.8$ Vdc, $I_D = 1mA$				Ω
		$T_A = 25°C$	7	11	15	
	SD5301	$T_A = 0°C$ to $70°C$	5		20	
		$V_{DD} = 10V$, $T_A = 25°C$		18		
R_{ON}	Switch on resistance	$V_{DD} = 15V$, $V_{AB} = V_{1\text{-}8} = 1.8$ Vdc, $I_D = 1mA$				Ω
		$T_A = 25°C$	7		30	
	SD5302	$T_A = 0°C$ to $70°C$	5		40	
		$V_{DD} = 10V$, $T_A = 25°C$				
I_{DD}	Supply current			4	7	mA
	Input leakage	$V_{IN} = 5V$				µA
I_Φ	Clock			.001	1	
I_D	Data			.001	1	
I_E	$\overline{\text{Enable}}$ 1 and $\overline{\text{Enable}}$ 2			.001	1	
	Switch leakage					µA
$I_{1\text{-}8}$	1-8 outputs					
		$V_{1\text{-}8} = 4.5Vdc$, $V_{AB} = 1.5Vdc$		.01	1	
I_{AB}	A,B inputs					
		$V_{AB} = 4.5Vdc$, $V_{1\text{-}8} = 1.5Vdc$		.1	1	
	Capacitance					pF
C_Φ	Clock			3.5		
C_D	Data	Inputs = 0Vdc, f = 1MHz		4.5		
C_E	$\overline{\text{Enable}}$ 1 and $\overline{\text{Enable}}$ 2			3.0		
C_A,C_B	A,B inputs	$V_{DD} = V_{SS} = 0Vdc$, $V_A = V_B = 2.5Vdc$		150		
C_1-C_8	1-8 outputs	$V_{1\text{-}8} = 2.5Vdc$, f = 1MHz		8		
	Input voltage	All digital inputs				V
V_{IL}	Low		−0.3		0.8	
V_{IH}	High		5.0		15.0	

AC ELECTRICAL CHARACTERISTICS[1]

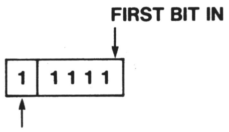
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
CT	Crosstalk	See Figure 1		−105	−90	dB
I_O	Off isolation	See Figure 2		−105	−90	dB
f	Clock frequency	Clock voltage = 0Vdc when f = 0Hz	0	2.0	1.0	MHz
T_{LG}	Lag time	See Figure 3				ns
	Data and enable (5)		100			
	Lead time	See Figure 3				ns
T_{LD1}	Data and enable (5)		400			
T_{LD2}			150			
T_W	Write time	See Figure 3		2.0	3.0	µs
Φ_{PW}	Clock pulse width	Measured at 3.0Vdc level	0.4		100	µs
		$t_{rise} = t_{fall} \leq 500$ ns				

NOTES

1. These specs apply to both the SD5301 and SD5302 except where separately specified.
2. ΔR_{ON} for the crosspoints of a single SD5301 is typically $\pm 2\Omega$.

	1	2	3	4	5	6	7	8
INPUT A	1 1 1 1	1 0 1 1	1 1 0 1	1 0 0 1	1 1 1 0	1 0 1 0	1 1 0 0	1 0 0 0
INPUT B	0 1 1 1	0 0 1 1	0 1 0 1	0 0 0 1	0 1 1 0	0 0 1 0	0 1 0 0	0 0 0 0

EXAMPLE:


FIRST BIT IN
1
1 1 1 1

"1" = SWITCH ON, "0" SWITCH OFF

Table 1 SD5301/SD5302 SWITCHING CODES

CROSSTALK MEASUREMENTS

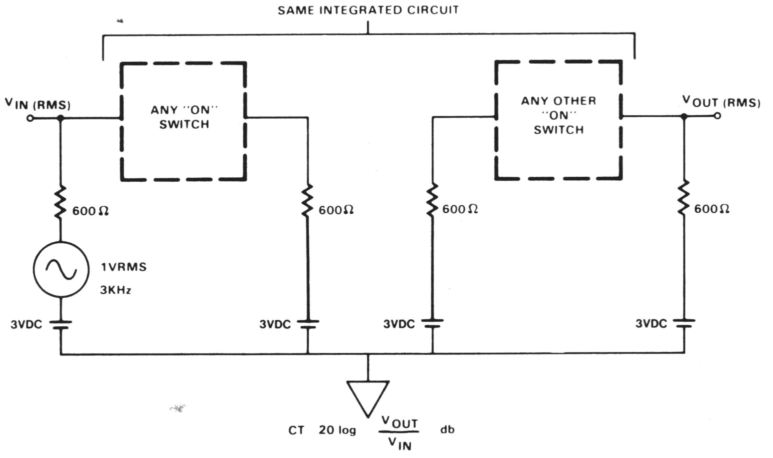

SAME INTEGRATED CIRCUIT
V IN (RMS)
ANY "ON" SWITCH
ANY OTHER "ON" SWITCH
V OUT (RMS)
600Ω
600Ω
600Ω
600Ω
1VRMS
3KHz
3VDC
3VDC
3VDC
3VDC
CT 20 log V OUT / V IN db

Figure 1

OFF ISOLATION MEASUREMENT

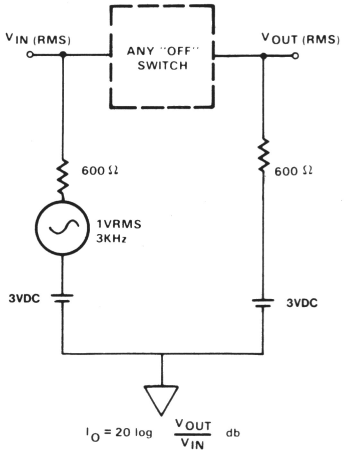

V IN (RMS)
ANY "OFF" SWITCH
V OUT (RMS)
600 Ω
600 Ω
1VRMS
3KHz
3VDC
3VDC
I O = 20 log V OUT / V IN db

Figure 2

TIMING DIAGRAM

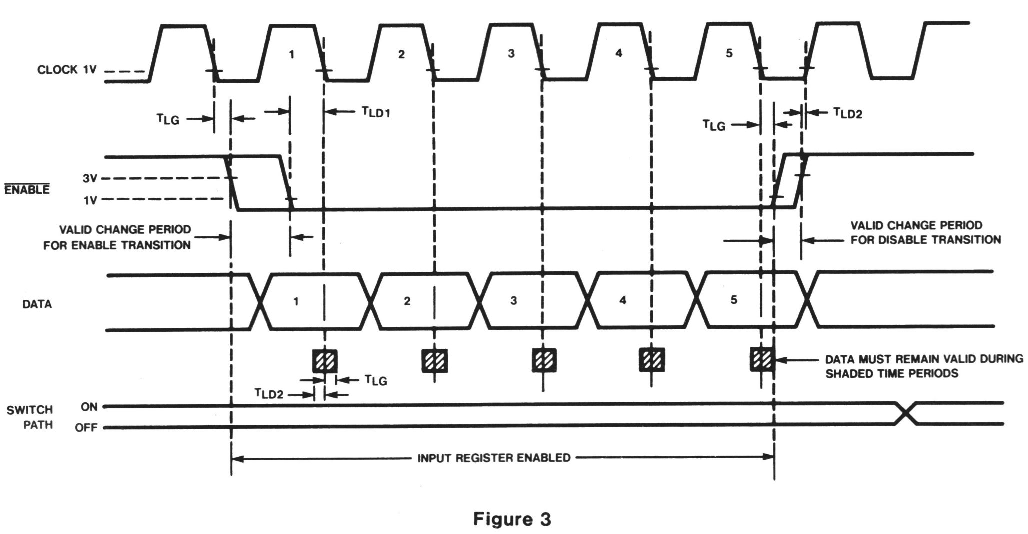

CLOCK 1V
1
2
3
4
5
TLG
TLD1
TLG
TLD2
ENABLE
3V
1V
VALID CHANGE PERIOD FOR ENABLE TRANSITION
VALID CHANGE PERIOD FOR DISABLE TRANSITION
DATA
1
2
3
4
5
DATA MUST REMAIN VALID DURING SHADED TIME PERIODS
TLD2
TLG
SWITCH PATH
ON
OFF
INPUT REGISTER ENABLED

Figure 3

THEORY OF OPERATION

The 8x2 array consists of 16 switches. Each switch consists of one low impedance D-MOS transistor and a gated flip-flop to maintain the required On or Off state.

To establish the status of any switch, the enable inputs for the 8x2 array must be selected as shown in Figure 3. This disables the decoder preventing accidental changing of voice paths and simultaneously enables the clock input for this array. With the circuit enabled, 5 bits of serial data are fed into the data/address pin. The first 4 bits are decoded to select one of the 16 switches. The selected switch will be turned on or off by the fifth bit. At this point, the circuit is disabled and the decoders are enabled. The switch will be updated within 3.0μs after the enable line has been disabled. The device is now ready to accept new data

APPLICATIONS

A typical PABX interface network is shown in Figure 4. This configuration is unbalanced. A balanced configuration can be made by tying the control lines of two SD5301s in parallel which allows a simple control of the balanced switch.

The SD5301 may be used in a variety of digital/analog routing and multiplexing applications. Application examples are shown in Figure 5 and Figure 6.

NOTE

All references to SD5301 in the text also apply to the SD5302.

PABX APPLICATION

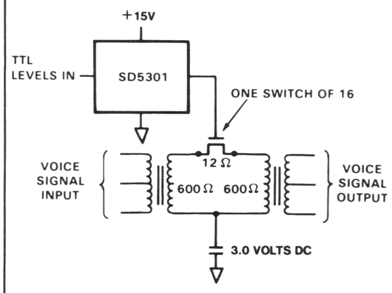
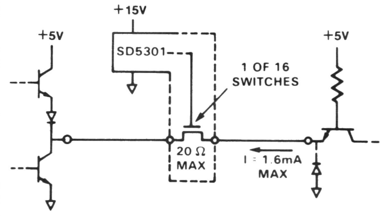

+15V
TTL LEVELS IN
SD5301
ONE SWITCH OF 16
VOICE SIGNAL INPUT
12 Ω
600 Ω
600 Ω
VOICE SIGNAL OUTPUT
3.0 VOLTS DC

Figure 4

DIGITAL ROUTING/ MULTIPLEXING APPLICATION


+15V
+5V
SD5301
1 OF 16 SWITCHES
+5V
20 Ω MAX
I = 1.6mA MAX

Maximum voltage drop across SD5301 switch is 20 Ω x 1.6mA = 32mV

Figure 5

VARIABLE GAIN CONTROL CIRCUIT EMPLOYING ONE SD5301 AND ONE MC1458

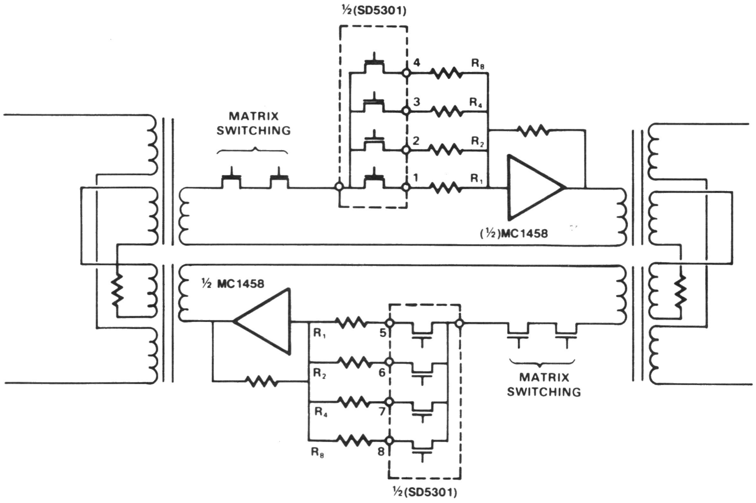

½(SD5301)
4
R₈
3
R₄
2
R₂
1
R₁
MATRIX SWITCHING
(½)MC1458
½ MC1458
R₁
5
R₂
6
R₄
7
R₈
8
MATRIX SWITCHING
½(SD5301)

Figure 6

SECTION 16
NEW PRODUCTS

Section 16—NEW PRODUCTS

NE5034	8-Bit SAR A/D Converter	407
NE5044	Programmable Seven Channel RC Encoder	408
NE5045	Seven Channel RC Decoder	409
NE5046	2 Channel RC Decoder	410
NE/SE5512	High Performance Operational Amplifier	411
NE/SE5514	High Performance Operational Amplifier	411
NE5539	Ultra High Frequency Operational Amplifier	412
ULN2212	1-Watt TV/FM Sound Channel	413
ST100	μ255 PCM CODEC	414
NE5020	10-Bit Microprocessor MP Compatible DAC	*
NE647	Low Voltage Dolby-B Noise Reduction Circuit	*
NE5557	Precision Voltage Reference Source	*
SD224H	Power FET Single Gate N-Channel Enhancement	415

NOTE

*Any product listed in this section but not incorporated within the text may be obtained by writing Information Services at Signetics, 811 E. Arques, M/S 027, Sunnyvale, California 94086, or by calling (408) 746-1682.

8 BIT GENERAL PURPOSE ANALOG TO DIGITAL CONVERTER NE5034

F,N

DESCRIPTION

The 5034 is an 8-bit resolution analog-to-digital converter. The 5034 contains all of the elements comprising a true 8-bit accuracy analog-to-digital converter on one monolithic chip. These elements include the logic, voltage reference, comparator, clock, and output buffers. The output buffers are microprocessor addressable for three-state bus compatibility.

The 5034 achieves fast conversion time (17 microseconds, Typ) using a single external capacitor to set the internal clock frequency. Faster conversion times are possible using an external clock.

FEATURES

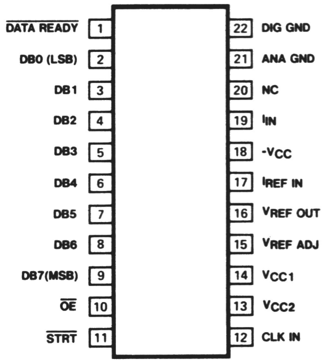
- **8-bit resolution and accuracy**
- **Microprocessor compatible logic**
- **Internal clock with external override for higher speed**
- **No missing codes over full operating temperature range**

APPLICATIONS

- **A/D converters in microprocessor based systems**
- **High speed A/D systems**
- **Ratiometric A/D conversion**
- **Automated process controls**
- **Low cost A/D systems**

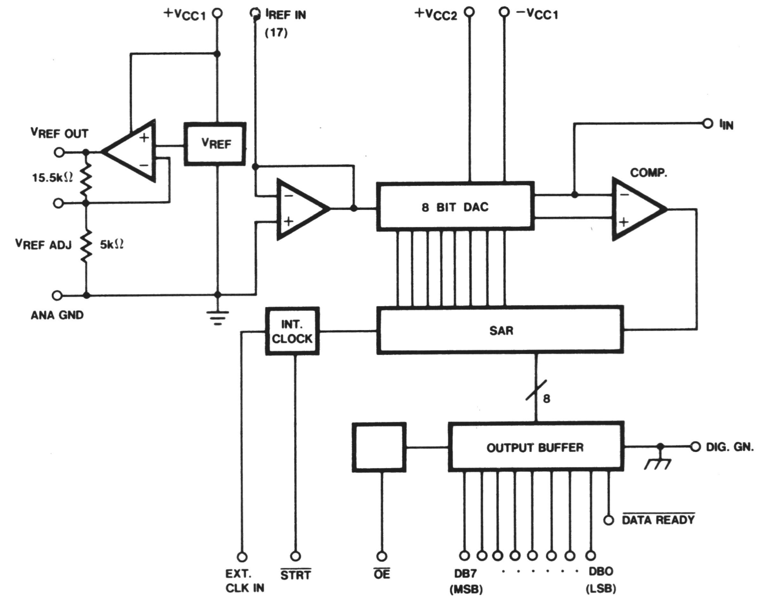
PIN CONFIGURATION

F,N PACKAGE


DATA READY 1
DB0 (LSB) 2
DB1 3
DB2 4
DB3 5
DB4 6
DB5 7
DB6 8
DB7(MSB) 9
OE 10
STRT 11
22 DIG GND
21 ANA GND
20 NC
19 IIN
18 -VCC
17 IREF IN
16 VREF OUT
15 VREF ADJ
14 VCC1
13 VCC2
12 CLK IN

NE 5034 N Plastic DIP Package
NE 5034 F Ceramic DIP Package

BLOCK DIAGRAM


+VCC1
IREF IN
(17)
+VCC2
−VCC1
IIN
VREF OUT
VREF
15.5kΩ
COMP.
8 BIT DAC
VREF ADJ
5kΩ
ANA GND
INT.
CLOCK
SAR
8
OUTPUT BUFFER
DIG. GN.
DATA READY
EXT.
CLK IN
STRT
OE
DB7
(MSB)
DB0
(LSB)

PROGRAMMABLE SEVEN CHANNEL RC ENCODER NE5044

OBJECTIVE SPECIFICATION
March 1979

DESCRIPTION

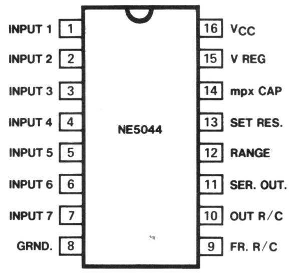
The NE5044 is a programmable parallel input, serial output pulsewidth encoder. A multiplexed dual linear ramp technique is used to allow up to 7 inputs to be converted to a serial pulsewidth modulated signal with excellent linearity and minimal crosstalk. Fixed or variable frame rates can be used, externally controlled, for ease of demodulation.

Features

- **3 to 7 channels, externally selectable**
- **Constant current dual linear ramp for linearity better than .5%**
- **Internal voltage regulator for low drift**
- **Wide supply range 6 – 16V**
- **Fixed or variable frame rate set by external R-C**
- **External control for channel gain or range**
- **Versatile applications; exponential rates, mixing, dual rate, reversing etc.**
- **Minimum external components**

PIN CONFIGURATION

N PACKAGE

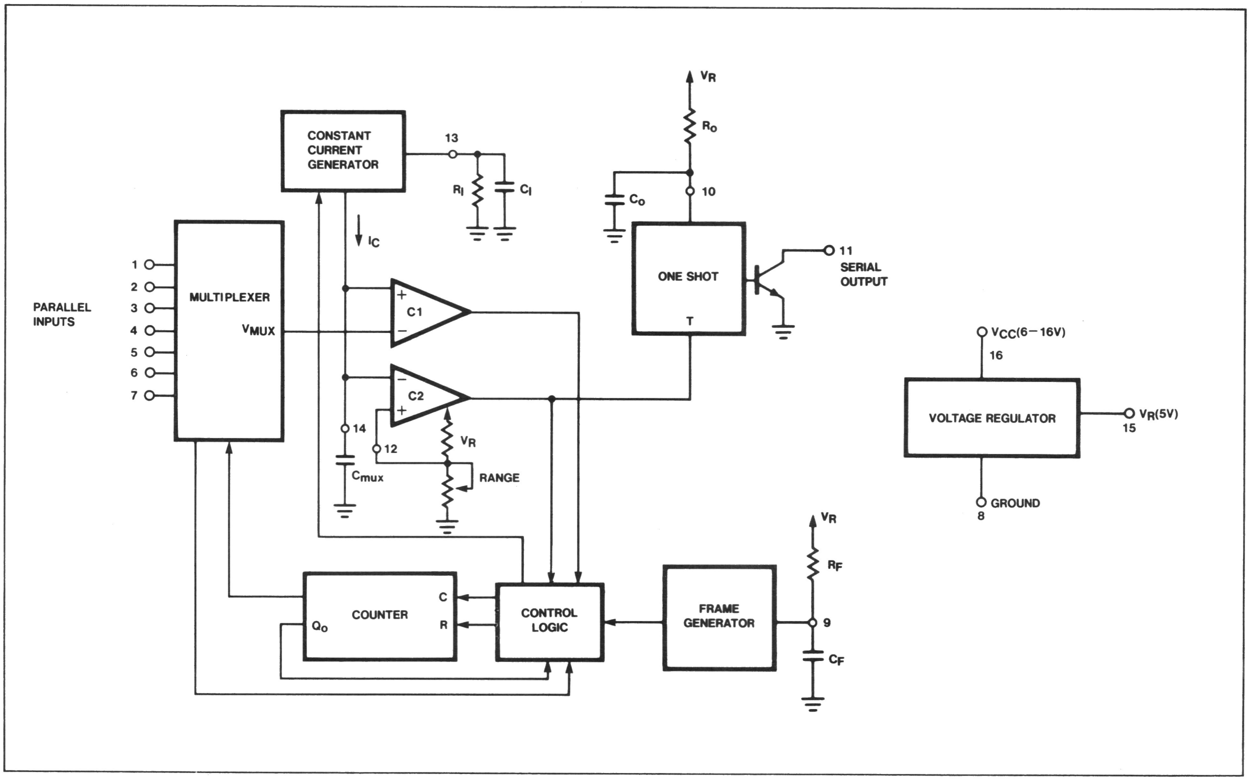

INPUT 1 1
INPUT 2 2
INPUT 3 3
INPUT 4 4
INPUT 5 5
INPUT 6 6
INPUT 7 7
GRND. 8
NE5044
16 V_{CC}
15 V REG
14 mpx CAP
13 SET RES.
12 RANGE
11 SER. OUT.
10 OUT R/C
9 FR. R/C

ORDER NE5044N
7 CHANNEL ENCODER

ELECTRICAL CHARACTERISTICS

PARAMETERS	LIMITS
Supply voltage range	6 -16V
Supply current	15mA
Input bias current	<200nA
Power supply rejection	0.01%/V
Pulsewidth tempco	0.01%/°C
Crosstalk	$<2\mu S$
Linearity error	$<2\mu S$
Output drive current	25mA
Regulator output voltage	5V
Regulator output current	25mA
Regulator voltage drop	1.2V
Operating temperature	−20 to +75°C
Storage temperature	−65 to +150°C

BLOCK DIAGRAM


V_R
R_O
CONSTANT CURRENT GENERATOR
13
R_I
C_I
C_O
10
I_C
PARALLEL INPUTS
1
2
3
4
5
6
7
MULTIPLEXER
V_{MUX}
C1
C2
14
12
C_{mux}
V_R
RANGE
ONE SHOT
T
11
SERIAL OUTPUT
V_{CC}(6−16V)
16
VOLTAGE REGULATOR
V_R(5V)
15
GROUND
8
COUNTER
Q_O
C
R
CONTROL LOGIC
FRAME GENERATOR
V_R
R_F
9
C_F

SEVEN CHANNEL RC DECODER — NE5045

OBJECTIVE SPECIFICATION
March 1979

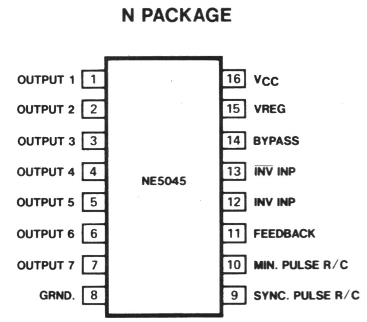
DESCRIPTION

The NE5045 is a serial input, parallel output, decoder intended for applications in pulse width or pulse position modulation systems. The serial input is amplified and shaped before being fed to the counter/decoder. An integrating type sync. separator detects pulses greater than $T_W = R_S C_S$ to reset the counter. An internal voltage regulator supplies power for the radio receiver providing excellent isolation from the power supply as well as the decoder logic.

FEATURES

- **Up to 7 channels**
- **High gain op amp input**
- **Sync separator time constant set externally, $T = R_S C_S$**
- **Voltage regulator for receiver**
- **Wide supply voltage range 3.6V to 8V**
- **Low power dissipation**
- **Minimum external components**
- **Positive or negative inputs**
- **Noise spike flutter rejection**
- **Outputs reset to zero without input**

PIN CONFIGURATION

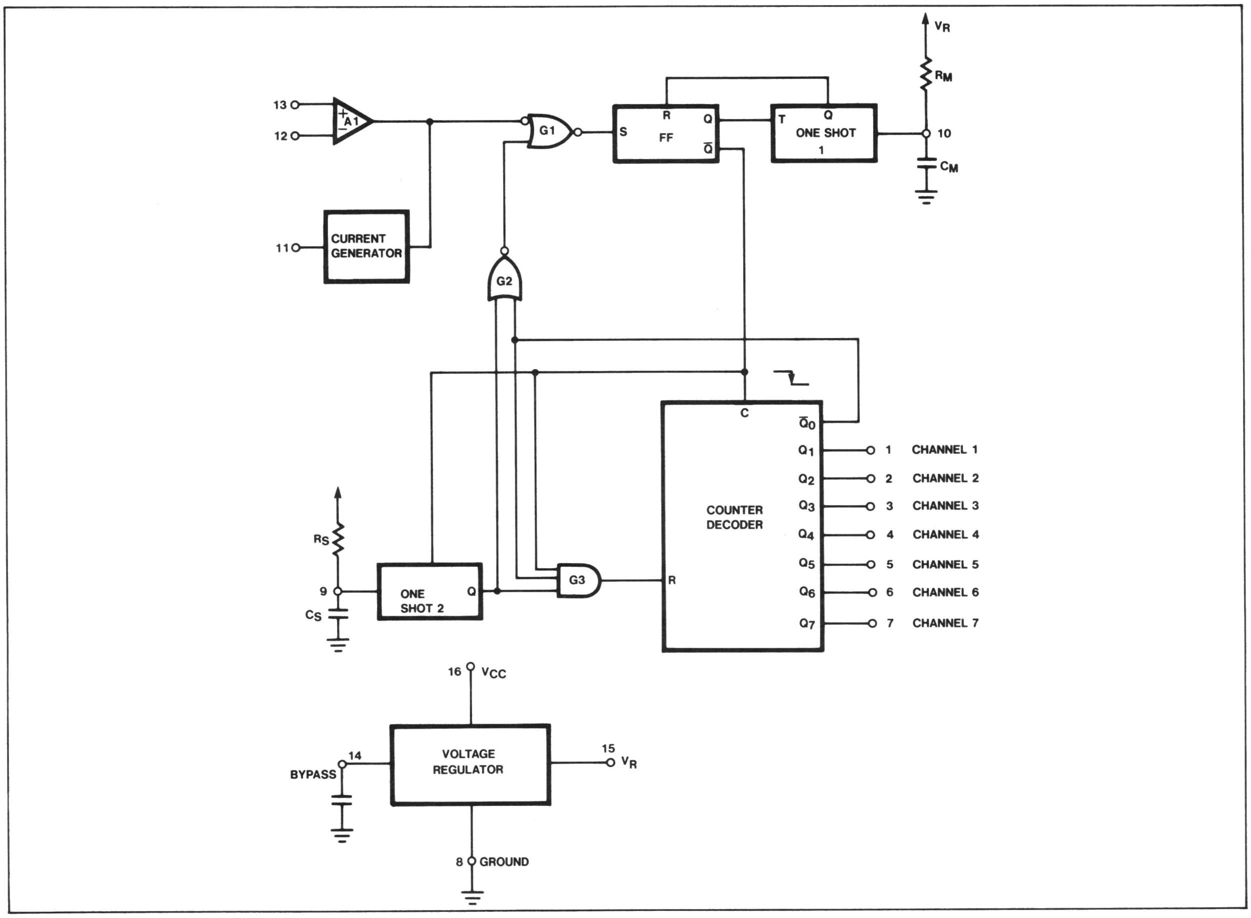

N PACKAGE
OUTPUT 1
1
OUTPUT 2
2
OUTPUT 3
3
OUTPUT 4
4
OUTPUT 5
5
OUTPUT 6
6
OUTPUT 7
7
GRND.
8
NE5045
16
V_{CC}
15
VREG
14
BYPASS
13
$\overline{INV}$ INP
12
INV INP
11
FEEDBACK
10
MIN. PULSE R/C
9
SYNC. PULSE R/C

ORDER NE5045N
7 CHANNEL DECODER

ELECTRICAL CHARACTERISTICS

PARAMÉTERS	LIMITS
Supply voltage range	3.6 −8V
Supply current	10mA
Regulator output voltage	4.1V ($V_{CC} > 5V$), V_{CC} −0.9V ($V_{CC} < 5V$)
Regulator output current	25mA
Output drive current	2mA

BLOCK DIAGRAM


13
12
A1
11
CURRENT GENERATOR
G1
S
R
FF
Q
$\overline{Q}$
T
Q
ONE SHOT 1
V_R
R_M
10
C_M
G2
C
$\overline{Q}_0$
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
COUNTER DECODER
R
1 CHANNEL 1
2 CHANNEL 2
3 CHANNEL 3
4 CHANNEL 4
5 CHANNEL 5
6 CHANNEL 6
7 CHANNEL 7
R_S
9
C_S
ONE SHOT 2
Q
G3
16
V_{CC}
14
BYPASS
VOLTAGE REGULATOR
15
V_R
8
GROUND

2 CHANNEL RC DECODER NE5046

OBJECTIVE SPECIFICATION
March 1979

DESCRIPTION

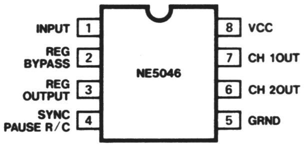
The NE5046 is a serial input parallel output decoder designed for 2 channel digital proportional pulse width or pulse position modulation systems. In a typical application, the serial input from the receiver is processed through an amplifier and pulse shaper and then converted to parallel output with a shift register. An internal sync separator detects the sync pause and clears the shift register.

FEATURES

- **High Gain input amplifier**
- **Minimum external components, low cost applications**
- **Space saving 8 pin mini dip package**
- **Low power consumption**
- **Adjustable sync separator timing**
- **Pulse shaper with hysteresis for high noise immunity**
- **Outputs reset to zero without input**

PIN CONFIGURATION

N PACKAGE



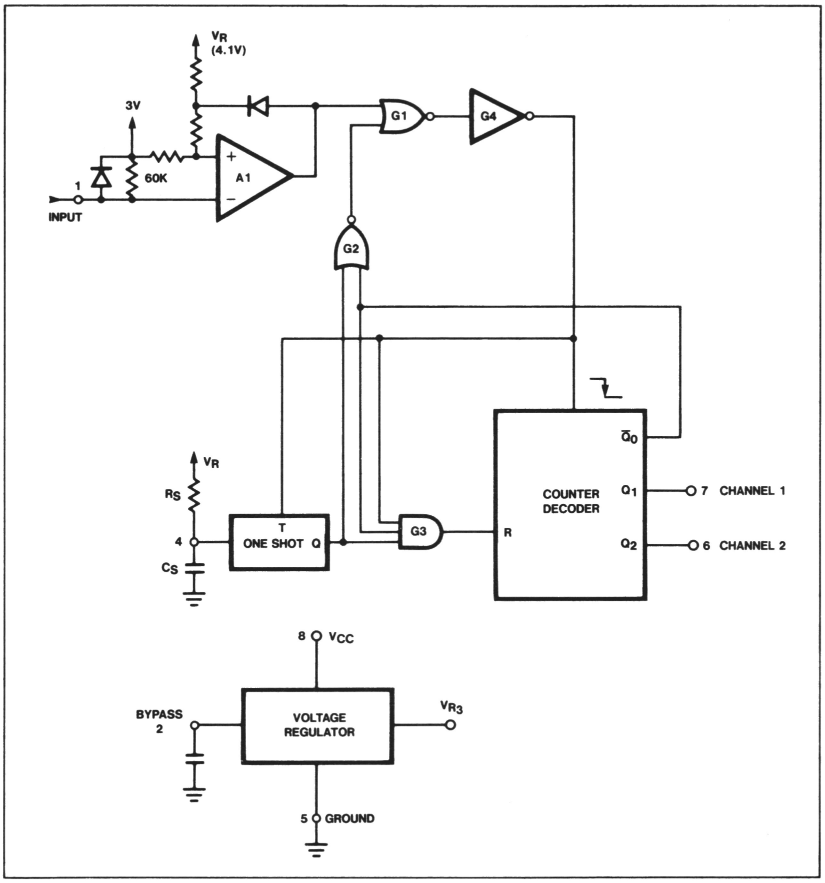
INPUT 1
REG BYPASS 2
REG OUTPUT 3
SYNC PAUSE R/C 4
NE5046
8 VCC
7 CH 1OUT
6 CH 2OUT
5 GRND

ORDER NE5046N
2 CHANNEL DECODER

ELECTRICAL CHARACTERISTICS

PARAMETERS	LIMITS
Supply voltage range	3.6 to 8 volt
Supply current	6mA
Input Impedance	>50kΩ
Output drive current	2mA
Regulator output voltage	4.1V ($V_{CC} > 5V$), V_{CC} −0.9V ($V_{CC} < 5V$)
Regulator output current	20mA

BLOCK DIAGRAM



VR (4.1V)
3V
60K
+
−
A1
1
INPUT
G1
G4
G2
G3
Q̄0
Q1
Q2
COUNTER DECODER
R
7 CHANNEL 1
6 CHANNEL 2
VR
RS
4
CS
T
ONE SHOT Q
8 VCC
BYPASS 2
VOLTAGE REGULATOR
VR3
5 GROUND

HIGH PERFORMANCE NE/SE 5512/5514

PRELIMINARY SPECIFICATION

N,FE,F,H

DESCRIPTION

The 5512/5514 series of high performance operational amplifier provides very good input characteristics coupled with single power supply operation. These amplifiers feature low input bias and voltage characteristics such as a 108 op amp with improved CMRR and a high differential input voltage limit achieved through the use of a bias cancellation and PNP input circuits with collector to emitter clamping. The output characteristics are like those of a 741 op amp with improved slew rate and drive capability yet have low supply quiescent current.

	5512	5514
Pin out	MC1458 TL072	LM324 TL074
Configuration	Dual	Quad

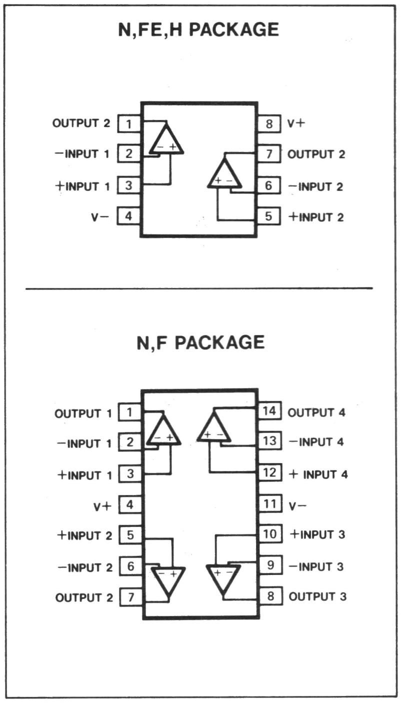
FEATURES

- **Low input bias $< \pm 1$nA**
- **Low input offset current $< \pm .5$nA**
- **Low input offset voltage $<$ 1mV**
- **Low V_{OS} temperature drift 3μV/°C**
- **Low input bias temperature drift 10pA/°C**
- **Low input current noise 0.1pA$\sqrt{\text{Hz}}$**
- **Low input voltage noise 10nV/$\sqrt{\text{Hz}}$**
- **Low supply current 1mA/amp**
- **High slew rate 1.2V/μs**
- **High CMRR 110dB**
- **High input impedance 100MΩ**
- **High common mode impedance 10GΩ**
- **High PSRR 110dB**
- **High differential input voltage limit**
- **No cross-over distortion**
- **Indefinite output short circuit protection**
- **Single supply operation**

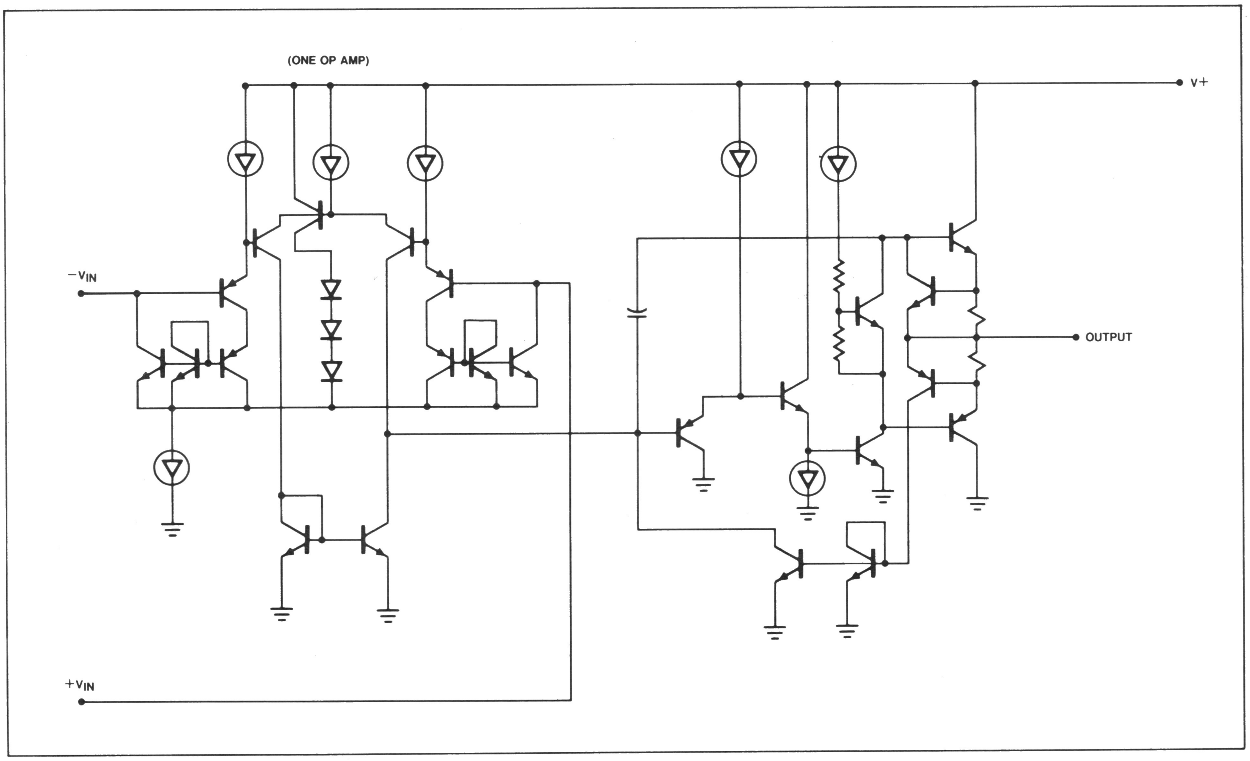
APPLICATIONS

- **AC amplifiers**
- **RC active filters**
- **Transducer amplifiers**
- **DC gain block**
- **5V dc power supply operation**
- **Battery operation**
- **Instrumentation application**
- **Low noise, low power audio PRE amps**

PIN CONFIGURATIONS


N,FE,H PACKAGE
OUTPUT 2 1
−INPUT 1 2
+INPUT 1 3
V− 4
8 V+
7 OUTPUT 2
6 −INPUT 2
5 +INPUT 2
N,F PACKAGE
OUTPUT 1 1
−INPUT 1 2
+INPUT 1 3
V+ 4
+INPUT 2 5
−INPUT 2 6
OUTPUT 2 7
14 OUTPUT 4
13 −INPUT 4
12 + INPUT 4
11 V−
10 +INPUT 3
9 −INPUT 3
8 OUTPUT 3

EQUIVALENT SCHEMATIC


(ONE OP AMP)
V+
−VIN
OUTPUT
+VIN

DESCRIPTION

The Signetics NE5539 is a very wide bandwidth, high slew rate, monolithic operational amplifier for use in video amplifiers, RF amplifiers, and extremely high slew rate amplifiers.

Emitter follower inputs provide a true differential high input impedance device. Proper external compensation will allow the designation to operate over a wide range of closed loop gains, both inverting and non-inverting, to meet specific design requirements.

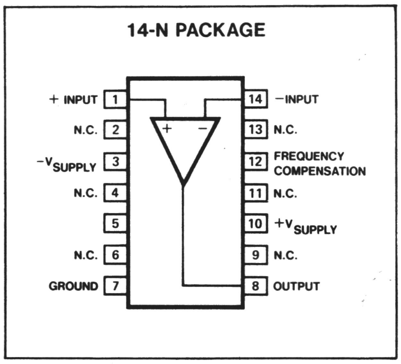
FEATURES

- **Gain bandwidth product: 1.2GHz**
- **Slew rate: 600V/μsec**
- **Full power response: 48MHz**
- **A_{VOL}: 50dB**

APPLICATIONS

- **Fast pulse amplifiers**
- **RF oscillators**
- **Fast sample and hold**
- **High gain video amplifiers (BW > 20MHz)**

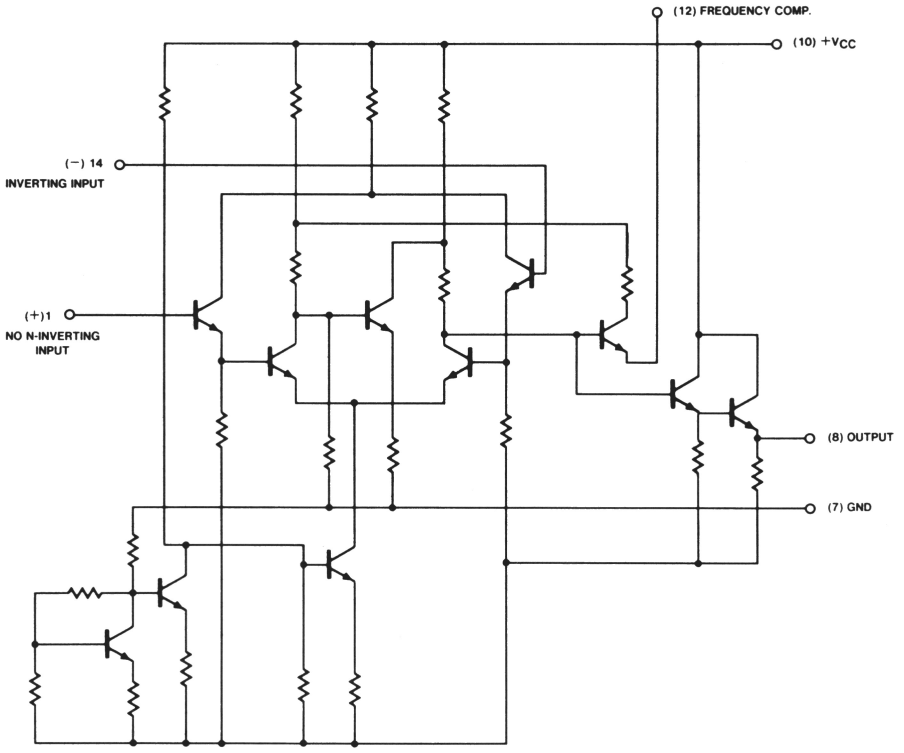
PIN CONFIGURATION


14-N PACKAGE
+ INPUT 1
N.C. 2
$-V_{SUPPLY}$ 3
N.C. 4
5
N.C. 6
GROUND 7
14 −INPUT
13 N.C.
12 FREQUENCY COMPENSATION
11 N.C.
10 $+V_{SUPPLY}$
9 N.C.
8 OUTPUT
+
−

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	±12	V
P_D	Internal power dissipation	550	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_J	Max junction temperature	150	°C
T_A	Operating temperature range	0 to +70	°C
	Lead temperature	300	°C

EQUIVALENT CIRCUIT


(12) FREQUENCY COMP.
(10) $+V_{CC}$
(−) 14
INVERTING INPUT
(+) 1
NO N-INVERTING INPUT
(8) OUTPUT
(7) GND

1-WATT TV/FM SOUND CHANNEL

ULN-2212

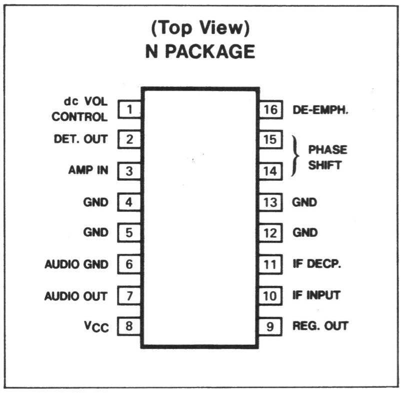
DESCRIPTION

Ideally suited for use in small-screen TV or mobile F-M radios, the ULN-2212B is a complete 1-watt sound channel. It operates from a single 14V supply and provides $V_{CC}/2$ output tracking as well as greater than 20dB of ripple rejection. This I.C. will directly drive an 8 or 16 ohm speaker. It has a true 1 watt output into the 8 ohm load.

FEATURES

- **Low limiting threshold**
- **Low external parts count**
- **High A-M rejection**
- **Single-adjustment tuning**
- **70dB limiter gain**
- **70dB DC volume control range**
- **Automatic thermal shutdown**
- **Output current limiting**
- **10V to 18V operating range**
- **>20dB ripple rejection**

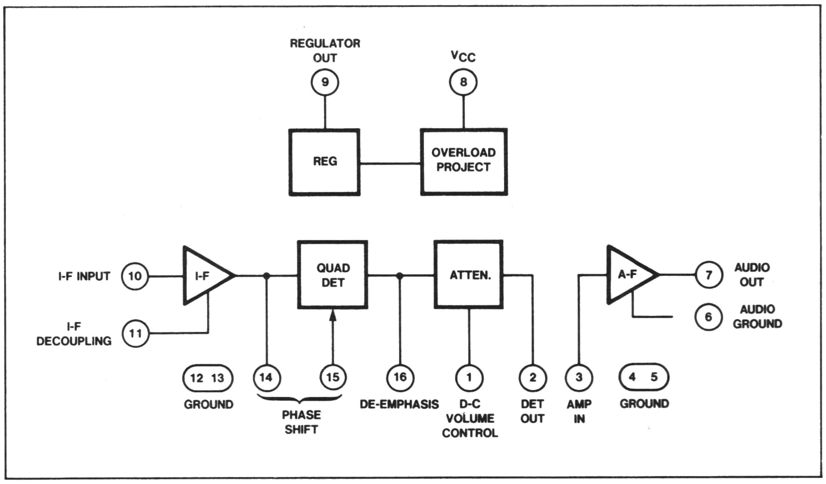
PIN CONFIGURATION


(Top View)
N PACKAGE
dc VOL CONTROL 1
DET. OUT 2
AMP IN 3
GND 4
GND 5
AUDIO GND 6
AUDIO OUT 7
VCC 8
16 DE-EMPH.
15
14
PHASE SHIFT
13 GND
12 GND
11 IF DECP.
10 IF INPUT
9 REG. OUT

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage, V_{CC}	+18	V
Regulator output current, I_{REG}	10	mA
Input voltage (pin 10), V_{IN}	+4.0	V
Operating temperature range, T_A	40°C to +85	°C
Storage temperature range, T_S	65° to +150	°C

BLOCK DIAGRAM


REGULATOR OUT
9
VCC
8
REG
OVERLOAD PROJECT
I-F INPUT
10
I-F
I-F DECOUPLING
11
QUAD DET
ATTEN.
A-F
7
AUDIO OUT
6
AUDIO GROUND
12 13
GROUND
14
15
PHASE SHIFT
16
DE-EMPHASIS
1
D-C VOLUME CONTROL
2
DET OUT
3
AMP IN
4 5
GROUND

μ255 PCM CODEC ST 100

DESCRIPTION

The Signetics ST100 is a monolithic μ255 law companded PCM Codec. This is a per channel device fabricated in I^2L technology. The ST100 has all the circuitry necessary to convert an analog signal into an 8 bit PCM digital data stream and vice versa. Asynchronous operation of transmit and receive is possible. A & B signaling and zero code suppression are also provided. Very few external components are required for its operation. The digital inputs are TTL compatible while the digital outputs are open collector, TTL compatible.

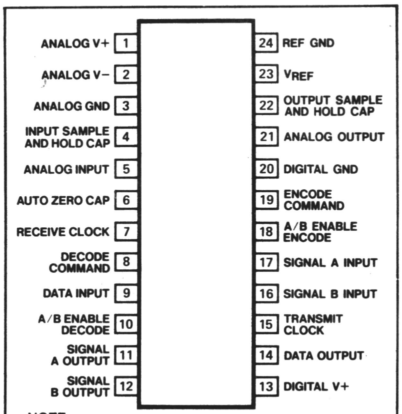
FEATURES

- **μ255 law companding**
- **Serial data rates up to 2.048MHz**
- **Sampling rates up to 16kHz**
- **Asynchronous operation of transmit and receive**
- **A & B dual channel signaling**
- **Zero code suppression**
- **Low noise**
- **Fabricated with proven, reliable bipolar process**
- **100% burned in**

APPLICATIONS

- **PCM channel banks**
- **EPABX's**
- **Subscriber loop carrier systems**
- **Central office switches**

PIN CONFIGURATION


ANALOG V+ 1
ANALOG V− 2
ANALOG GND 3
INPUT SAMPLE AND HOLD CAP 4
ANALOG INPUT 5
AUTO ZERO CAP 6
RECEIVE CLOCK 7
DECODE COMMAND 8
DATA INPUT 9
A/B ENABLE DECODE 10
SIGNAL A OUTPUT 11
SIGNAL B OUTPUT 12
24 REF GND
23 VREF
22 OUTPUT SAMPLE AND HOLD CAP
21 ANALOG OUTPUT
20 DIGITAL GND
19 ENCODE COMMAND
18 A/B ENABLE ENCODE
17 SIGNAL A INPUT
16 SIGNAL B INPUT
15 TRANSMIT CLOCK
14 DATA OUTPUT
13 DIGITAL V+

NOTE
Available in plastic, cer-dip and ceramic packages.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES T_A=0°C to 70°C
Plastic	ST100CN
Cer-dip	ST100CF
Ceramic	ST100CI

NOTE
For more information, contact your nearest Signetics sales office, representative, or franchised distributor.

BLOCK DIAGRAM

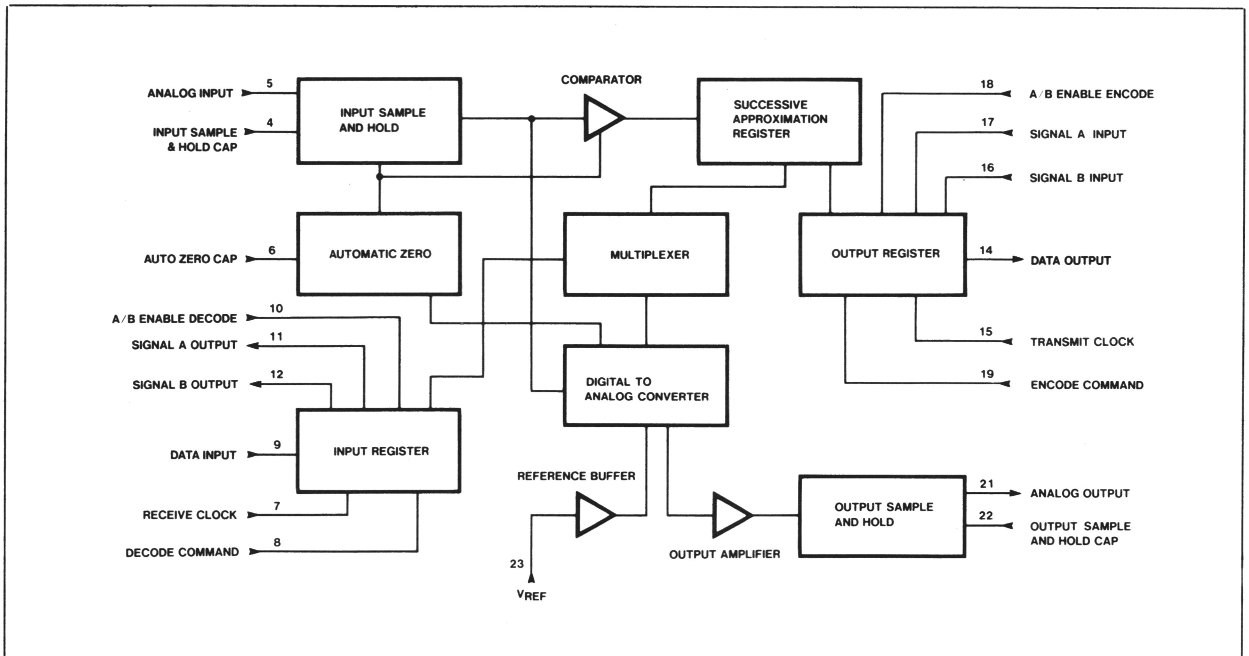

ANALOG INPUT 5
INPUT SAMPLE & HOLD CAP 4
INPUT SAMPLE AND HOLD
COMPARATOR
SUCCESSIVE APPROXIMATION REGISTER
18 A/B ENABLE ENCODE
17 SIGNAL A INPUT
16 SIGNAL B INPUT
AUTO ZERO CAP 6
AUTOMATIC ZERO
MULTIPLEXER
OUTPUT REGISTER
14 DATA OUTPUT
A/B ENABLE DECODE 10
SIGNAL A OUTPUT 11
SIGNAL B OUTPUT 12
DIGITAL TO ANALOG CONVERTER
15 TRANSMIT CLOCK
19 ENCODE COMMAND
DATA INPUT 9
INPUT REGISTER
REFERENCE BUFFER
OUTPUT SAMPLE AND HOLD
21 ANALOG OUTPUT
22 OUTPUT SAMPLE AND HOLD CAP
RECEIVE CLOCK 7
DECODE COMMAND 8
23 VREF
OUTPUT AMPLIFIER

Figure 1

D-MOS POWER FET SWITCH N-CHANNEL ENHANCEMENT SD224H

DESCRIPTION

The Signetics SD224 is a POWER MOSFET of the N-channel enhancement mode type designed for switching applications requiring high current, high speed, low "ON" resistance and excellent node-to-node isolation. Superior performance is achieved by utilizing the Signetics D-MOS process which provides high gain, low drain-to-source "ON" resistance, low inter-electrode capacitance and enhanced high frequency operation.

The SD224 is designed to switch analog signals up to ±7.5 volts. The device is hermetically sealed in a TO-12 package allowing each of the four electrodes to be biased independently.

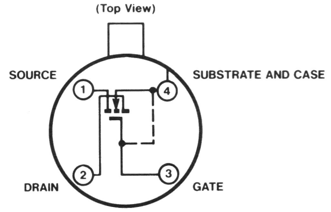
FEATURES

- **Low node capacitances**
- **Low feedthrough and feedback transients**
- **Excellent isolation input to output**
- **CMOS logic compatible input**
- **Extremely low drive power**
- **Switches 1A in less than 5ns**

APPLICATIONS

- **Switch driver**
- **Analog switch**
- **Digital switch**
- **Sample and hold**
- **Multiplexers**
- **A/D converters**
- **D/A converters**

PIN CONFIGURATION



ORDER PART NO
SD224H

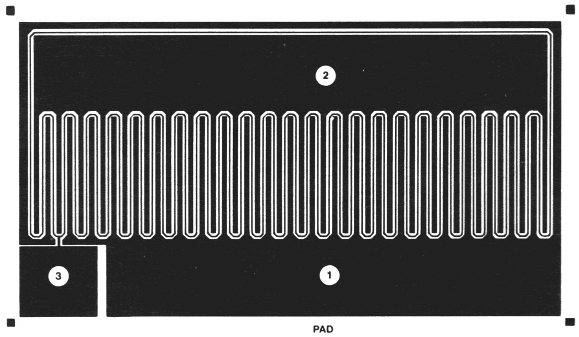
ABSOLUTE MAXIMUM RATINGS[1] $T_A = +25°C$ unless otherwise specified

PARAMETER		RATING	UNIT
V_{DS}	Drain-to-source	+25	V
V_{SD}	Source-to-drain[2]	+15	V
V_{DB}	Drain-to-body	−0.3, +20	V
V_{SB}	Source-to-body	−0.3, +20	V
V_{GS}	Gate-to-source	±30	V
V_{GD}	Gate-to-drain	±30	V
V_{GB}	Gate-to-body	±30	V
I_D (ON)	Continuous drain current	2	A
I_D(ON)	Pulsed drain current	3	A
P_D	Power dissipation		
	$T_A = +25°C$[3]	1	W
	$T_C = +25°C$[4]	5	W
	Power derating factors		
	Free air	8	mW/°C
	Infinite heat sink	40	mW/°C
Θ_{JA}	Thermal resistance	125	°C/W
Θ_{JC}	Thermal resistance	25	°C/W
T_{op}	Operating temperature	−55 to +125	°C
T_{stg}	Storage temperature	−55 to +150	°C

NOTES

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. See test conditions in dc electrical characteristics section.
3. Free air.
4. Infinite heat sink.

CHIP DIAGRAM



PAD NO.	PAD FUNCTION
1	SOURCE
2	DRAIN
3	GATE

SECTION 17
APPENDICES

MILITARY

MILITARY PRODUCTS/ PROCESS LEVELS

The Signetics MIL 38510/883 Program is organized to provide a broad selection of processing options, structured around the most commonly requested customer flows. The program is designed to provide our customers:

- Fully compliant 883 flows on all products.
- Standard processing flows to help minimize the need for custom specs.
- Cost savings realized by using standard processing flows in lieu of custom flows.
- Better delivery lead times by minimizing spec negotiation time, plus allows customer to buy product off-the-shelf or in various stages of production rather than waiting for devices started specifically to custom specs.

The following explains the different processing options available to you. Special device marking clearly distinguishes the type of screening performed. Refer to Tables 2, 3, 4 and 5.

JAN CASE OUTLINE AND LEAD FINISH	SIGNETICS MILITARY PACKAGE TYPES				
			DUAL-IN-LINE		
	8-PIN	10-PIN	14-PIN	16-PIN	24-PIN
CB	—	—	F	—	—
EB	—	—	—	F	—
JB	—	—	—	—	F
DB	—	—	W	—	—
FB	—	—	—	W	—
ZC	—	—	—	—	Q
GC	T	—	—	—	—
IC	—	K	—	—	—

All products listed are also available in Die form.

Table 1 MILITARY PACKAGE AVAILABILITY

	JB	RB	RC
	Jan Qualified	883B	883C
54/54H	X	X	X
54LS	X	X	X
54S	X	X	X
82/8T	X	X	X
93XX	X	X	X
96XX	—	X	X
Linear	X	X	X
Bipolar Memory	X	X	X
Microprocessor	—	X	X

Table 2 MILITARY SUMMARY

JAN QUALIFIED (JB)

JAN Qualified product is designed to give you the optimum in quality and reliability. The JAN processing level is offered as the result of the government's product standardization programs, and is monitored by the Defense Electronic Supply Center (DESC), through the use of industry-wide procedures and specifications.

JAN Qualified products are manufactured, processed and tested in a government certified facility to Mil-M 38510, and appropriate device slash sheet specifications. Design documentation, lot sampling plans, electrical test data and qualification data for each specific part type has been approved by the Defense Electronic Supply Center (DESC) and products appear on the DESC Qualified Products List (QPL-38510).

Group B testing, per Mil-Std-883 Method 5005, is performed on each six weeks of production on each slash sheet for each package type. Group C, per Mil-Std-883 Method 5005, is performed every ninety days for each microcircuit group. Group D testing, per Mil-Std-883 Method 5005, is performed every six months for each package type.

In addition to the common specs used throughout the industry for processing and testing, JAN Qualified products also possess a requirement for a standard marking used throughout the IC industry.

MIL-STD-883, LEVEL B

Processing to this option is ideal when no JAN slash sheets are released on devices required. Product is processed to Mil-Std-883 Method 5004, and is 100% electrically tested to industry data sheets. Devices are selectively available as custom processed parts with electricals screened to the JAN Slash Sheets.

MIL-STD-883, LEVEL C

If you need a Military temp, range device, but do not require burn in screening performed, our 883C product is ideal. 883C parts are the standard full Mil-Temperature range product to the Signetics data sheet parameters and screened to MIL-STD-883, Class C.

MILITARY GENERIC DATA

Signetics has a new program for those customers who require quality conformance data on their products. This program allows our customers to obtain reliability information without the necessity or running Groups B, C and D inspections for their particular purchase order. It provides for the customer something that has not been readily available before in the semiconductor industry in that all Military Generic Data is controlled and audited by both Government Inspection in the case of JAN data and Signetics Quality Assurance.

Signetics Military Generic Data is compiled by the Military Products Division based on data from 1) JAN quality conformance lots, and 2) Data generated by quality conformance lots run for other reliability programs. Refer to Table 4.

A Military Generic family is defined as consisting of die function and package type families.

Military Generic Data

- Allows our customers to qualify Signetics products based on existing quality conformance data performed at Signetics.
- Allows our customers to reduce costs and improve deliveries.
- Provides assurance that all Signetics die function families and packages meet Mil-M-38510 and customer reliability requirements.
- Provides an attributes summary to the customer backed by lot identity and traceability.

PROCESS LEVEL AND MARKETING	PRE-CAP VISUAL	BURN IN	FUNCTIONAL TEST	DC/AC @25°C	DC/AC @TEMP	QPL	OFFSHORE
JB JM38510XXXXX	2010, Cond. B	Yes	100%	100%	100%	Yes	No
RB SXXXX883B	2010, Cond.B	Yes	100%	100%	100%	No	Yes
RC SXXXX883C	2010, Cond. B	No	100%	100% dc Sample ac	Sample dc only	No	Yes

Table 3 MILITARY PRODUCTS PROCESSING MATRIX

QUALIFIED SUB-GROUPS	QUALIFIES	OPTION 1	OPTION 2
A*	Electrical Test		
B	Package—Same package construction and lead finish.	Data selected from devices manufactured within 6 weeks of the manufacturing period on the same production line through final seal.	Data selected from devices manufactured within 24 weeks of manufacturing period.
C	Die/Process—Devices representing the same process families.	Data selected from representative devices from the same microcircuit group and sealed within 12 weeks of the manufacturing period.	Data selected from the representative devices from the same microcircuit group and sealed within 48 weeks of the manufacturing period.
D	Package—Same package construction and lead finish.	Data selected from the devices representing the same package construction and lead finish manufactured within the 24 weeks of manufacturing period. If specific data not available, Option 2 will be supplied	Data selected from the devices representing the same package construction and lead finish manufactured within the 52 weeks of manufacturing period.

NOTE*
Group A is performed on each lot or sublot of Signetics devices.

Table 4 DEFINITION AND QUALIFYING MANUFACTURING PERIODS FOR GENERIC DATA

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 AND MIL-STD-883 REQUIREMENTS, METHDS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS			
			CLASS S	JAN QUALIFIED (JB)	883B (RB)	883C (RC)
General Mil-M-38510 1. Pre-Certification A. Product Assurance Program Plan B. Manufacturer's Certification	The Manufacturer shall establish and implement a Products Assurance Program Plan and provide for a manufacturer survey by the qualifying activity, Para. 3.4.1.1	—	X	X	N/A	N/A
2. Certification	Received after manufacturer has completed a successful survey, Para. 3.4.1.2	—	X	X	N/A	N/A
3. Device Qualification	Device qualification shall consist of subjecting the desired device to groups A, B, C & D of method 5005 to tightened LTPD, Para. 3.4.1.2	—	X	X	N/A	N/A
4. Traceability	Traceability maintained back to a production lot Para. 3.4.6	—	X	X	X	X
5. Country of Origin	Devices must be manufactured, assembled, and tested within the U.S. or its territories, Para. 3.2.1	—	X	X	N/A	N/A
Screening Per Method 5004 of Mil-Std-883						
6. Internal Visual (Precap)	2010, Cond. A or B	100%	XA	XB	XB	XB
7. Stabilization Bake	1008, Cond. C Min; (24 Hrs @ 150°C)	100%	X	X	X	X
8. Temperature Cycling* *For Class B and C devices thermal shock may be substituted, 1011, Cond. A; (15 cycles, 0° to +100°C)	1010, Cond. C; (10 cycles, −65°C to +150°C)	100%	X	X	X	X
9. Constant Acceleration	2001, Cond. E; (30kg in YI Plane)	100%	X	X	X	X
10. Visual Inspection	There is no test method for this screen; it is intended only for the removal of "Catastrophic Failures" defined as "Missing Leads, Broken Packages or Lids Off."	100%	X	X	X	X
11. Seal (Hermeticity)	1014					
A. Fine	Cond. A or B (5.0 X 10^{-8}CC/Sec)	100%	X	X	X	X
B. Gross	Cond. C2 Min.	100%	X	X	X	X
12. Interim Electricals (Pre Burn-In)	Per applicable device specification	100% Optional	100% Read & Record	Slash Sheet	Data Sheet	N/A
13. Burn-In	1015, Cond. as specified (160 hrs. Min. at 125°C)	100%	100% 240 hrs.	X	X	N/A
14. Final Electricals	Per applicable Device Specification	100%	100% Read & Record	Slash Sheet	Data Sheet	Data Sheet
A. Static Tests @ 25°C	Sub Group 1		X	X	X	X
B. Static Tests @ +125°C	Sub Group 2		X	X	X	N/A
C. Static Tests @ −55°C	Sub Group 3		X	X	X	N/A

Table 5 REQUIREMENTS AND SCREENING FLOWS FOR STANDARD PRODUCTS

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 AND MIL-STD-883 REQUIREMENTS, METHODS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS			
			CLASS S	JAN QUALIFIED (JB)	883B (RB)	883C (RC)
D. Dynamic Test @25°C	Sub Group 4 (for Linear Product Mainly)		X	X	X	X
E. Functional Test @25°C	Sub Group 7		X	X	X	X
F. Switching Test @25°C	Sub Group 9		X	X	X	N/A
15. Percent Defective allowable (PDA)	**A PDA of 10% is a normal requirement applied against the static tests @25°C (A-1). This is controlled by the slash sheets for JB products. For RB 10% is standard**	10%	10% 3% Funct"l	X	X	N/A
16. Marking	Fungus Inhibiting Paint	100%	As Req'd	JM38510/ XXXX Slash Sheet #	S X X X X 883B	SXXXX 883C
17. X-Ray	2012		100%	N/A	N/A	N/A
18. External Visual	2009	100%	X	X	X	X
Quality Conformance Inspection per Method 5005 of Mil-Std 883						
19. Group A	Electrical Tests-Final Electricals (#14 above) repeated on a sample basis. (Sub Groups 1 thru 12 as specified.)	Each Lot	X	X	X	X
20. Group B	Package functional and constructional related test I.E. package dimensions, resistance to solvents, internal visual & mechanical, bond strength & solderability.	**Every 6 week per pkg. group**	X	X	Generic Data Available	
21. Group C	Die related tests I.E. 1,000 hr. operating life, temperature cycling, & constand acceleration.	**Every 3 months per μcircuit type**	X	X	Generic Data Available	
22. Group D	Package related tests I.E. physical dimensions, lead fatigue, thermal shock, temperature cycle, moisture resistance, mechanical shock, vibration variable frequency constant acceleration, & salt atmosphere.	**Every 6 months per package type**	X	X	Generic Data Available	

Table 5 REQUIREMENTS AND SCREENING FLOWS FOR STANDARD PRODUCTS (Cont'd)

LINEAR DEVICES

DEVICE	DESCRIPTION	PACKAGE*	
		DIP	CAN
	OPERATIONAL AMPLIFIERS		
LF155/A	JFET Op Amp		H
LF156/A	JFET Op Amp		H
LF157/A	JFET Op Amp		H
LH2101A	Dual Op Amp	F	
LM101/A	Hi Perf Op Amp	F	H
LM107	Gen Purp Op Amp	F	H
LM108/A	Precision Op Amp	F	H
LM124	Quad Op Amp	F	
LM158	Dual Op Amp		H
MC1556	Hi Perf Op Amp	F	H
MC1558	Dual Op Amp	F	H
SE530	Hi Slew Op Amp	F	H
SE532	Dual Op Amp		H
SE535	Hi Slew Op Amp	F	H
SE538	Hi Slew Op Amp	F	H
SE5530	Dual Op Amp	F	H
SE5534	Lo Noise Op Amp	F	H
SE5535	Dual Op Amp	F	H
SE5538	Dual Op Amp	F	H
µA709/A	Gen Purp Op Amp	F	H
µA741	Gen Purp Op Amp	F	H
µA747	Dual Op Amp	F	H
µA748	Gen Purp Op Amp	F	H
	COMPARATORS		
SE521	Dual Differential Comparator	F	
SE522	Dual Differential Comparator	F	
SE527	Voltage Comparator	F	H
SE529	Voltage Comparator	F	H
LH2111	Dual Voltage Comparator	F	
LM111	Voltage Comparator	F	H
LM139/A	Quad Voltage Comparator	F	
LM193/A	Dual Voltage Comparator		H
µA710	Voltage Comparator	F	H
µA711	Dual Voltage Comparator	F	H
	DIFFERENTIAL AMPLIFIERS		
SE510	Dual Differential Amplifier	F	
SE511	Dual Differential Amplifier	F	
SE515	Differential Amplifier	F	H
SE592	Video Amplifier	F	H
µA733	Video Amplifier	F	H
	PHASE LOCKED LOOPS		
SE567	Tone Decoder PLL	F	H
SE564*	Phase Locked Loop	F	H
	TIMERS		
SE555	Timer	F,FE	H
SE556	Dual Timer	F	
SE558	Quad Timer	F	
SE559	Quad Timer	F	

DEVICE	DESCRIPTION	PACKAGE*	
		DIP/ CAN	CAN
	VOLTAGE REGULATORS		
SE5551	Dual Track Reg	F	H
SE5552	Dual Track Reg	F	H
SE5553	Dual Track Reg	F	H
SE5554	Dual Track Reg	F	H
SE5555	Dual Track Reg	F	H
78HV(8)	3 Term Pos Reg	K	—
78MHV(8)	3 Term Pos Reg	—	H
790X(8)	3 Term Neg Reg	K	—
79MOX(8)	3 Term Neg Reg	—	H
µA723	Adj Volt Reg	F	H

DEVICE	DESCRIPTION	PACKAGE	
		DIP	CAN
	D to A CONVERTERS		
SE5008	8-Bit Mult DAC	F	—
SE5009	8-Bit Mult DAC	F	—
SE5018	8-Bit µP-Comp DAC	F	—
SE5019	8-Bit µP-Comp DAC	F	—

JAN – 38510		
DEVICE	QPL I	QPL II
SE555F	1979	10901BCB
SE555FE	1979	10901BPB
SE555H	1979	10901BGC
SE556F	1979	10902BCB
LH2101AF	1979	10105BEB
LM101AF	10103BCB	—
LM101AFE	1979	10103BPB
LM101AH	1979	—
µA741H	1979	—
µA747H	1979	—
LM111F	—	1979
LM111H	1979	—
LM124F	—	1979
LM139F	—	1979

NOTES
F = Cerdip, K = TO-3
H = TO-5

PACKAGES

INTRODUCTION

The following information applies to all packages unless otherwise specified on individual package outline drawings.

General

1. Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).
2. Lead spacing shall be measured within this zone.
    a. Shoulder and lead tip dimensions are to centerline of leads.
3. Tolerances non-cumulative
4. Thermal resistance values are determined by utilizing the linear temperature dependence of the forward voltage drop across the substrate diode in a digital device to monitor the junction temperature rise during known power application across V_{CC} and ground. The values are based upon 120 mils square die for plastic packages and a 90 mils square die in the smallest available cavity for hermetic packages. All units were solder mounted to P.C. boards, with standard stand-off, for measurement.

Plastic Only

5. Lead material: Alloy 42 or equivalent, solder dipped.
6. Body material: Plastic
7. Round hole in top corner denotes lead No. 1.
8. Body dimensions do not include molding flash.

Hermetic Only

9. Lead material
    a. Alloy 52—gold plated, or solder dipped.
    b. ASTM alloy F-15 (KOVAR) or equivalent—gold plated, tin plated, or solder dipped.
    c. ASTM alloy F-30 (Alloy 42) or equivalent—tin plated.
    d. ASTM alloy F-15 (KOVAR) or equivalent—gold plated.
    e. ASTM alloy F-15 (KOVAR) or equivalent—tin plated.
10. Body Material
    a. 1010 Steel—nickel plated or tin plate over nickel.
    b. Eyelet, ASTM alloy F-15 or equivalent—gold or tin plated.
    c. Eyelet, ASTM alloy F-15 or equivalent—gold or tin plated, glass body.
    d. Ceramic with glass seal at leads.
    e. BeO ceramic with glass seal at leads.
    f. Ceramic with ASTM alloy F-15 or equivalent.
11. Lid Material
    a. 1010 steel, nickel plated, or tin-plate over nickel, weld seal.
    b. Nickel or tin plated nickel, weld seal.
    c. Ceramic, glass seal.
    d. ASTM alloy F-15 or equivalent, gold plated.
    e. BeO Ceramic with glass seal.
    f. Translucent Al_2O_3, glass seal.
12. Signetics symbol, angle cut, or lead tab denotes Lead No. 1.
13. Recommended minimum offset before lead bend.
14. Maximum glass climb .010 inches.
15. Maximum glass climb or lid skew is .010 inches.
16. Typical four places.
17. Dimension also applies to seating plane.

PLASTIC PACKAGES

NO. OF LEADS	PACKAGE CODE	Θ_{ja}/Θ_{jc}(°C/W)	DESCRIPTION[1]
Standard Dual-In-Line			
8	NE	162/65	
14	NH	150/65	TO-116/MO-001
16	NJ	137/53	MO-001
18	NK	135/53	
20	NL	135/53	
22	NM	120/53	
24	NN	116/53	MO-015
24	NNE	TBD	
28	NQ	116/53	MO-015
40	NW	110/50	MO-015
Power Dual-In-Line			
8	NEA[2]	180/80	Heatsink
14	NHA[2]	95/33	Heatsink
16	NJA[2]	95/33	Heatsink
18	NKA[2]	90/26	Heatsink
20	NLA[2]	90/26	Heatsink
22	NMA[2]	80/40	Heatsink
24	NNA[2]	60/23	Heatsink
28	NQA[2]	56/21	Heatsink
40	NWA[2]	45/18	Heatsink
Power			
3	S	200/70	TO-92
3	UCA	75/3	TO-220
3 + GND	UC	95/15	Single-in-Line (SIL)
4 + GND	UD	95/15	Single-in-Line (SIL)
5 + GND	UEA	TBD	TO-220
7 + GND	UGA	TBD	TO-220
12 + GND	PH/PHA	95/15	Batwing

HERMETIC PACKAGES

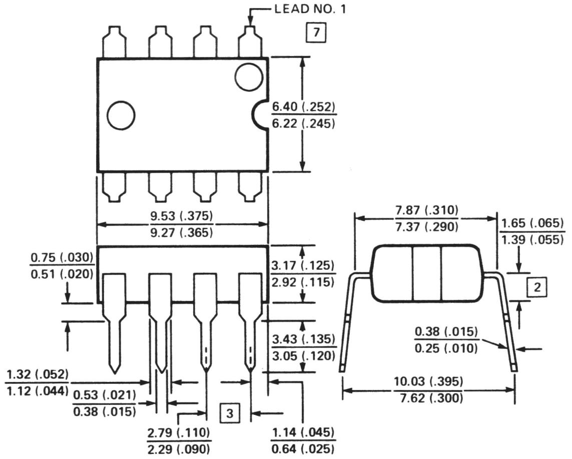
NO. OF LEADS	PACKAGE CODE	Θ_{ja}/Θ_{jc}(°C/W)	DESCRIPTION[1]
Metal Headers			
2	K	TBD	TO-3 Solid Header
3	HBA	TBD	TO-39 Solid Header, Short Can
4	DC	TBD	TO-72 Solid Header
4	DE	TBD	TO-72 Glass Filled Header
4	HCA	TBD	TO-12 Glass Filled Header, Short Can
8	HEA	150/45	TO-99 Header (.200 Dia.)
10	HFA	150/45	TO-100 Header, Short Can
10	HFC	150/45	TO-100 Header, Tall Can
Flat Packs			
10	WF	240/50	Flat Ceramic
14	WH	205/50	Flat Ceramic
16	WJ	200/50	Flat Ceramic
24	WN	155/40	Flat Ceramic
16	RJA	145/26	Flat Ceramic, BeO
18	RKA	107/22	Flat Ceramic, BeO
24	RNA	96/22	Flat Ceramic, BeO
28	RQA	92/22	Flat Ceramic, BeO
40	RWA	77/20	Flat Ceramic, BeO
10	QFA	230/55	Flat Ceramic Laminate
14	QHA	185/45	Flat Ceramic Laminate
16	QJA	170/45	Flat Ceramic Laminate
24	QNA	155/44	Flat Ceramic Laminate
Cerdip Family			
8	FE	140/32	Dual-in-Line Ceramic
14	FH	110/30	Dual-in-Line Ceramic
16	FJ	100/30	Dual-in-Line Ceramic
18	FK	93/27	Dual-in-Line Ceramic
20	FL	88/27	Dual-in-Line Ceramic
22	FM	75/27	Dual-in-Line Ceramic
24	FN	60/26	Dual-in-Line Ceramic
28	FQ	55/26	Dual-in-Line Ceramic
Laminated Ceramic, Side Brazed Lead			
8	IEA	100/30	Dip Laminate
14	IHA	95/25	Dip Laminate
16	IJA	90/25	Dip Laminate
18	IKA	88/25	Dip Laminate
22	IMA	80/25	Dip Laminate
24	INC	65/25	Dip Laminate
28	IQA	60/25	Dip Laminate
40	IWA	55/25	Dip Laminate
48	JY	TBD	Leadless Dip Laminate
50	IZA	42/20	Dip Laminate

NOTES

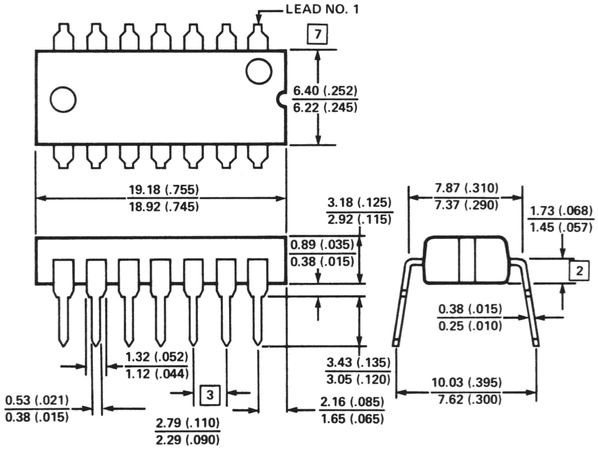
1. Dual-in-Line packages unless otherwise described.
2. Package outline is the same as corresponding standard Dual-in-Line package with identical number of leads.

PLASTIC: Standard and Power Dual-In-Line

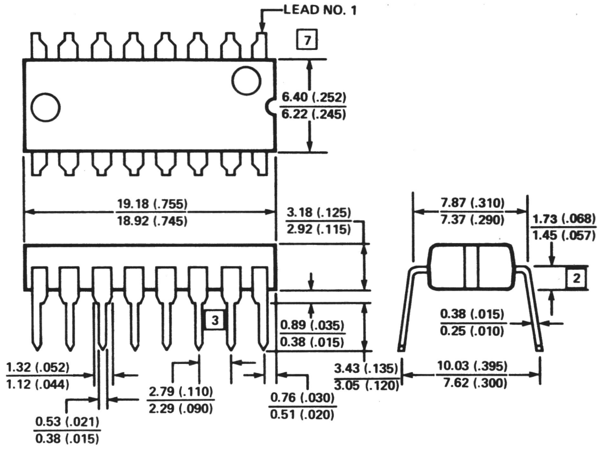
NE Package and NEA Package


LEAD NO. 1
7
6.40 (.252)
6.22 (.245)
9.53 (.375)
9.27 (.365)
0.75 (.030)
0.51 (.020)
3.17 (.125)
2.92 (.115)
3.43 (.135)
3.05 (.120)
1.32 (.052)
1.12 (.044)
0.53 (.021)
0.38 (.015)
3
2.79 (.110)
2.29 (.090)
1.14 (.045)
0.64 (.025)
7.87 (.310)
7.37 (.290)
1.65 (.065)
1.39 (.055)
2
0.38 (.015)
0.25 (.010)
10.03 (.395)
7.62 (.300)

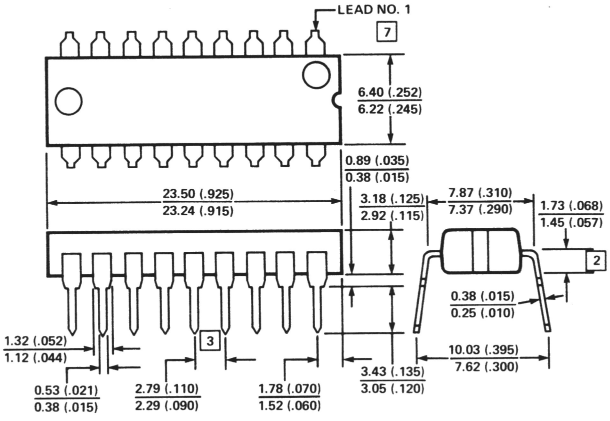
NH Package and NHA Package


LEAD NO. 1
7
6.40 (.252)
6.22 (.245)
19.18 (.755)
18.92 (.745)
3.18 (.125)
2.92 (.115)
0.89 (.035)
0.38 (.015)
7.87 (.310)
7.37 (.290)
1.73 (.068)
1.45 (.057)
2
0.38 (.015)
0.25 (.010)
1.32 (.052)
1.12 (.044)
3.43 (.135)
3.05 (.120)
10.03 (.395)
7.62 (.300)
0.53 (.021)
0.38 (.015)
3
2.79 (.110)
2.29 (.090)
2.16 (.085)
1.65 (.065)

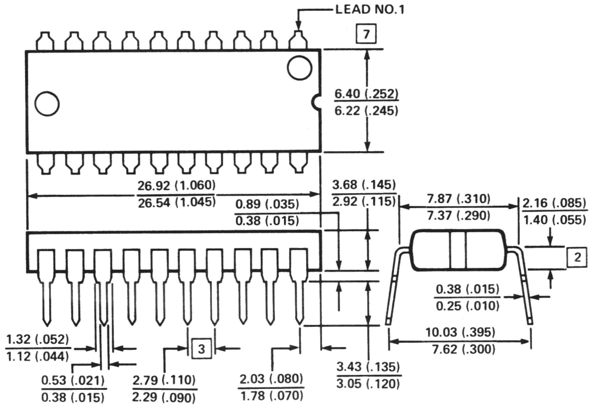
NJ Package and NJA Package


LEAD NO. 1
7
6.40 (.252)
6.22 (.245)
19.18 (.755)
18.92 (.745)
3.18 (.125)
2.92 (.115)
7.87 (.310)
7.37 (.290)
1.73 (.068)
1.45 (.057)
2
3
0.89 (.035)
0.38 (.015)
0.38 (.015)
0.25 (.010)
1.32 (.052)
1.12 (.044)
2.79 (.110)
2.29 (.090)
3.43 (.135)
3.05 (.120)
10.03 (.395)
7.62 (.300)
0.76 (.030)
0.51 (.020)
0.53 (.021)
0.38 (.015)

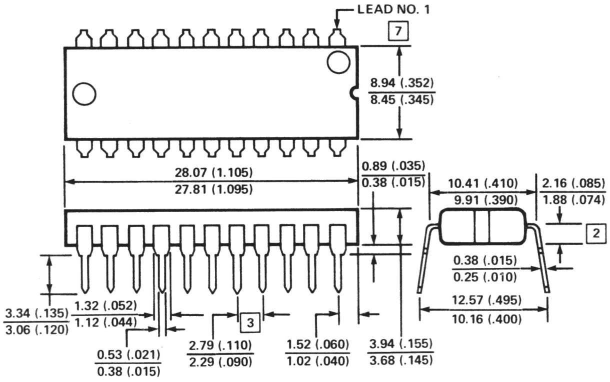
NK Package and NKA Package


LEAD NO. 1
7
6.40 (.252)
6.22 (.245)
0.89 (.035)
0.38 (.015)
23.50 (.925)
23.24 (.915)
3.18 (.125)
2.92 (.115)
7.87 (.310)
7.37 (.290)
1.73 (.068)
1.45 (.057)
2
0.38 (.015)
0.25 (.010)
1.32 (.052)
1.12 (.044)
3
10.03 (.395)
7.62 (.300)
3.43 (.135)
3.05 (.120)
0.53 (.021)
0.38 (.015)
2.79 (.110)
2.29 (.090)
1.78 (.070)
1.52 (.060)

NL Package and NLA Package

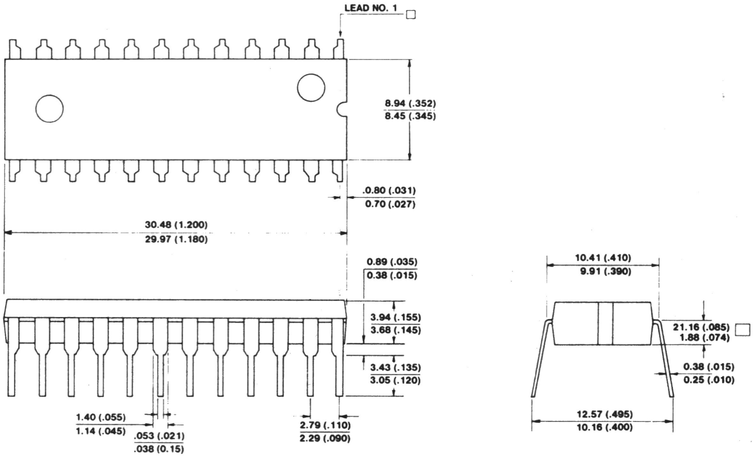

LEAD NO.1
7
6.40 (.252)
6.22 (.245)
26.92 (1.060)
26.54 (1.045)
0.89 (.035)
0.38 (.015)
3.68 (.145)
2.92 (.115)
7.87 (.310)
7.37 (.290)
2.16 (.085)
1.40 (.055)
2
0.38 (.015)
0.25 (.010)
10.03 (.395)
7.62 (.300)
1.32 (.052)
1.12 (.044)
3
0.53 (.021)
0.38 (.015)
2.79 (.110)
2.29 (.090)
2.03 (.080)
1.78 (.070)
3.43 (.135)
3.05 (.120)

NM Package and NMA Package

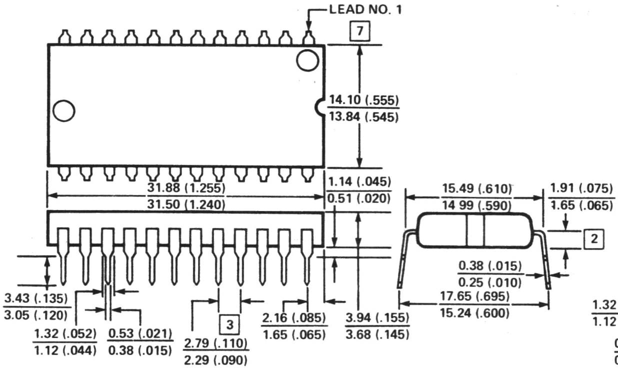

LEAD NO. 1
7
8.94 (.352)
8.45 (.345)
0.89 (.035)
0.38 (.015)
28.07 (1.105)
27.81 (1.095)
10.41 (.410)
9.91 (.390)
2.16 (.085)
1.88 (.074)
2
0.38 (.015)
0.25 (.010)
12.57 (.495)
10.16 (.400)
3.34 (.135)
3.06 (.120)
1.32 (.052)
1.12 (.044)
3
0.53 (.021)
0.38 (.015)
2.79 (.110)
2.29 (.090)
1.52 (.060)
1.02 (.040)
3.94 (.155)
3.68 (.145)

PLASTIC: Standard and Power Dual-In-Line (cont'd.)

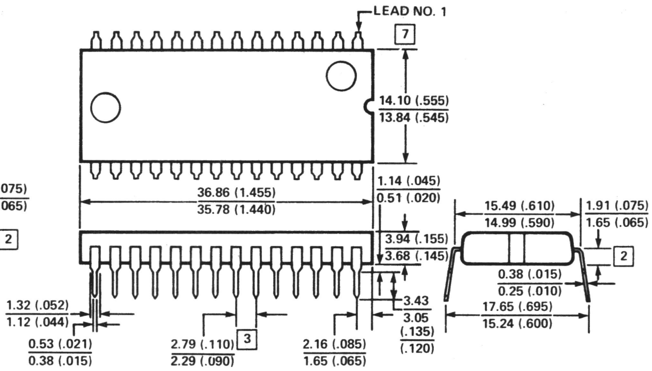
NNE/NNF Package


LEAD NO. 1 □
8.94 (.352)
8.45 (.345)
.0.80 (.031)
0.70 (.027)
30.48 (1.200)
29.97 (1.180)
0.89 (.035)
0.38 (.015)
3.94 (.155)
3.68 (.145)
3.43 (.135)
3.05 (.120)
1.40 (.055)
1.14 (.045)
.053 (.021)
.038 (0.15)
2.79 (.110)
2.29 (.090)
10.41 (.410)
9.91 (.390)
21.16 (.085)
1.88 (.074) □
0.38 (.015)
0.25 (.010)
12.57 (.495)
10.16 (.400)

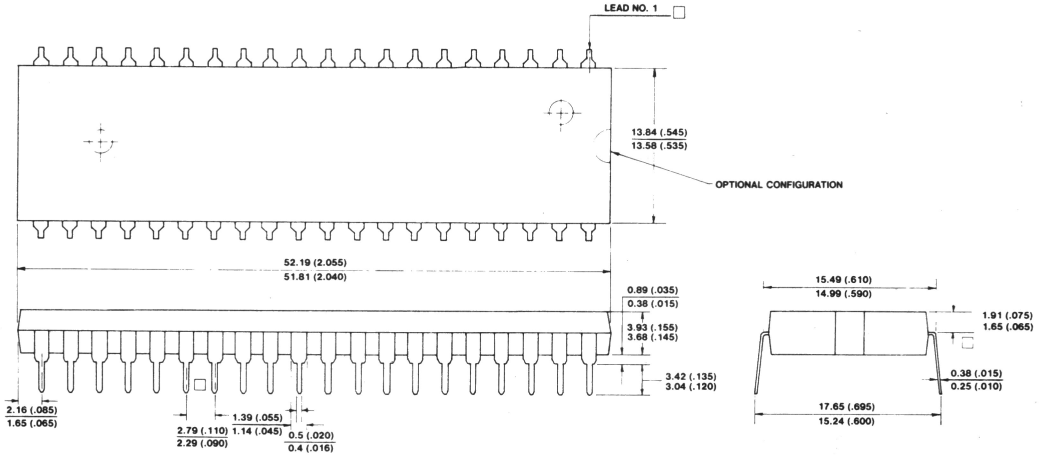
NN Package and NNA Package


LEAD NO. 1
7
14.10 (.555)
13.84 (.545)
31.88 (1.255)
31.50 (1.240)
1.14 (.045)
0.51 (.020)
15.49 (.610)
14.99 (.590)
1.91 (.075)
1.65 (.065)
2
0.38 (.015)
0.25 (.010)
17.65 (.695)
15.24 (.600)
3.43 (.135)
3.05 (.120)
1.32 (.052)
1.12 (.044)
0.53 (.021)
0.38 (.015)
3
2.79 (.110)
2.29 (.090)
2.16 (.085)
1.65 (.065)
3.94 (.155)
3.68 (.145)

NQ Package and NQA Package

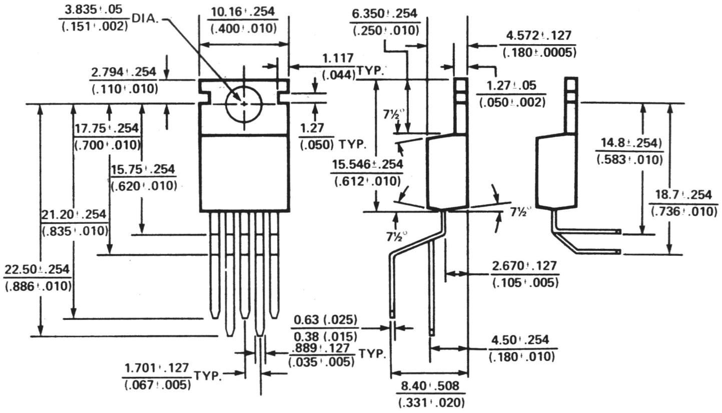

LEAD NO. 1
7
14.10 (.555)
13.84 (.545)
1.14 (.045)
0.51 (.020)
36.86 (1.455)
35.78 (1.440)
3.94 (.155)
3.68 (.145)
15.49 (.610)
14.99 (.590)
1.91 (.075)
1.65 (.065)
2
0.38 (.015)
0.25 (.010)
17.65 (.695)
15.24 (.600)
3.43
3.05
(.135)
(.120)
1.32 (.052)
1.12 (.044)
0.53 (.021)
0.38 (.015)
2.79 (.110)
2.29 (.090)
3
2.16 (.085)
1.65 (.065)

NW Package and NWA Package


LEAD NO. 1 □
13.84 (.545)
13.58 (.535)
OPTIONAL CONFIGURATION
52.19 (2.055)
51.81 (2.040)
0.89 (.035)
0.38 (.015)
3.93 (.155)
3.68 (.145)
3.42 (.135)
3.04 (.120)
2.16 (.085)
1.65 (.065)
□
1.39 (.055)
1.14 (.045)
2.79 (.110)
2.29 (.090)
0.5 (.020)
0.4 (.016)
15.49 (.610)
14.99 (.590)
1.91 (.075)
1.65 (.065)
□
0.38 (.015)
0.25 (.010)
17.65 (.695)
15.24 (.600)

PLASTIC: Power (Not Dual-In-Line) (cont'd.)

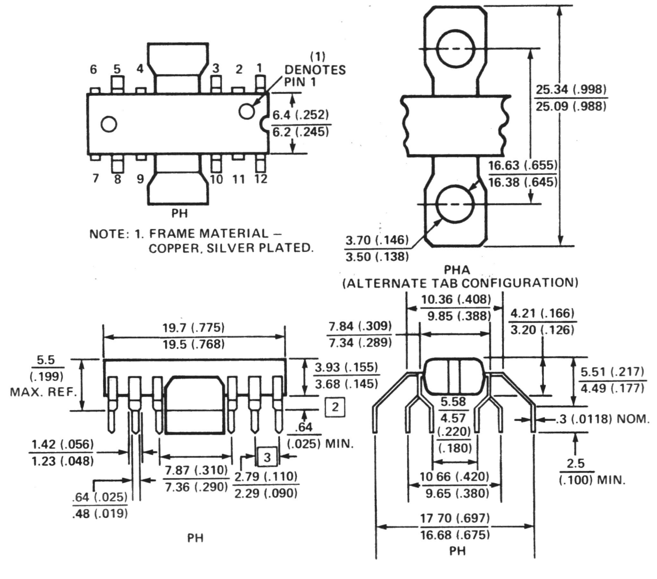
UEA Package


3.835±.05 (.151±.002) DIA.
10.16±.254 (.400±.010)
6.350±.254 (.250±.010)
4.572±.127 (.180±.0005)
1.117 (.044) TYP.
2.794±.254 (.110±.010)
1.27±.05 (.050±.002)
7½°
17.75±.254 (.700±.010)
1.27 (.050) TYP.
14.8±.254) (.583±.010)
15.75±.254 (.620±.010)
15.546±.254 (.612±.010)
18.7±.254 (.736±.010)
7½°
21.20±.254 (.835±.010)
7½°
2.670±.127 (.105±.005)
22.50±.254 (.886±.010)
0.63 (.025)
0.38 (.015)
.889±.127 (.035±.005) TYP.
4.50±.254 (.180±.010)
1.701±.127 (.067±.005) TYP.
8.40±.508 (.331±.020)

UGA Package

Package drawing not yet available.

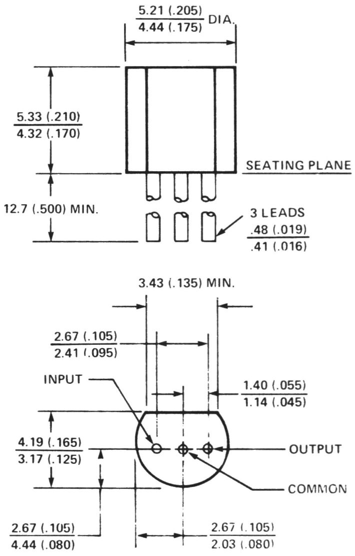
PH/PHA Package


6 5 4 3 2 1
(1) DENOTES PIN 1
6.4 (.252)
6.2 (.245)
7 8 9 10 11 12
PH
25.34 (.998)
25.09 (.988)
16.63 (.655)
16.38 (.645)
3.70 (.146)
3.50 (.138)
PHA
(ALTERNATE TAB CONFIGURATION)
19.7 (.775)
19.5 (.768)
5.5 (.199) MAX. REF.
3.93 (.155)
3.68 (.145)
2
.64 (.025) MIN.
1.42 (.056)
1.23 (.048)
7.87 (.310)
7.36 (.290)
3
2.79 (.110)
2.29 (.090)
.64 (.025)
.48 (.019)
PH
10.36 (.408)
9.85 (.388)
7.84 (.309)
7.34 (.289)
4.21 (.166)
3.20 (.126)
5.51 (.217)
4.49 (.177)
5.58
4.57
(.220)
(.180)
.3 (.0118) NOM.
10.66 (.420)
9.65 (.380)
2.5 (.100) MIN.
17.70 (.697)
16.68 (.675)
PH

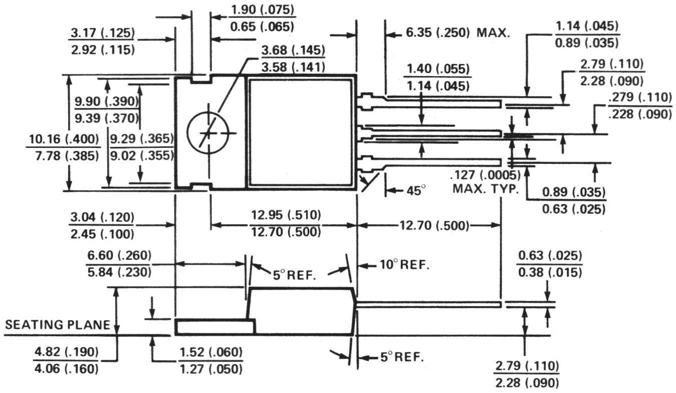
NOTE: 1. FRAME MATERIAL – COPPER, SILVER PLATED.

PLASTIC: Power (Not Dual-In-Line)

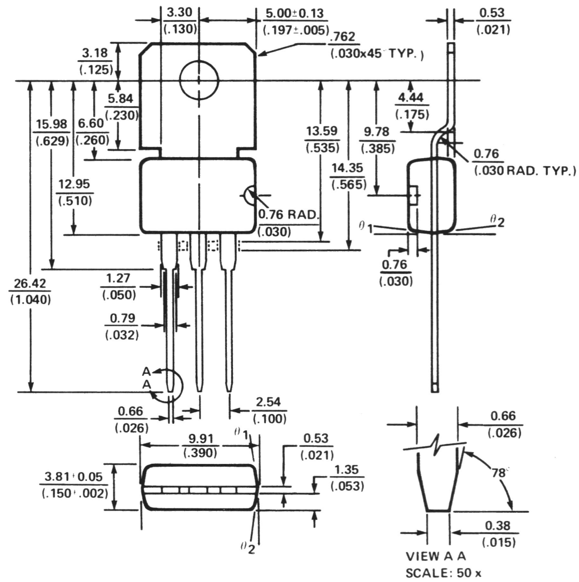
S Package


5.21 (.205)
4.44 (.175) DIA.
5.33 (.210)
4.32 (.170)
SEATING PLANE
12.7 (.500) MIN.
3 LEADS
.48 (.019)
.41 (.016)
3.43 (.135) MIN.
2.67 (.105)
2.41 (.095)
INPUT
1.40 (.055)
1.14 (.045)
4.19 (.165)
3.17 (.125)
OUTPUT
COMMON
2.67 (.105)
4.44 (.080)
2.67 (.105)
2.03 (.080)

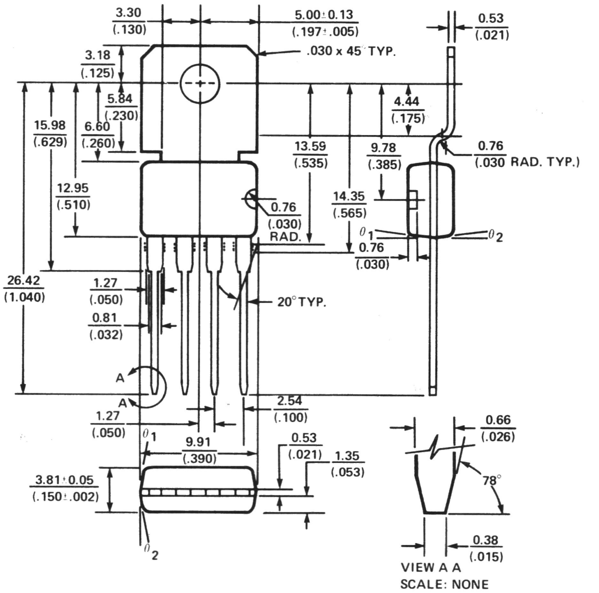
UCA Package


1.90 (.075)
0.65 (.065)
3.17 (.125)
2.92 (.115)
3.68 (.145)
3.58 (.141)
6.35 (.250) MAX.
1.14 (.045)
0.89 (.035)
1.40 (.055)
1.14 (.045)
2.79 (.110)
2.28 (.090)
.279 (.110)
.228 (.090)
9.90 (.390)
9.39 (.370)
10.16 (.400)
7.78 (.385)
9.29 (.365)
9.02 (.355)
45°
.127 (.0005)
MAX. TYP.
0.89 (.035)
0.63 (.025)
3.04 (.120)
2.45 (.100)
12.95 (.510)
12.70 (.500)
12.70 (.500)
6.60 (.260)
5.84 (.230)
5° REF.
10° REF.
0.63 (.025)
0.38 (.015)
SEATING PLANE
4.82 (.190)
4.06 (.160)
1.52 (.060)
1.27 (.050)
5° REF.
2.79 (.110)
2.28 (.090)

UC Package

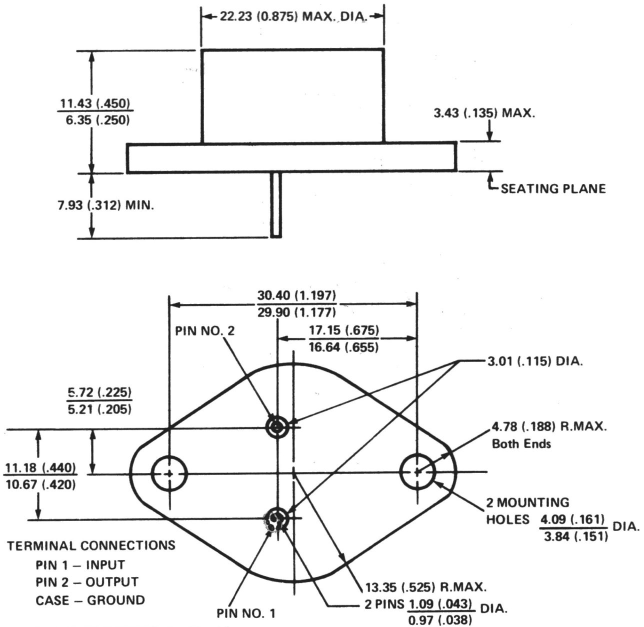

3.30
(.130)
5.00±0.13
(.197±.005)
.762
(.030x45° TYP.)
0.53
(.021)
3.18
(.125)
5.84
(.230)
15.98
(.629)
6.60
(.260)
4.44
(.175)
13.59
(.535)
9.78
(.385)
0.76
(.030 RAD. TYP.)
14.35
(.565)
12.95
(.510)
0.76 RAD.
(.030)
θ1
θ2
0.76
(.030)
26.42
(1.040)
1.27
(.050)
0.79
(.032)
A
A
0.66
(.026)
2.54
(.100)
9.91
(.390)
θ1
0.53
(.021)
1.35
(.053)
3.81±0.05
(.150±.002)
θ2
0.66
(.026)
78°
0.38
(.015)
VIEW A A
SCALE: 50 x

UD Package


3.30
(.130)
5.00±0.13
(.197±.005)
.030 x 45° TYP.
0.53
(.021)
3.18
(.125)
5.84
(.230)
15.98
(.629)
6.60
(.260)
4.44
(.175)
13.59
(.535)
9.78
(.385)
0.76
(.030 RAD. TYP.)
14.35
(.565)
12.95
(.510)
0.76
(.030)
RAD.
θ1
θ2
0.76
(.030)
26.42
(1.040)
1.27
(.050)
0.81
(.032)
20° TYP.
A
A
2.54
(.100)
1.27
(.050)
θ1
9.91
(.390)
0.53
(.021)
1.35
(.053)
3.81±0.05
(.150±.002)
θ2
0.66
(.026)
78°
0.38
(.015)
VIEW A A
SCALE: NONE

HERMETIC: Metal Headers

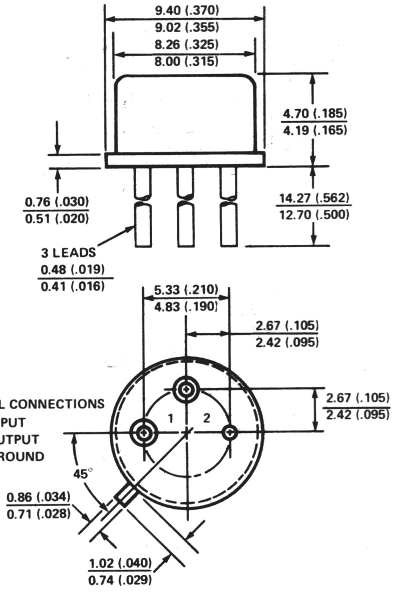
K Package (formerly DA)


22.23 (0.875) MAX. DIA.
11.43 (.450)
6.35 (.250)
3.43 (.135) MAX.
SEATING PLANE
7.93 (.312) MIN.
30.40 (1.197)
29.90 (1.177)
PIN NO. 2
17.15 (.675)
16.64 (.655)
3.01 (.115) DIA.
5.72 (.225)
5.21 (.205)
4.78 (.188) R.MAX.
Both Ends
11.18 (.440)
10.67 (.420)
2 MOUNTING
HOLES 4.09 (.161) / 3.84 (.151) DIA.
13.35 (.525) R.MAX.
2 PINS 1.09 (.043) / 0.97 (.038) DIA.
PIN NO. 1

TERMINAL CONNECTIONS
PIN 1 – INPUT
PIN 2 – OUTPUT
CASE – GROUND

CONSTRUCTION NOTES: 9a, 10a, 11a

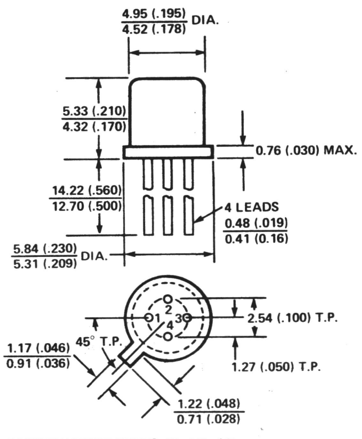
HBA Package (formerly DB)


9.40 (.370)
9.02 (.355)
8.26 (.325)
8.00 (.315)
4.70 (.185)
4.19 (.165)
0.76 (.030)
0.51 (.020)
14.27 (.562)
12.70 (.500)
3 LEADS
0.48 (.019)
0.41 (.016)
5.33 (.210)
4.83 (.190)
2.67 (.105)
2.42 (.095)
2.67 (.105)
2.42 (.095)
1
2
45°
0.86 (.034)
0.71 (.028)
1.02 (.040)
0.74 (.029)

TERMINAL CONNECTIONS
PIN 1 – INPUT
PIN 2 – OUTPUT
CASE – GROUND

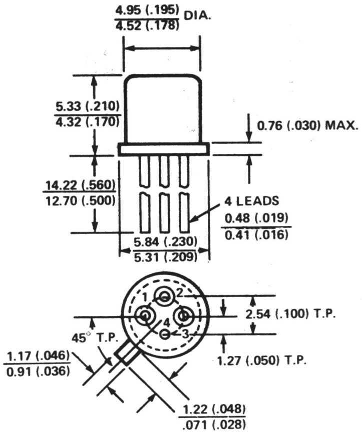
CONSTRUCTION NOTES: 9b, 10b, 11b

DC Package


4.95 (.195) / 4.52 (.178) DIA.
5.33 (.210)
4.32 (.170)
0.76 (.030) MAX.
14.22 (.560)
12.70 (.500)
4 LEADS
0.48 (.019)
0.41 (0.16)
5.84 (.230) / 5.31 (.209) DIA.
1
2
3
4
2.54 (.100) T.P.
45° T.P.
1.17 (.046)
0.91 (.036)
1.27 (.050) T.P.
1.22 (.048)
0.71 (.028)

CONSTRUCTION NOTES: 9b, 10b, 11b

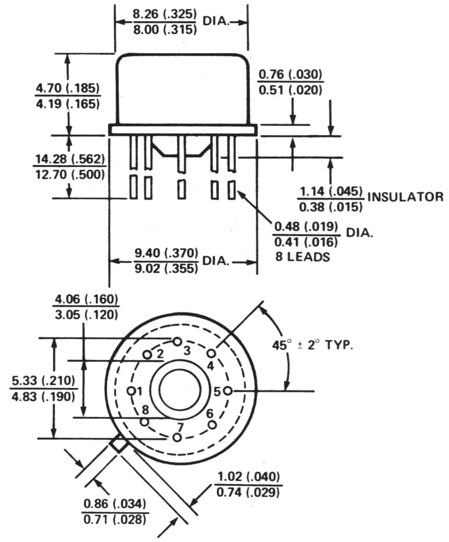
DE Package


4.95 (.195) / 4.52 (.178) DIA.
5.33 (.210)
4.32 (.170)
0.76 (.030) MAX.
14.22 (.560)
12.70 (.500)
4 LEADS
0.48 (.019)
0.41 (.016)
5.84 (.230)
5.31 (.209)
1
2
3
4
2.54 (.100) T.P.
45° T.P.
1.17 (.046)
0.91 (.036)
1.27 (.050) T.P.
1.22 (.048)
.071 (.028)

CONSTRUCTION NOTES: 9b, 10c, 11b

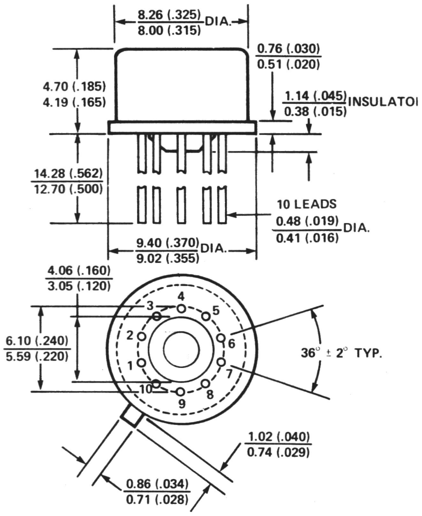
HERMETIC: Metal Headers (cont'd.)

HEA Package (formerly T)


8.26 (.325) / 8.00 (.315) DIA.
4.70 (.185) / 4.19 (.165)
0.76 (.030) / 0.51 (.020)
14.28 (.562) / 12.70 (.500)
1.14 (.045) / 0.38 (.015) INSULATOR
0.48 (.019) / 0.41 (.016) DIA.
9.40 (.370) / 9.02 (.355) DIA.
8 LEADS
4.06 (.160) / 3.05 (.120)
45° ± 2° TYP.
5.33 (.210) / 4.83 (.190)
1 2 3 4 5 6 7 8
1.02 (.040) / 0.74 (.029)
0.86 (.034) / 0.71 (.028)

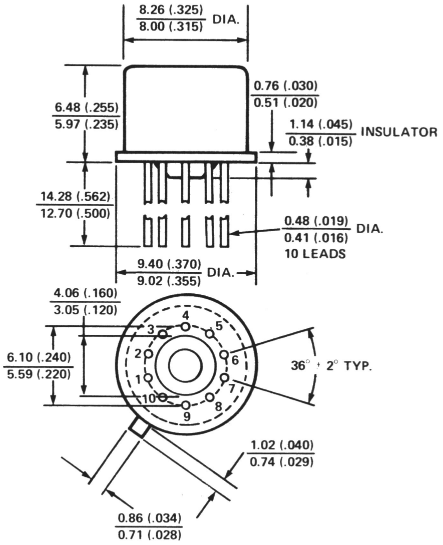
CONSTRUCTION NOTES: 9b, 10c, 11b

HFA Package (formerly K)


8.26 (.325) / 8.00 (.315) DIA.
0.76 (.030) / 0.51 (.020)
4.70 (.185) / 4.19 (.165)
1.14 (.045) / 0.38 (.015) INSULATOI
14.28 (.562) / 12.70 (.500)
10 LEADS
0.48 (.019) / 0.41 (.016) DIA.
9.40 (.370) / 9.02 (.355) DIA.
4.06 (.160) / 3.05 (.120)
6.10 (.240) / 5.59 (.220)
1 2 3 4 5 6 7 8 9 10
36° ± 2° TYP.
1.02 (.040) / 0.74 (.029)
0.86 (.034) / 0.71 (.028)

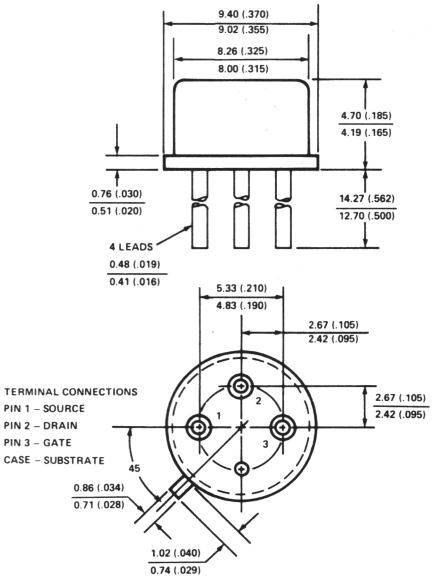
CONSTRUCTION NOTES: 9b, 10c, 11b

HFC Package (formerly L)


8.26 (.325) / 8.00 (.315) DIA.
6.48 (.255) / 5.97 (.235)
0.76 (.030) / 0.51 (.020)
1.14 (.045) / 0.38 (.015) INSULATOR
14.28 (.562) / 12.70 (.500)
0.48 (.019) / 0.41 (.016) DIA.
10 LEADS
9.40 (.370) / 9.02 (.355) DIA.
4.06 (.160) / 3.05 (.120)
6.10 (.240) / 5.59 (.220)
1 2 3 4 5 6 7 8 9 10
36° ± 2° TYP.
1.02 (.040) / 0.74 (.029)
0.86 (.034) / 0.71 (.028)

CONSTRUCTION NOTES: 9b, 10c, 11b

HCA Package

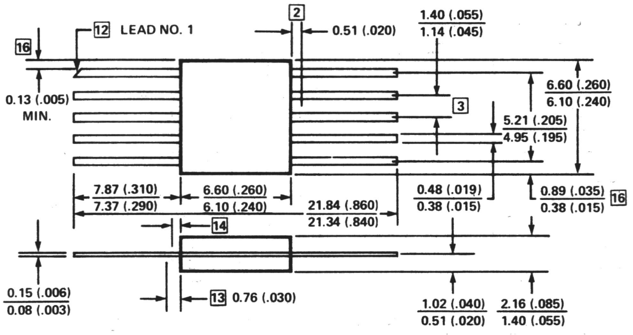

9.40 (.370) / 9.02 (.355)
8.26 (.325) / 8.00 (.315)
4.70 (.185) / 4.19 (.165)
0.76 (.030) / 0.51 (.020)
14.27 (.562) / 12.70 (.500)
4 LEADS
0.48 (.019) / 0.41 (.016)
5.33 (.210) / 4.83 (.190)
2.67 (.105) / 2.42 (.095)
2.67 (.105) / 2.42 (.095)
1 2 3
45
0.86 (.034) / 0.71 (.028)
1.02 (.040) / 0.74 (.029)

TERMINAL CONNECTIONS
PIN 1 – SOURCE
PIN 2 – DRAIN
PIN 3 – GATE
CASE – SUBSTRATE

CONSTRUCTION NOTES: 9b, 10b, 11b

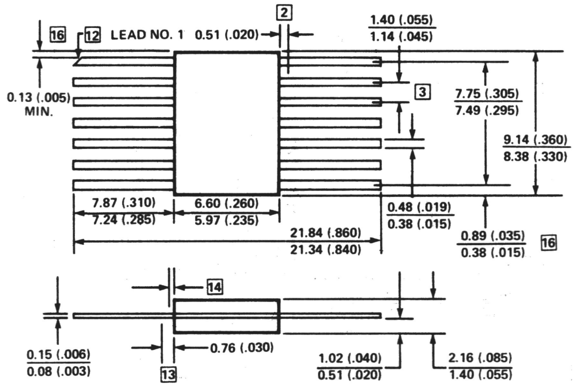
HERMETIC: Flat Packs

WF Package


12 LEAD NO. 1
2
0.51 (.020)
1.40 (.055)
1.14 (.045)
16
0.13 (.005)
MIN.
6.60 (.260)
6.10 (.240)
3
5.21 (.205)
4.95 (.195)
7.87 (.310)
7.37 (.290)
6.60 (.260)
6.10 (.240)
21.84 (.860)
21.34 (.840)
0.48 (.019)
0.38 (.015)
0.89 (.035)
0.38 (.015)
16
14
0.15 (.006)
0.08 (.003)
13 0.76 (.030)
1.02 (.040)
0.51 (.020)
2.16 (.085)
1.40 (.055)

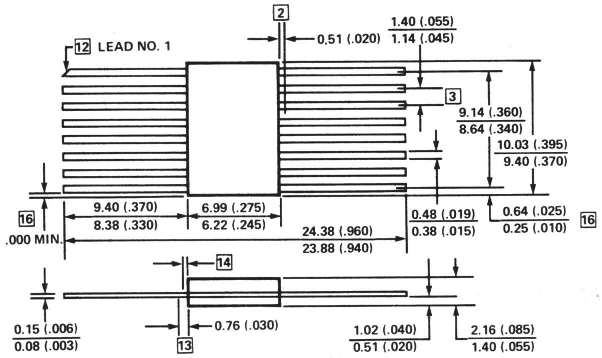
CONSTRCUTION NOTES: 9c, 10d, 11c

WH Package


16
12 LEAD NO. 1
0.51 (.020)
2
1.40 (.055)
1.14 (.045)
0.13 (.005)
MIN.
3
7.75 (.305)
7.49 (.295)
9.14 (.360)
8.38 (.330)
7.87 (.310)
7.24 (.285)
6.60 (.260)
5.97 (.235)
0.48 (.019)
0.38 (.015)
21.84 (.860)
21.34 (.840)
0.89 (.035)
0.38 (.015)
16
14
0.15 (.006)
0.08 (.003)
0.76 (.030)
13
1.02 (.040)
0.51 (.020)
2.16 (.085)
1.40 (.055)

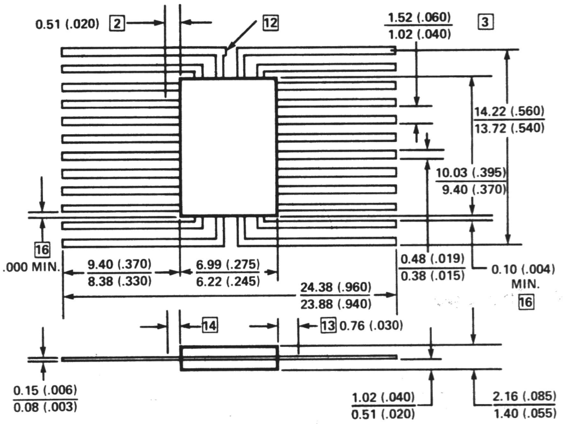
CONSTRUCTION NOTES: 9c, 10d, 11c

WJ Package


2
12 LEAD NO. 1
0.51 (.020)
1.40 (.055)
1.14 (.045)
3
9.14 (.360)
8.64 (.340)
10.03 (.395)
9.40 (.370)
16
.000 MIN.
9.40 (.370)
8.38 (.330)
6.99 (.275)
6.22 (.245)
24.38 (.960)
23.88 (.940)
0.48 (.019)
0.38 (.015)
0.64 (.025)
0.25 (.010)
16
14
0.15 (.006)
0.08 (.003)
0.76 (.030)
13
1.02 (.040)
0.51 (.020)
2.16 (.085)
1.40 (.055)

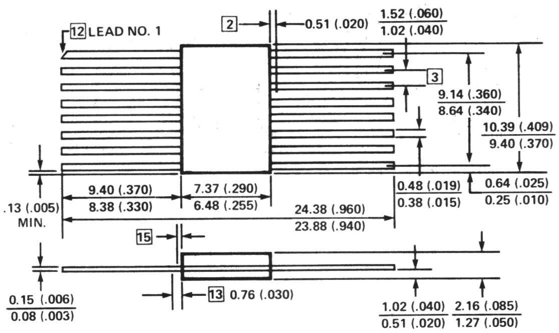
CONSTRUCTION NOTES: 9c, 10d, 11c

WN Package


0.51 (.020)
2
12
1.52 (.060)
1.02 (.040)
3
14.22 (.560)
13.72 (.540)
10.03 (.395)
9.40 (.370)
16
.000 MIN.
9.40 (.370)
8.38 (.330)
6.99 (.275)
6.22 (.245)
24.38 (.960)
23.88 (.940)
0.48 (.019)
0.38 (.015)
0.10 (.004)
MIN.
16
14
13 0.76 (.030)
0.15 (.006)
0.08 (.003)
1.02 (.040)
0.51 (.020)
2.16 (.085)
1.40 (.055)

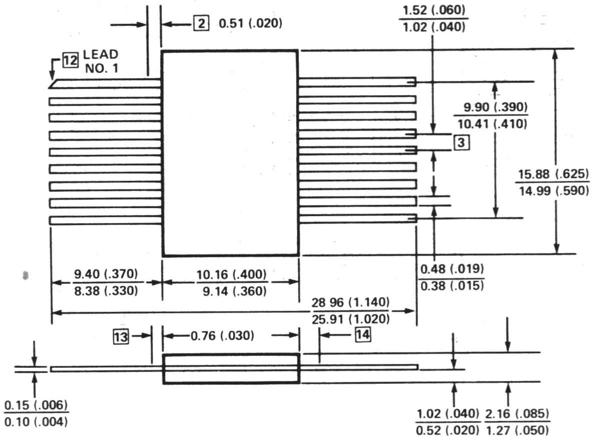
CONSTRUCTION NOTES: 9c, 10d, 11c

RJA Package


12 LEAD NO. 1
2
0.51 (.020)
1.52 (.060)
1.02 (.040)
3
9.14 (.360)
8.64 (.340)
10.39 (.409)
9.40 (.370)
.13 (.005)
MIN.
9.40 (.370)
8.38 (.330)
7.37 (.290)
6.48 (.255)
24.38 (.960)
23.88 (.940)
0.48 (.019)
0.38 (.015)
0.64 (.025)
0.25 (.010)
15
0.15 (.006)
0.08 (.003)
13 0.76 (.030)
1.02 (.040)
0.51 (.020)
2.16 (.085)
1.27 (.050)

RJA CONSTRUCTION NOTES: 9c, 10e, 11e

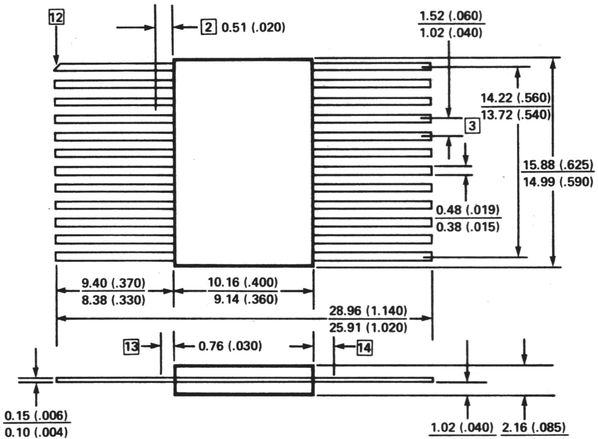
RKA Package


2 0.51 (.020)
1.52 (.060)
1.02 (.040)
12 LEAD NO. 1
9.90 (.390)
10.41 (.410)
3
15.88 (.625)
14.99 (.590)
9.40 (.370)
8.38 (.330)
10.16 (.400)
9.14 (.360)
0.48 (.019)
0.38 (.015)
28 96 (1.140)
25.91 (1.020)
13
0.76 (.030)
14
0.15 (.006)
0.10 (.004)
1.02 (.040)
0.52 (.020)
2.16 (.085)
1.27 (.050)

CONSTRUCTION NOTES: 9c, 10e, 11e

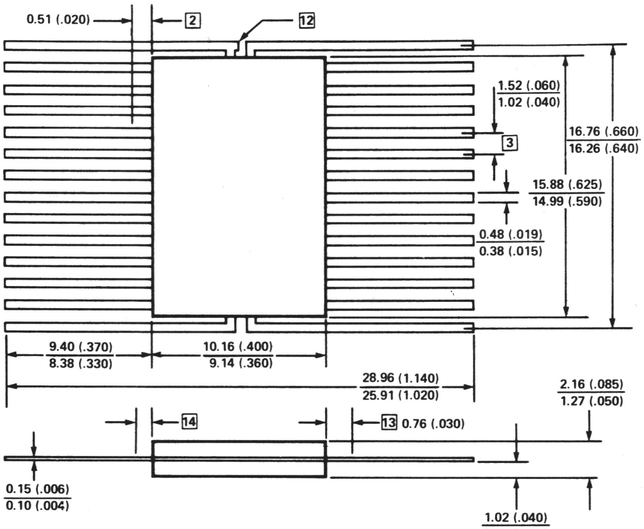
HERMETIC: Flat Packs (cont'd.)

RNA Package


12
2 0.51 (.020)
1.52 (.060)
1.02 (.040)
14.22 (.560)
13.72 (.540)
3
15.88 (.625)
14.99 (.590)
0.48 (.019)
0.38 (.015)
9.40 (.370)
8.38 (.330)
10.16 (.400)
9.14 (.360)
28.96 (1.140)
25.91 (1.020)
13
0.76 (.030)
14
0.15 (.006)
0.10 (.004)
1.02 (.040)
0.51 (.020)
2.16 (.085)
1.27 (.050)

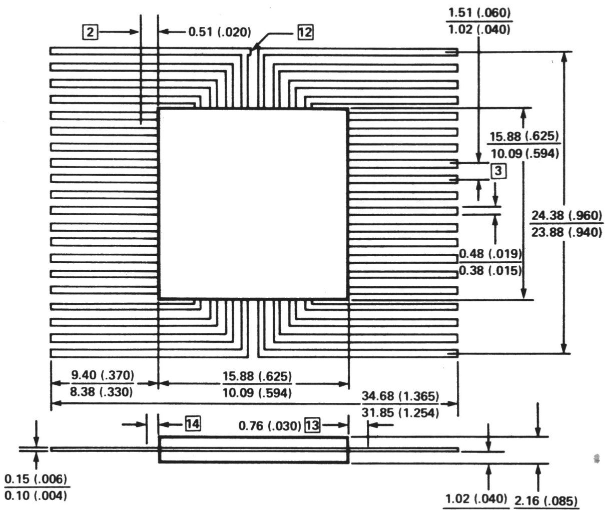
CONSTRUCTION NOTES: 9c, 10e, 11e

RQA Package


0.51 (.020)
2
12
1.52 (.060)
1.02 (.040)
3
16.76 (.660)
16.26 (.640)
15.88 (.625)
14.99 (.590)
0.48 (.019)
0.38 (.015)
9.40 (.370)
8.38 (.330)
10.16 (.400)
9.14 (.360)
28.96 (1.140)
25.91 (1.020)
2.16 (.085)
1.27 (.050)
14
13 0.76 (.030)
0.15 (.006)
0.10 (.004)
1.02 (.040)
0.51 (.020)

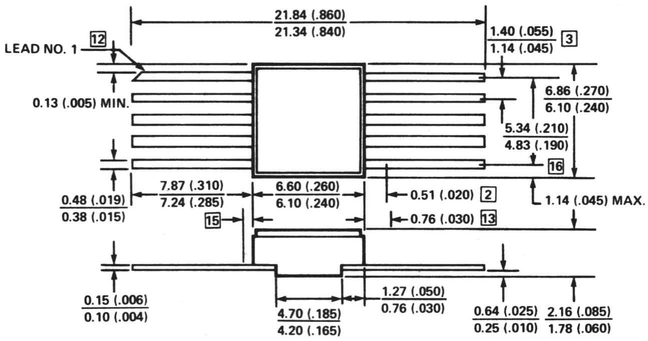
CONSTRUCTION NOTES: 9c, 10e, 11e

RWA Package


2
0.51 (.020)
12
1.51 (.060)
1.02 (.040)
15.88 (.625)
10.09 (.594)
3
24.38 (.960)
23.88 (.940)
0.48 (.019)
0.38 (.015)
9.40 (.370)
8.38 (.330)
15.88 (.625)
10.09 (.594)
34.68 (1.365)
31.85 (1.254)
14
0.76 (.030) 13
0.15 (.006)
0.10 (.004)
1.02 (.040)
0.51 (.020)
2.16 (.085)
1.27 (.050)

CONSTRUCTION NOTES: 9c, 10e, 11e

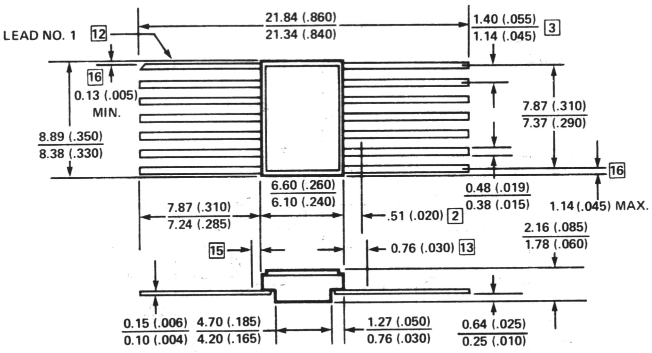
QFA Package


21.84 (.860)
21.34 (.840)
1.40 (.055)
1.14 (.045)
3
LEAD NO. 1
12
0.13 (.005) MIN.
6.86 (.270)
6.10 (.240)
5.34 (.210)
4.83 (.190)
16
0.48 (.019)
0.38 (.015)
7.87 (.310)
7.24 (.285)
6.60 (.260)
6.10 (.240)
0.51 (.020) 2
1.14 (.045) MAX.
0.76 (.030) 13
15
0.15 (.006)
0.10 (.004)
4.70 (.185)
4.20 (.165)
1.27 (.050)
0.76 (.030)
0.64 (.025)
0.25 (.010)
2.16 (.085)
1.78 (.060)

CONSTRUCTION NOTES: 9d, 10f, 11c

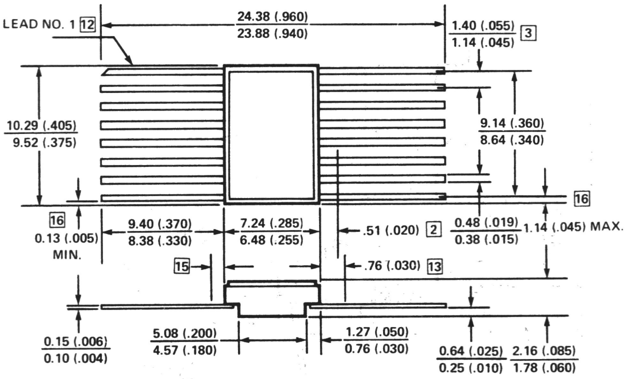
HERMETIC: Flat Packs (cont'd.)

QHA Package


LEAD NO. 1 12
21.84 (.860)
21.34 (.840)
1.40 (.055)
1.14 (.045) 3
16
0.13 (.005)
MIN.
8.89 (.350)
8.38 (.330)
7.87 (.310)
7.37 (.290)
16
6.60 (.260)
6.10 (.240)
0.48 (.019)
0.38 (.015)
1.14 (.045) MAX.
7.87 (.310)
7.24 (.285)
.51 (.020) 2
2.16 (.085)
1.78 (.060)
15
0.76 (.030) 13
0.15 (.006)
0.10 (.004)
4.70 (.185)
4.20 (.165)
1.27 (.050)
0.76 (.030)
0.64 (.025)
0.25 (.010)

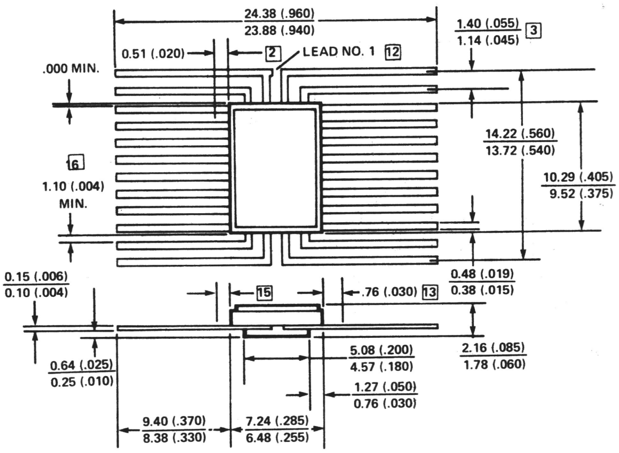
CONSTRUCTION NOTES: 9d, 10f, 11c

QJA Package


LEAD NO. 1 12
24.38 (.960)
23.88 (.940)
1.40 (.055)
1.14 (.045) 3
10.29 (.405)
9.52 (.375)
9.14 (.360)
8.64 (.340)
16
16
0.13 (.005)
MIN.
9.40 (.370)
8.38 (.330)
7.24 (.285)
6.48 (.255)
.51 (.020) 2
0.48 (.019)
0.38 (.015)
1.14 (.045) MAX.
15
.76 (.030) 13
0.15 (.006)
0.10 (.004)
5.08 (.200)
4.57 (.180)
1.27 (.050)
0.76 (.030)
0.64 (.025)
0.25 (.010)
2.16 (.085)
1.78 (.060)

CONSTRUCTION NOTES: 9d, 10f, 11c

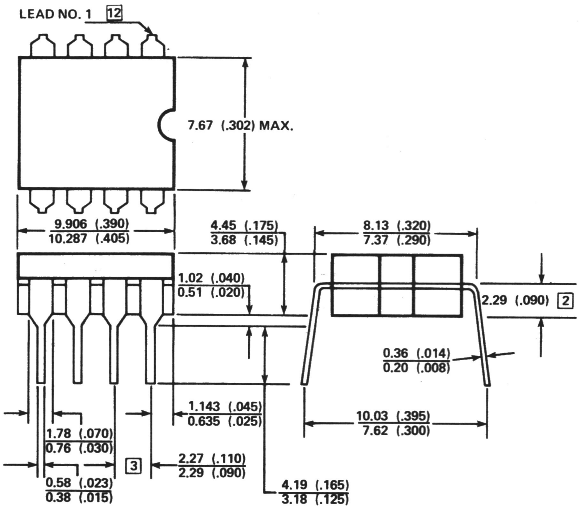
QNA Package


24.38 (.960)
23.88 (.940)
1.40 (.055)
1.14 (.045) 3
0.51 (.020)
2
LEAD NO. 1 12
.000 MIN.
14.22 (.560)
13.72 (.540)
16
1.10 (.004)
MIN.
10.29 (.405)
9.52 (.375)
0.15 (.006)
0.10 (.004)
15
.76 (.030) 13
0.48 (.019)
0.38 (.015)
0.64 (.025)
0.25 (.010)
5.08 (.200)
4.57 (.180)
2.16 (.085)
1.78 (.060)
1.27 (.050)
0.76 (.030)
9.40 (.370)
8.38 (.330)
7.24 (.285)
6.48 (.255)

CONSTRUCTION NOTES: 9d, 10f, 11c

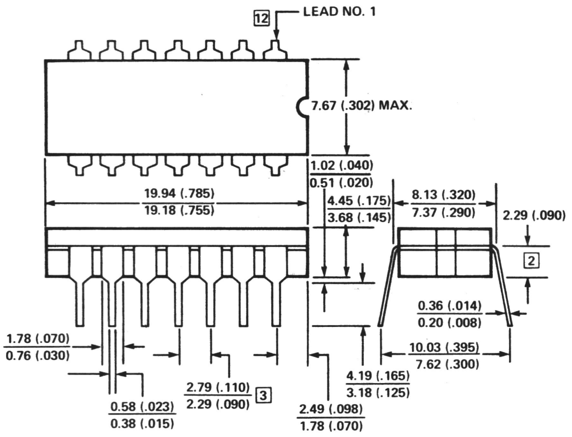
HERMETIC: Cerdip

FE Package


LEAD NO. 1 12
7.67 (.302) MAX.
9.906 (.390)
10.287 (.405)
4.45 (.175)
3.68 (.145)
8.13 (.320)
7.37 (.290)
1.02 (.040)
0.51 (.020)
2.29 (.090) 2
0.36 (.014)
0.20 (.008)
1.143 (.045)
0.635 (.025)
10.03 (.395)
7.62 (.300)
1.78 (.070)
0.76 (.030)
3
2.27 (.110)
2.29 (.090)
0.58 (.023)
0.38 (.015)
4.19 (.165)
3.18 (.125)

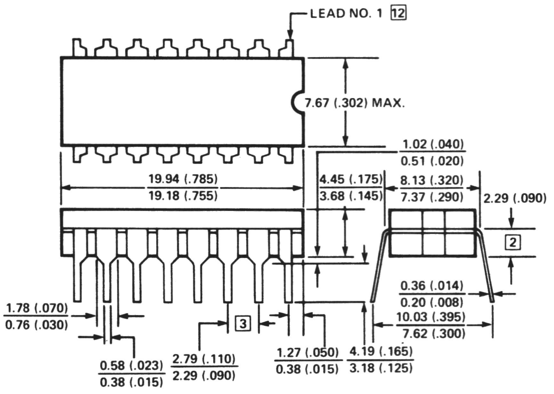
CONSTRUCTION NOTES: 9C, 10D, 11C

FH Package


12 LEAD NO. 1
7.67 (.302) MAX.
1.02 (.040)
0.51 (.020)
19.94 (.785)
19.18 (.755)
4.45 (.175)
3.68 (.145)
8.13 (.320)
7.37 (.290)
2.29 (.090)
2
0.36 (.014)
0.20 (.008)
1.78 (.070)
0.76 (.030)
10.03 (.395)
7.62 (.300)
2.79 (.110)
2.29 (.090)
3
4.19 (.165)
3.18 (.125)
0.58 (.023)
0.38 (.015)
2.49 (.098)
1.78 (.070)

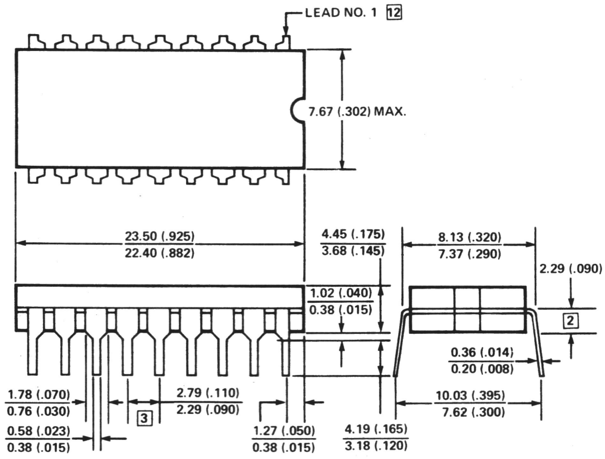
CONSTRUCTION NOTES: 9c, 10d, 11c

FJ Package


LEAD NO. 1 12
7.67 (.302) MAX.
1.02 (.040)
0.51 (.020)
19.94 (.785)
19.18 (.755)
4.45 (.175)
3.68 (.145)
8.13 (.320)
7.37 (.290)
2.29 (.090)
2
0.36 (.014)
0.20 (.008)
10.03 (.395)
7.62 (.300)
1.78 (.070)
0.76 (.030)
3
0.58 (.023)
0.38 (.015)
2.79 (.110)
2.29 (.090)
1.27 (.050)
0.38 (.015)
4.19 (.165)
3.18 (.125)

CONSTRUCTION NOTES: 9c, 10d, 11c

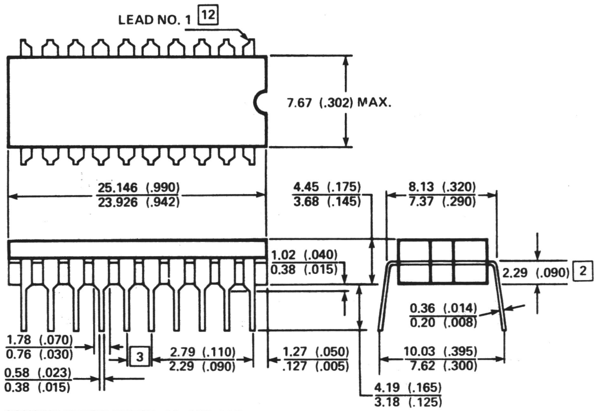
FK Package


LEAD NO. 1 12
7.67 (.302) MAX.
23.50 (.925)
22.40 (.882)
4.45 (.175)
3.68 (.145)
8.13 (.320)
7.37 (.290)
2.29 (.090)
1.02 (.040)
0.38 (.015)
2
0.36 (.014)
0.20 (.008)
1.78 (.070)
0.76 (.030)
2.79 (.110)
2.29 (.090)
3
10.03 (.395)
7.62 (.300)
0.58 (.023)
0.38 (.015)
1.27 (.050)
0.38 (.015)
4.19 (.165)
3.18 (.120)

CONSTRUCTION NOTES: 9c, 10d, 11c

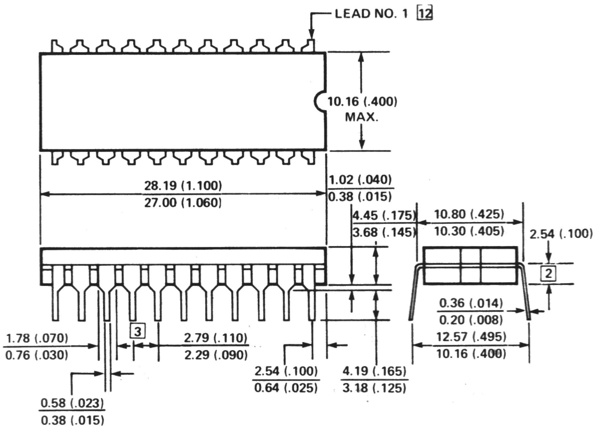
HERMETIC: Cerdip (cont'd.)

FL Package


LEAD NO. 1 12
7.67 (.302) MAX.
25.146 (.990)
23.926 (.942)
4.45 (.175)
3.68 (.145)
8.13 (.320)
7.37 (.290)
1.02 (.040)
0.38 (.015)
2.29 (.090) 2
0.36 (.014)
0.20 (.008)
1.78 (.070)
0.76 (.030)
3
2.79 (.110)
2.29 (.090)
1.27 (.050)
.127 (.005)
10.03 (.395)
7.62 (.300)
0.58 (.023)
0.38 (.015)
4.19 (.165)
3.18 (.125)

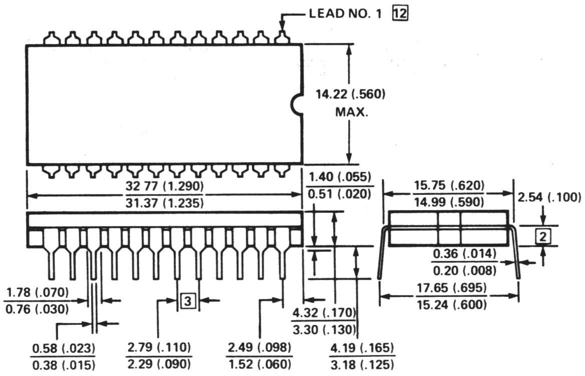
CONSTRUCTION NOTES: 9C, 10D, 11C

FM Package


LEAD NO. 1 12
10.16 (.400)
MAX.
28.19 (1.100)
27.00 (1.060)
1.02 (.040)
0.38 (.015)
4.45 (.175)
3.68 (.145)
10.80 (.425)
10.30 (.405)
2.54 (.100)
2
0.36 (.014)
0.20 (.008)
12.57 (.495)
10.16 (.400)
1.78 (.070)
0.76 (.030)
3
2.79 (.110)
2.29 (.090)
2.54 (.100)
0.64 (.025)
4.19 (.165)
3.18 (.125)
0.58 (.023)
0.38 (.015)

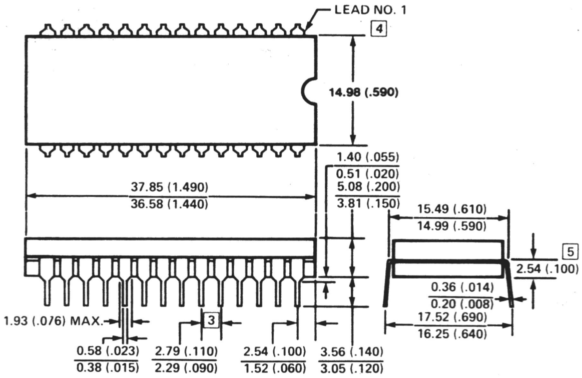
CONSTRUCTION NOTES: 9c, 10d, 11c

FN Package


LEAD NO. 1 12
14.22 (.560)
MAX.
32 77 (1.290)
31.37 (1.235)
1.40 (.055)
0.51 (.020)
15.75 (.620)
14.99 (.590)
2.54 (.100)
2
0.36 (.014)
0.20 (.008)
17.65 (.695)
15.24 (.600)
1.78 (.070)
0.76 (.030)
3
4.32 (.170)
3.30 (.130)
0.58 (.023)
0.38 (.015)
2.79 (.110)
2.29 (.090)
2.49 (.098)
1.52 (.060)
4.19 (.165)
3.18 (.125)

CONSTRUCTION NOTES: 9c. 10d, 11c

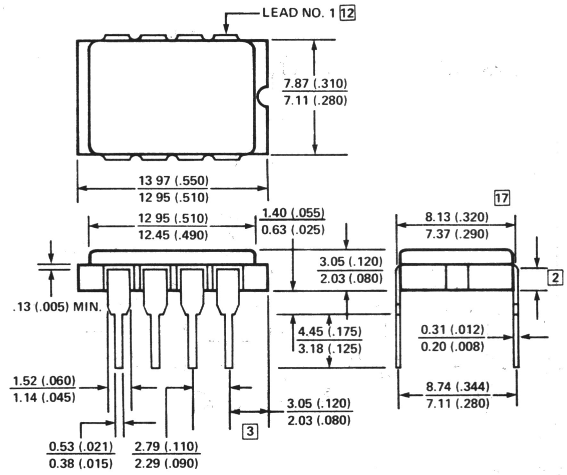
FQ Package


LEAD NO. 1
4
14.98 (.590)
1.40 (.055)
0.51 (.020)
5.08 (.200)
3.81 (.150)
37.85 (1.490)
36.58 (1.440)
15.49 (.610)
14.99 (.590)
5
2.54 (.100)
0.36 (.014)
0.20 (.008)
17.52 (.690)
16.25 (.640)
1.93 (.076) MAX.
3
0.58 (.023)
0.38 (.015)
2.79 (.110)
2.29 (.090)
2.54 (.100)
1.52 (.060)
3.56 (.140)
3.05 (.120)

CONSTRUCTIONS NOTES: 9c, 10d, 11c

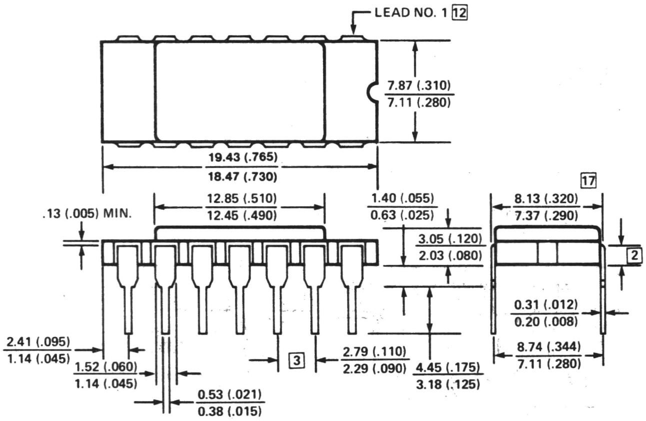
HERMETIC: Laminated Ceramic, Side Brazed Lead

IEA Package


LEAD NO. 1 12
7.87 (.310)
7.11 (.280)
13 97 (.550)
12 95 (.510)
12 95 (.510)
12.45 (.490)
1.40 (.055)
0.63 (.025)
17
8.13 (.320)
7.37 (.290)
3.05 (.120)
2.03 (.080)
2
.13 (.005) MIN.
4.45 (.175)
3.18 (.125)
0.31 (.012)
0.20 (.008)
1.52 (.060)
1.14 (.045)
8.74 (.344)
7.11 (.280)
3.05 (.120)
2.03 (.080)
3
0.53 (.021)
0.38 (.015)
2.79 (.110)
2.29 (.090)

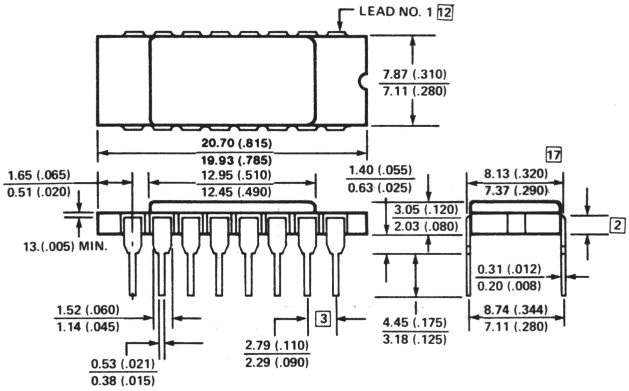
CONSTRUCTION NOTES: 9e, 10f, 11c

IHA Package


LEAD NO. 1 12
7.87 (.310)
7.11 (.280)
19.43 (.765)
18.47 (.730)
17
.13 (.005) MIN.
12.85 (.510)
12.45 (.490)
1.40 (.055)
0.63 (.025)
8.13 (.320)
7.37 (.290)
3.05 (.120)
2.03 (.080)
2
0.31 (.012)
0.20 (.008)
2.41 (.095)
1.14 (.045)
8.74 (.344)
7.11 (.280)
1.52 (.060)
1.14 (.045)
3
2.79 (.110)
2.29 (.090)
4.45 (.175)
3.18 (.125)
0.53 (.021)
0.38 (.015)

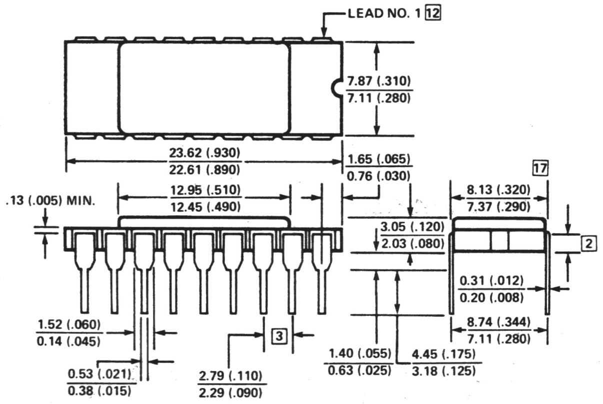
CONSTRUCTION NOTES: 9e, 10f, 11c

IJA Package


LEAD NO. 1 12
7.87 (.310)
7.11 (.280)
20.70 (.815)
19.93 (.785)
17
1.65 (.065)
0.51 (.020)
12.95 (.510)
12.45 (.490)
1.40 (.055)
0.63 (.025)
8.13 (.320)
7.37 (.290)
3.05 (.120)
2.03 (.080)
2
13.(.005) MIN.
0.31 (.012)
0.20 (.008)
1.52 (.060)
1.14 (.045)
3
8.74 (.344)
7.11 (.280)
4.45 (.175)
3.18 (.125)
2.79 (.110)
2.29 (.090)
0.53 (.021)
0.38 (.015)

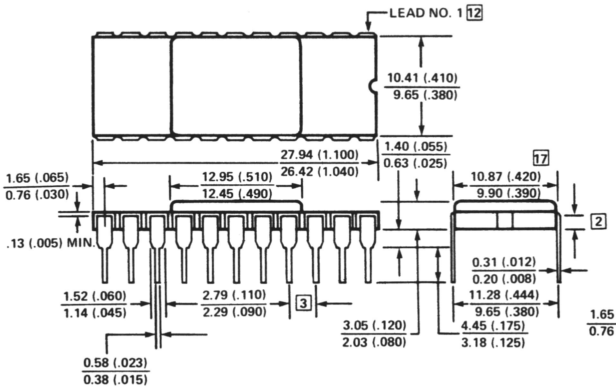
CONSTRUCTION NOTES: 9e, 10d,11c

IKA Package


LEAD NO. 1 12
7.87 (.310)
7.11 (.280)
23.62 (.930)
22.61 (.890)
1.65 (.065)
0.76 (.030)
17
.13 (.005) MIN.
12.95 (.510)
12.45 (.490)
8.13 (.320)
7.37 (.290)
3.05 (.120)
2.03 (.080)
2
0.31 (.012)
0.20 (.008)
1.52 (.060)
0.14 (.045)
8.74 (.344)
7.11 (.280)
3
1.40 (.055)
0.63 (.025)
4.45 (.175)
3.18 (.125)
0.53 (.021)
0.38 (.015)
2.79 (.110)
2.29 (.090)

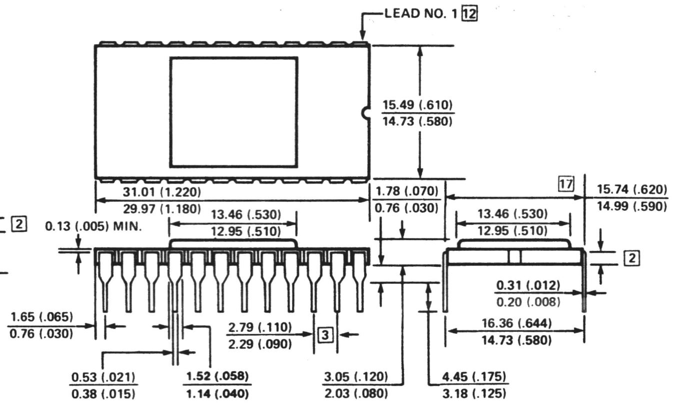
CONSTRUCTION NOTES: 9e, 10f, 11c

IMA Package


LEAD NO. 1 12
10.41 (.410)
9.65 (.380)
1.40 (.055)
0.63 (.025)
27.94 (1.100)
26.42 (1.040)
17
1.65 (.065)
0.76 (.030)
12.95 (.510)
12.45 (.490)
10.87 (.420)
9.90 (.390)
2
.13 (.005) MIN.
0.31 (.012)
0.20 (.008)
11.28 (.444)
9.65 (.380)
1.52 (.060)
1.14 (.045)
2.79 (.110)
2.29 (.090)
3
3.05 (.120)
2.03 (.080)
4.45 (.175)
3.18 (.125)
0.58 (.023)
0.38 (.015)

CONSTRUCTION NOTES: 9e, 10f, 11c

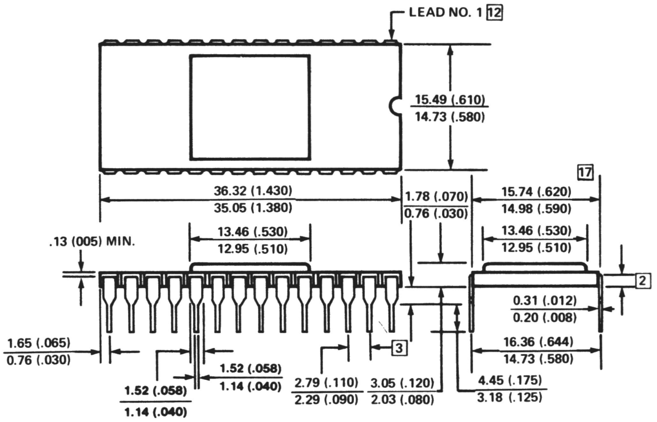
INC Package


LEAD NO. 1 12
15.49 (.610)
14.73 (.580)
31.01 (1.220)
29.97 (1.180)
1.78 (.070)
0.76 (.030)
17
15.74 (.620)
14.99 (.590)
0.13 (.005) MIN.
13.46 (.530)
12.95 (.510)
13.46 (.530)
12.95 (.510)
2
0.31 (.012)
0.20 (.008)
1.65 (.065)
0.76 (.030)
2.79 (.110)
2.29 (.090)
3
16.36 (.644)
14.73 (.580)
0.53 (.021)
0.38 (.015)
1.52 (.058)
1.14 (.040)
3.05 (.120)
2.03 (.080)
4.45 (.175)
3.18 (.125)

CONSTRUCTION NOTES: 9e, 10f, 11f (IND)

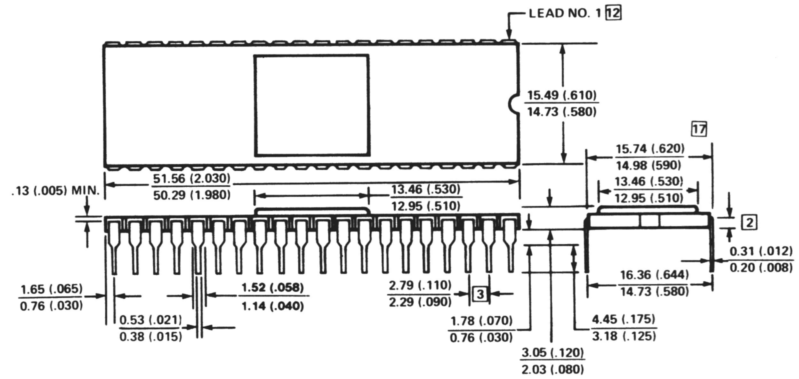
HERMETIC: Laminated Cermaic, Side Brazed Lead (cont'd.)

IQA Package


LEAD NO. 1 12
15.49 (.610)
14.73 (.580)
17
36.32 (1.430)
35.05 (1.380)
1.78 (.070)
0.76 (.030)
15.74 (.620)
14.98 (.590)
.13 (005) MIN.
13.46 (.530)
12.95 (.510)
13.46 (.530)
12.95 (.510)
2
0.31 (.012)
0.20 (.008)
1.65 (.065)
0.76 (.030)
3
16.36 (.644)
14.73 (.580)
1.52 (.058)
1.14 (.040)
1.52 (.058)
1.14 (.040)
2.79 (.110)
2.29 (.090)
3.05 (.120)
2.03 (.080)
4.45 (.175)
3.18 (.125)

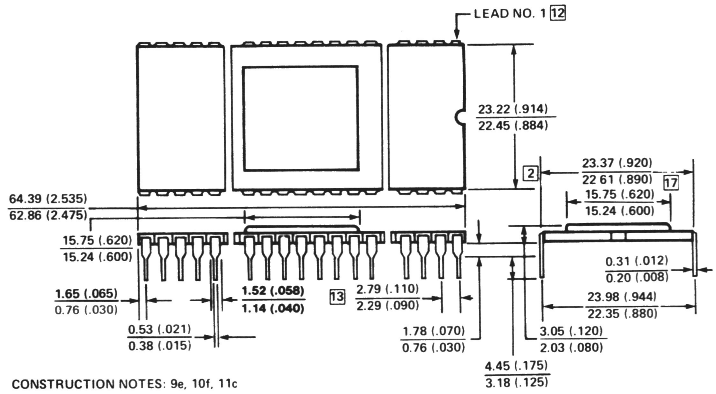
CONSTRUCTION NOTES: 9e, 10f, 11c

IWA Package


LEAD NO. 1 12
15.49 (.610)
14.73 (.580)
17
15.74 (.620)
14.98 (590)
51.56 (2.030)
50.29 (1.980)
.13 (.005) MIN.
13.46 (.530)
12.95 (.510)
13.46 (.530)
12.95 (.510)
2
0.31 (.012)
0.20 (.008)
16.36 (.644)
14.73 (.580)
1.65 (.065)
0.76 (.030)
1.52 (.058)
1.14 (.040)
2.79 (.110)
2.29 (.090)
3
0.53 (.021)
0.38 (.015)
1.78 (.070)
0.76 (.030)
4.45 (.175)
3.18 (.125)
3.05 (.120)
2.03 (.080)

CONSTRUCTION NOTES: 9e, 10f, 11c

IZA Package


LEAD NO. 1 12
23.22 (.914)
22.45 (.884)
2
23.37 (.920)
22 61 (.890)
17
15.75 (.620)
15.24 (.600)
64.39 (2.535)
62.86 (2.475)
15.75 (.620)
15.24 (.600)
0.31 (.012)
0.20 (.008)
1.65 (.065)
0.76 (.030)
1.52 (.058)
1.14 (.040)
13
2.79 (.110)
2.29 (.090)
23.98 (.944)
22.35 (.880)
0.53 (.021)
0.38 (.015)
1.78 (.070)
0.76 (.030)
3.05 (.120)
2.03 (.080)
4.45 (.175)
3.18 (.125)

CONSTRUCTION NOTES: 9e, 10f, 11c

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